ANALOG DEVICES

Dual/Quad Rail-to-Rail Operational Amplifiers

OP295/OP495

FEATURES

Rail-to-rail output swing
Single-supply operation: 3 V to 36 V
Low offset voltage: 300 μV
Gain bandwidth product: 75 kHz
High open-loop gain: 1000 V/mV
Unity-gain stable
Low supply current/per amplifier: 150 μA maximum

APPLICATIONS

Battery-operated instrumentation
Servo amplifiers
Actuator drives
Sensor conditioners
Power supply control

GENERAL DESCRIPTION

Rail-to-rail output swing combined with dc accuracy are the key features of the OP495 quad and OP295 dual CBCMOS operational amplifiers. By using a bipolar front end, lower noise and higher accuracy than those of CMOS designs have been achieved. Both input and output ranges include the negative supply, providing the user with zero-in/zero-out capability. For users of 3.3 V systems such as lithium batteries, the OP295/OP495 are specified for 3 V operation.

Maximum offset voltage is specified at 300 μV for 5 V operation, and the open-loop gain is a minimum of 1000 V/mV. This yields performance that can be used to implement high accuracy systems, even in single-supply designs.

The ability to swing rail-to-rail and supply 15 mA to the load makes the OP295/OP495 ideal drivers for power transistors and H bridges. This allows designs to achieve higher efficiencies and to transfer more power to the load than previously possible without the use of discrete components.

For applications such as transformers that require driving inductive loads, increases in efficiency are also possible. Stability while driving capacitive loads is another benefit of this design over CMOS rail-to-rail amplifiers. This is useful for driving coax cable or large FET transistors. The OP295/OP495 are stable with loads in excess of 300 pF.

PIN CONFIGURATIONS

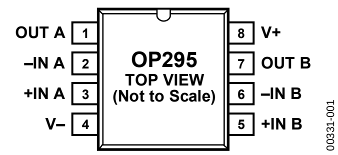


Figure 1. 8-Lead Narrow-Body SOIC_N S Suffix (R-8)

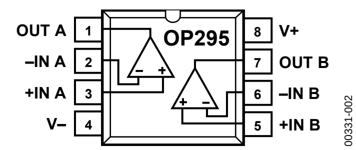


Figure 2. 8-Lead PDIP P Suffix (N-8)

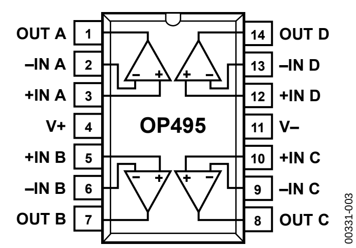


Figure 3. 14-Lead PDIP P Suffix (N-14)

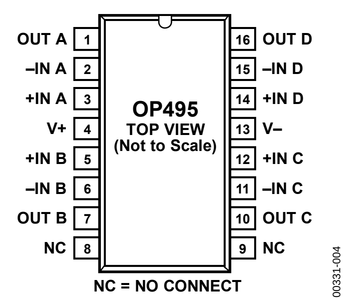


Figure 4. 16-Lead SOIC_W S Suffix (RW-16)

The OP295 and OP495 are specified over the extended industrial (–40°C to +125°C) temperature range. The OP295 is available in 8-lead PDIP and 8-lead SOIC_N surface-mount packages. The OP495 is available in 14-lead PDIP and 16-lead SOIC_W surface-mount packages.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_S = 5.0 V, V_{CM} = 2.5 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			30	300	µV
		−40°C ≤ T_A ≤ +125°C			800	µV
Input Bias Current	I_B			8	20	nA
		−40°C ≤ T_A ≤ +125°C			30	nA
Input Offset Current	I_{OS}			±1	±3	nA
		−40°C ≤ T_A ≤ +125°C			±5	nA
Input Voltage Range	V_{CM}		0		4.0	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 4.0 V, −40°C ≤ T_A ≤ +125°C	90	110		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, 0.005 ≤ V_{OUT} ≤ 4.0 V	1000	10,000		V/mV
		R_L = 10 kΩ, −40°C ≤ T_A ≤ +125°C	500			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1	5	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	R_L = 100 kΩ to GND	4.98	5.0		V
		R_L = 10 kΩ to GND	4.90	4.94		V
		I_{OUT} = 1 mA, −40°C ≤ T_A ≤ +125°C		4.7		V
Output Voltage Swing Low	V_{OL}	R_L = 100 kΩ to GND		0.7	2	mV
		R_L = 10 kΩ to GND		0.7	2	mV
		I_{OUT} = 1 mA, −40°C ≤ T_A ≤ +125°C		90		mV
Output Current	I_{OUT}		±11	±18		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	±1.5 V ≤ V_S ≤ ±15 V	90	110		dB
		±1.5 V ≤ V_S ≤ ±15 V, −40°C ≤ T_A ≤ +125°C	85			dB
Supply Current per Amplifier	I_{SY}	V_{OUT} = 2.5 V, R_L = ∞, −40°C ≤ T_A ≤ +125°C			150	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		0.03		V/µs
Gain Bandwidth Product	GBP			75		kHz
Phase Margin	θ_O			86		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		1.5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		51		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		<0.1		pA/√Hz

V_S = 3.0 V, V_{CM} = 1.5 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			100	500	µV
Input Bias Current	I_B			8	20	nA
Input Offset Current	I_{OS}			±1	±3	nA
Input Voltage Range	V_{CM}		0		2.0	V
Common-Mode Rejection Ration	CMRR	0 V ≤ V_{CM} ≤ 2.0 V, −40°C ≤ T_A ≤ +125°C	90	110		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ		750		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1		µV/°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	R_L = 10 kΩ to GND	2.9			V
Output Voltage Swing Low	V_{OL}	R_L = 10 kΩ to GND		0.7	2	mV
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	±1.5 V ≤ V_S ≤ ±15 V	90	110		dB
		±1.5 V ≤ V_S ≤ ±15 V, −40°C ≤ T_A ≤ +125°C	85			dB
Supply Current per Amplifier	I_{SY}	V_{OUT} = 1.5 V, R_L = ∞, −40°C ≤ T_A ≤ +125°C			150	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		0.03		V/µs
Gain Bandwidth Product	GBP			75		kHz
Phase Margin	θ_O			85		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		1.6		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		53		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		<0.1		pA/√Hz

V_S = ±15.0 V, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			300	500	µV
		−40°C ≤ T_A ≤ +125°C			800	µV
Input Bias Current	I_B	V_{CM} = 0 V		7	20	nA
		V_{CM} = 0 V, −40°C ≤ T_A ≤ +125°C			30	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V		±1	±3	nA
		V_{CM} = 0 V, −40°C ≤ T_A ≤ +125°C			±5	nA
Input Voltage Range	V_{CM}		−15		+13.5	V
Common-Mode Rejection Ratio	CMRR	−15.0 V ≤ V_{CM} ≤ +13.5 V, −40°C ≤ T_A ≤ +125°C	90	110		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ	1000	4000		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	R_L = 100 kΩ to GND	14.95			V
		R_L = 10 kΩ to GND	14.80			V
Output Voltage Swing Low	V_{OL}	R_L = 100 kΩ to GND			−14.95	V
		R_L = 10 kΩ to GND			−14.85	V
Output Current	I_{OUT}		±15	±25		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±1.5 V to ±15 V	90	110		dB
		V_S = ±1.5 V to ±15 V, −40°C ≤ T_A ≤ +125°C	85			dB
Supply Current per Amplifier	I_{SY}	V_O = 0 V, R_L = ∞, V_S = ±18 V, −40°C ≤ T_A ≤ +125°C			175	µA
Supply Voltage Range	V_S		3 (± 1.5)		36 (± 18)	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		0.03		V/µs
Gain Bandwidth Product	GBP			85		kHz
Phase Margin	θ_O			83		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		1.25		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		45		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		<0.1		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter[1]	Rating
Supply Voltage	±18 V
Input Voltage	±18 V
Differential Input Voltage[2]	36 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
P, S Packages	−65°C to +150°C
Operating Temperature Range	
OP295G, OP495G	−40°C to +125°C
Junction Temperature Range	
P, S Packages	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] Absolute maximum ratings apply to packaged parts, unless otherwise noted.
[2] For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for worst case mounting conditions; that is, θ_{JA} is specified for device in socket for PDIP; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.

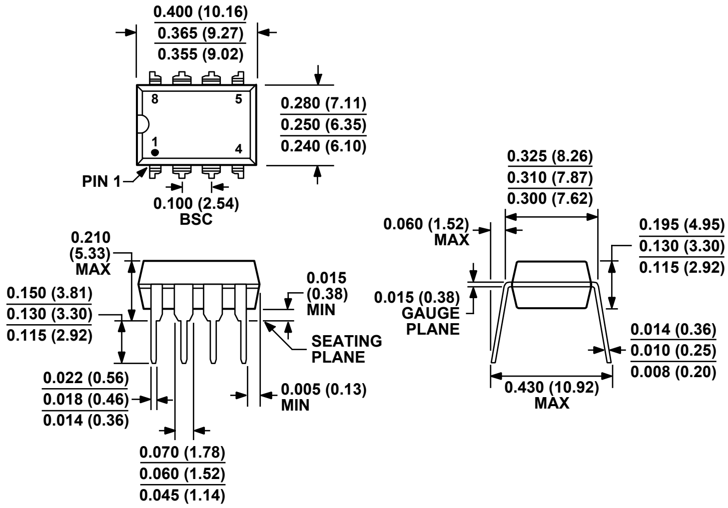
Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead PDIP (N-8)	103	43	°C/W
8-Lead SOIC_N (R-8)	158	43	°C/W
14-Lead PDIP (N-14)	83	39	°C/W
16-Lead SOIC_W (RW-16)	98	30	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

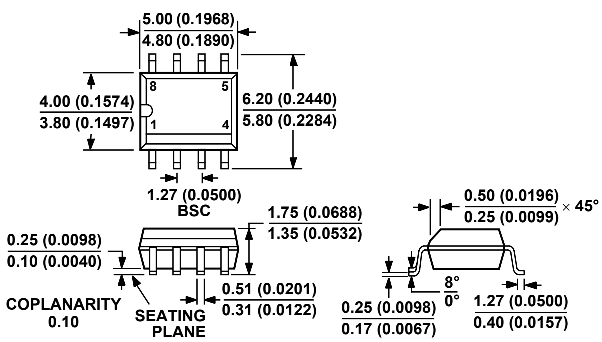
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001-BA

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 34. 8-Lead Plastic Dual In-Line Package [PDIP]
(N-8) P Suffix
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 35. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8) S Suffix
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP295GP	−40°C to +125°C	8-Lead PDIP	P-Suffix (N-8)
OP295GPZ[1]	−40°C to +125°C	8-Lead PDIP	P-Suffix (N-8)
OP295GS	−40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)
OP295GS-REEL	−40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)
OP295GS-REEL7	−40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)
OP295GSZ[1]	−40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)
OP295GSZ-REEL[1]	−40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)
OP295GSZ-REEL7[1]	−40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)
OP495GP	−40°C to +125°C	14-Lead PDIP	P-Suffix (N-14)
OP495GPZ[1]	−40°C to +125°C	14-Lead PDIP	P-Suffix (N-14)
OP495GS	−40°C to +125°C	16-Lead SOIC_W	S-Suffix (RW-16)
OP495GS-REEL	−40°C to +125°C	16-Lead SOIC_W	S-Suffix (RW-16)
OP495GSZ[1]	−40°C to +125°C	16-Lead SOIC_W	S-Suffix (RW-16)
OP495GSZ-REEL[1]	−40°C to +125°C	16-Lead SOIC_W	S-Suffix (RW-16)

[1] Z = RoHS Compliant Part.