Very Low Noise Quad Operational Amplifier

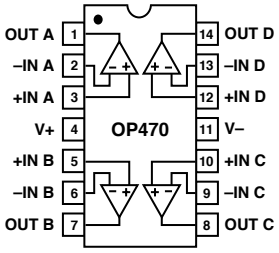
OP470

FEATURES

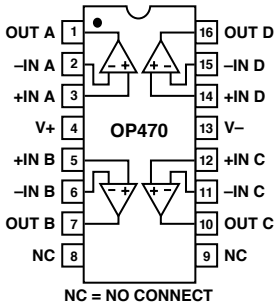
Very Low-Noise, 5 nV/√Hz @ 1 kHz Max
Excellent Input Offset Voltage, 0.4 mV Max
Low Offset Voltage Drift, 2 μV/°C Max
Very High Gain, 1000 V/mV Min
Outstanding CMR, 110 dB Min
Slew Rate, 2 V/μs Typ
Gain-Bandwidth Product, 6 MHz Typ
Industry Standard Quad Pinouts
Available in Die Form

PIN CONNECTIONS

14-Lead Hermetic DIP (Y-Suffix)
14-Lead Plastic DIP (P-Suffix)



16-Lead SOIC Package (S-Suffix)



GENERAL DESCRIPTION

The OP470 is a high-performance monolithic quad operational amplifier with exceptionally low voltage noise, 5 nV/√Hz at 1 kHz max, offering comparable performance to ADI's industry standard OP27.

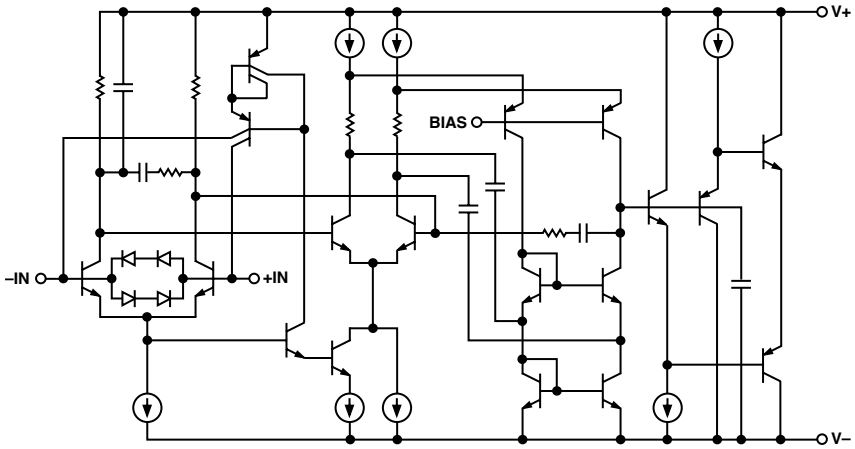
The OP470 features an input offset voltage below 0.4 mV, excellent for a quad op amp, and an offset drift under 2 μV/°C, guaranteed over the full military temperature range. Open loop gain of the OP470 is over 1,000,000 into a 10 kΩ load ensuring excellent gain accuracy and linearity, even in high gain applications. Input bias current is under 25 nA, which reduces errors due to signal source resistance. The OP470's CMR of over 110 dB and PSRR of less than 1.8 μV/V significantly reduce errors due to ground noise and power supply fluctuations. Power consumption of the quad OP470 is half that of four OP27s, a significant advantage for power conscious applications. The OP470 is unity-gain stable with a gain bandwidth product of 6 MHz and a slew rate of 2 V/μs.

The OP470 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low noise instrumentation amplifiers, quad buffers, and low noise active filters.

The OP470 conforms to the industry standard 14-lead DIP pinout. It is pin compatible with the LM148/149, HA4741, HA5104, and RM4156 quad op amps and can be used to upgrade systems using these devices.

For higher speed applications, the OP471, with a slew rate of 8 V/μs, is recommended.

SIMPLIFIED SCHEMATIC



OP470–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (at V_S = ±15 V, T_A = 25°C, unless otherwise noted.)

			OP470A/E			OP470F			OP470G			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT OFFSET VOLTAGE	V_{OS}			0.1	0.4		0.2	0.8		0.4	1.0	mV
INPUT OFFSET CURRENT	I_{OS}	V_{CM} = 0 V		3	10		6	20		12	30	nA
INPUT BIAS CURRENT	I_B	V_{CM} = 0 V		6	25		15	50		25	60	nA
INPUT NOISE VOLTAGE	e_{np-p}	0.1 Hz to 10 Hz (Note 1)		80	200		80	200		80	200	nV p-p
INPUT NOISE Voltage Density	e_n	f_O = 10 Hz f_O = 100 Hz f_O = 1 kHz (Note 2)		3.8 3.3 3.2	6.5 5.5 5.0		3.8 3.3 3.2	6.5 5.5 5.0		3.8 3.3 3.2	6.5 5.5 5.0	nV$\sqrt{Hz}$
INPUT NOISE Current Density	i_n	f_O = 10 Hz f_O = 100 Hz f_O = 1 kHz		1.7 0.7 0.4			1.7 0.7 0.4			1.7 0 7 0.4		pA$\sqrt{Hz}$
LARGE-SIGNAL Voltage Gain	A_{VO}	V = ±10 V R_L = 10 kΩ R_L = 2 kΩ	 1000 500	 2300 1200		 800 400	 1700 900		 800 400	 1700 900		V/mV
INPUT VOLTAGE RANGE	IVR	(Note 3)	±11	±12		±11	±12		±11	±12		V
OUTPUT VOLTAGE SWING	V_O	$R_L \geq 2$ kΩ	±12	±13		±12	±13		±12	±13		V
COMMON-MODE REJECTION	CMR	V_{CM} = ±11 V	110	125		100	120		100	120		dB
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±4.5 V to ±18 V		0.56	1.8		1.0	5.6		1.0	5.6	µV/V
SLEW RATE	SR		1.4	2		1.4	2		1.4	2		V/µs
SUPPLY CURRENT (All Amplifiers)	I_{SY}	No Load		9	11		9	11		9	11	mA
GAIN BANDWIDTH PRODUCT	GBW	A_V = 10		6			6			6		MHz
CHANNEL SEPARATION	CS	V_O = 20 V p-p f_O = 10 Hz (Note 1)	125	155		125	155		125	155		dB
INPUT CAPACITANCE	C_{IN}			2			2			2		pF
INPUT RESISTANCE Differential-Mode	R_{IN}			0.4			0.4			0.4		MΩ
INPUT RESISTANCE Common-Mode	R_{INCM}			11			11			11		GΩ
SETTLING TIME	t_S	A_V = 1 to 0.1% to 0.01 %		 5.5 6.0			 5.5 6.0			 5.5 6.0		µs

NOTES
[1]Guaranteed but not 100% tested
[2]Sample tested
[3]Guaranteed by CMR test

ELECTRICAL CHARACTERISTICS (at V_S = ±15 V, –55°C ≤ T_A ≤ 125°C for OP470A, unless otherwise noted.)

Parameter	Symbol	Conditions	OP470A Min	OP470A Typ	OP470A Max	Unit
INPUT OFFSET VOLTAGE	V_{OS}			0.14	0.6	mV
AVERAGE INPUT Offset Voltage Drift	TCV_{OS}			0.4	2	µV/°C
INPUT OFFSET CURRENT	I_{OS}	V_{CM} = 0 V		5	20	nA
INPUT BIAS CURRENT	I_B	V_{CM} = 0 V		15	20	nA
LARGE-SIGNAL Voltage Gain	A_{VO}	V_O = ±10 V R_L = 10 kΩ R_L = 2 kΩ	 750 400	 1600 800		V/mV
INPUT VOLTAGE RANGE*	IVR		±11	±12		V
OUTPUT VOLTAGE SWING	V_O	R_L ≥ 2 kΩ	±12	±13		V
COMMON-MODE REJECTION	CMR	V_{CM} = ±11 V	100	120		dB
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±4.5 V to ±18 V		1.0	5.6	µV/V
SUPPLY CURRENT (All Amplifiers)	I_{SY}	No Load	—	9.2	11	mA

*Guaranteed by CMR test

ELECTRICAL CHARACTERISTICS (at V_S = ±15 V, –25°C ≤ T_A ≤ 85°C for OP470E/OP470EF, –40°C ≤ T_A ≤ 85°C for OP470G, unless otherwise noted.)

Parameter	Symbol	Conditions	OP470E Min	OP470E Typ	OP470E Max	OP470F Min	OP470F Typ	OP470F Max	OP470G Min	OP470G Typ	OP470G Max	Unit
INPUT OFFSET VOLTAGE	V_{OS}			0.12	0.5		0.24	1.0		0.5	1.5	mV
AVERAGE INPUT Offset Voltage Drift	TCV_{OS}			0.4	2		0.6	4		2		µV/°C
INPUT OFFSET CURRENT	I_{OS}	V_{CM} = 0 V		4	20		7	40		20	50	nA
INPUT BIAS CURRENT	I_B	V_{CM} = 0 V		11	50		20	70		40	75	nA
LARGE-SIGNAL Voltage Gain	A_{VO}	V_O = ±10 V R_L = 10 kΩ R_L = 2 kΩ	 800 400	 1800 900		 600 300	 1400 700		 600 300	 1500 800		V/mV
INPUT VOLTAGE RANGE*	IVR		±11	±12		±11	±12		±11	±12		V
OUTPUT VOLTAGE SWING	V_O	R_L ≥ 2 kΩ	±12	±13		±12	±13		±12	±13		V
COMMON-MODE REJECTION	CMR	V_{CM} = ±11 V	100	120		90	115		90	110		dB
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±4.5 V to ±18 V		0.7	5.6		1.8	10		1.8	10	µV/V
SUPPLY CURRENT (All Amplifiers)	I_{SY}	No Load	—	9.2	11	—	9.2	11	—	9.3	11	mA

*Guaranteed by CMR test

OP470–SPECIFICATIONS

WAFER TEST LIMITS (at V_S = ±15 V, 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP470GBC Limit	Unit
INPUT OFFSET VOLTAGE	V_{OS}		0.8	mV Max
INPUT OFFSET CURRENT	I_{OS}	V_{CM} = 0 V	20	nA Max
INPUT BIAS CURRENT	I_B	V_{CM} = 0 V	50	nA Min
LARGE-SIGNAL Voltage Gain	A_{VO}	V_O = ±10 V R_L = 10 kΩ R_L = 2 kΩ	 800 400	V/mV Min
INPUT VOLTAGE RANGE*	IVR		±11	V Min
OUTPUT VOLTAGE SWING	V_O	$R_L \geq 2$ kΩ	±12	V Min
COMMON-MODE REJECTION	CMR	V_{CM} = ±11 V	100	dB
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±4.5 V to ±18 V	5.6	µV/V Max
SUPPLY CURRENT (All Amplifiers)	I_{SY}	No Load	11	mA Max

NOTE
*Guaranteed by CMR test

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Differential Input Voltage[2] . . . . . ±1.0 V
Differential Input Current[2] . . . . . ±25 mA
Input Voltage . . . . . Supply Voltage
Output Short-Circuit Duration . . . . . Continuous
Storage Temperature Range
P, Y Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C
Junction Temperature (T_j) . . . . . –65°C to +150°C
Operating Temperature Range
OP470A . . . . . –55°C to +125°C
OP470E, OP470F . . . . . –25°C to +85°C
OP470G . . . . . –40°C to +85°C

Package Type	θ_{JA}[3]	θ_{JC}	Unit
14-Lead Hermetic DIP(Y)	94	10	°C/W
14-Lead Plastic DIP(P)	76	33	°C/W
16-Lead SOIC (S)	88	23	°C/W

NOTES
[1]Absolute Maximum Ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]The OP470's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±1.0 V, the input current should be limited to ±25 mA.
[3]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, CerDIP, PDIP, packages; θ_{JA} is specified for device soldered to printed circuit board for SOIC packages.

ORDERING GUIDE

T_A = 25°C V_{OS} max (µV)	Package Options		Operating Temperature Range
	Cerdip 14-Pin	Plastic	
400			MIL
400	OP470AY*		MIL
400	OP470EY		IND
800	OP470FY*		IND
1000		OP470GP	XIND
1000		OP470GS	XIND

*Not for new design; obsolete April 2002.

For military processed devices, please refer to the standard Microcircuit Drawing (SMD) available at www.dscc.dla.mil/programs/milspec/default.asp

SMD Part Number	ADI Equivalent
59628856501CA	OP470AYMDA
596288565012A	OP470ARCMDA
596288565013A*	OP470ATCMDA

*Not for new designs; obsolete April 2002.

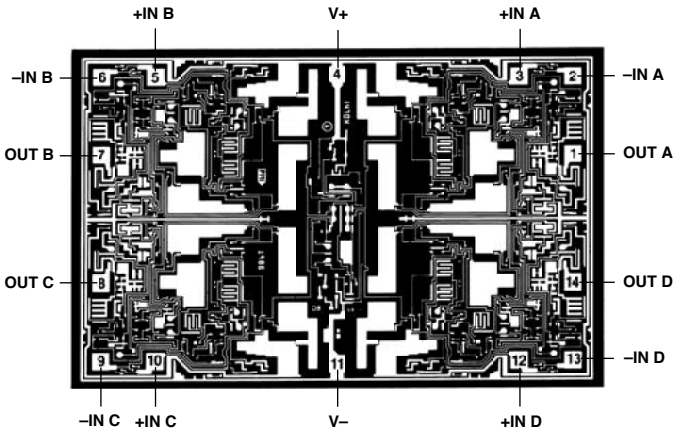


Figure 1. Dice Characteristics

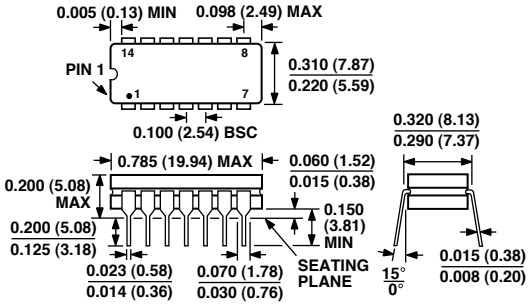
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP470 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

OUTLINE DIMENSIONS

14-Lead Ceramic Dip-Glass Hermetic Seal [CERDIP]
(Q-14)

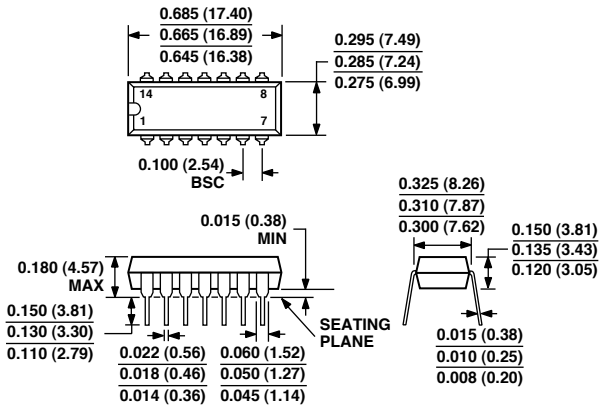
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

14-Lead Plastic Dual-in-Line Package [PDIP]
(N-14)

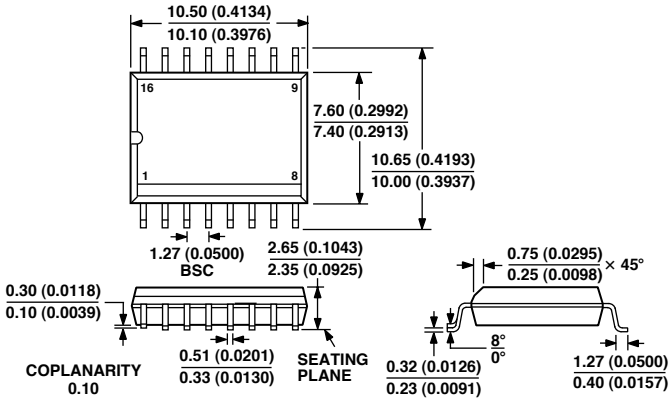
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-095-AB
CONTROLLING DIMENSIONS ARE IN INCH; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

16-Lead Standard Small Outline Package [SOIC]
Wide Body
(RW-16)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-013AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN