

FEATURES

- Low offset voltage:** 50 μV maximum
- Low offset voltage drift:** 0.6 $\mu\text{V}/^\circ\text{C}$ maximum
- Very low bias current:** 100 pA maximum
- Very high open-loop gain:** 2000 V/mV minimum
- Low supply current (per amplifier):** 625 μA maximum
- Operates from ± 2 V to ± 20 V supplies**
- High common-mode rejection:** 120 dB minimum

APPLICATIONS

- Strain gage and bridge amplifiers**
- High stability thermocouple amplifiers**
- Instrumentation amplifiers**
- Photocurrent monitors**
- High gain linearity amplifiers**
- Long-term integrators/filters**
- Sample-and-hold amplifiers**
- Peak detectors**
- Logarithmic amplifiers**
- Battery-powered systems**

GENERAL DESCRIPTION

The OP297 is the first dual op amp to pack precision performance into the space saving, industry-standard 8-lead SOIC package. The combination of precision with low power and extremely low input bias current makes the dual OP297 useful in a wide variety of applications.

Precision performance of the OP297 includes very low offset (less than 50 μV) and low drift (less than 0.6 $\mu\text{V}/^\circ\text{C}$). Open-loop gain exceeds 2000 V/mV, ensuring high linearity in every application.

Errors due to common-mode signals are eliminated by the common-mode rejection of over 120 dB, which minimizes offset voltage changes experienced in battery-powered systems. The supply current of the OP297 is under 625 μA .

The OP297 uses a super-beta input stage with bias current cancellation to maintain picoamp bias currents at all temperatures. This is in contrast to FET input op amps whose bias currents start in the picoamp range at 25°C, but double for every 10°C rise in temperature, to reach the nanoamp range above 85°C. Input bias current of the OP297 is under 100 pA at 25°C and is under 450 pA over the military temperature range per amplifier. This part can operate with supply voltages as low as ± 2 V.

PIN CONFIGURATION

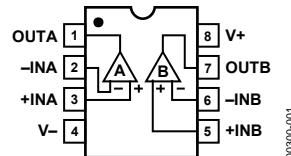


Figure 1.

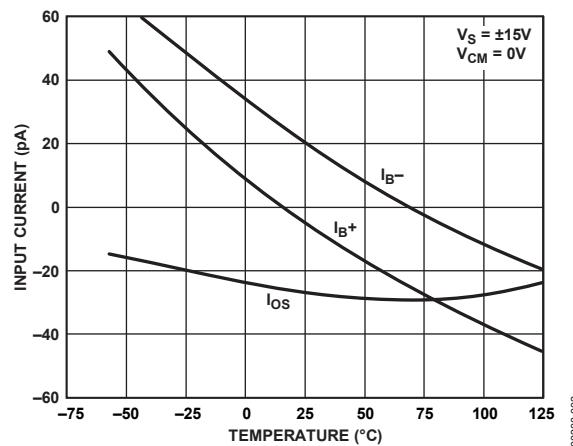


Figure 2. Low Bias Current over Temperature

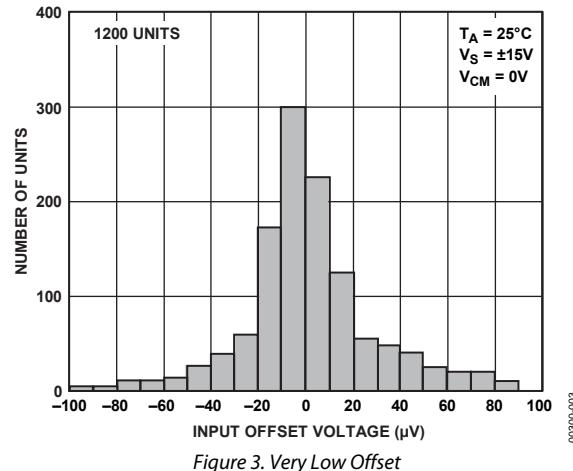


Figure 3. Very Low Offset

Combining precision, low power, and low bias current, the OP297 is ideal for a number of applications, including instrumentation amplifiers, log amplifiers, photodiode preamplifiers, and long term integrators. For a single device, see the [OP97](#); for a quad device, see the [OP497](#).

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

@ $V_S = \pm 15$ V, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	OP297E			OP297F			OP297G			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{os}		25	50		50	100		80	200		μV
Long-Term Input Voltage Stability			0.1			0.1			0.1			$\mu\text{V/month}$
Input Offset Current	I_{os}	$V_{CM} = 0$ V		20	100		35	150		50	200	pA
Input Bias Current	I_B	$V_{CM} = 0$ V		+20	± 100		+35	± 150		+50	± 200	pA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz		0.5			0.5			0.5		$\mu\text{V p-p}$
Input Noise Voltage Density	e_n	$f_{OUT} = 10$ Hz		20			20			20		nV/ $\sqrt{\text{Hz}}$
		$f_{OUT} = 1000$ Hz		17			17			17		nV/ $\sqrt{\text{Hz}}$
Input Noise Current Density	i_n	$f_{OUT} = 10$ Hz		20			20			20		fA/ $\sqrt{\text{Hz}}$
Input Resistance												
Differential Mode	R_{IN}			30			30			30		$M\Omega$
Common-Mode	R_{INCM}			500			500			500		$G\Omega$
Large Signal Voltage Gain	A_{vo}	$V_{OUT} = \pm 10$ V, $R_L = 2$ k Ω	2000	4000		1500	3200		1200	3200		V/mV
Input Voltage Range ¹	V_{CM}		± 13	± 14		± 13	± 14		± 13	± 14		V
Common-Mode Rejection	CMRR	$V_{CM} = \pm 13$ V	120	140		114	135		114	135		dB
Power Supply Rejection	PSRR	$V_S = \pm 2$ V to ± 20 V	120	130		114	125		114	125		dB
Output Voltage Swing	V_{OUT}	$R_L = 10$ k Ω	± 13	± 14		± 13	± 14		± 13	± 14		V
		$R_L = 2$ k Ω	± 13	± 13.7		± 13	± 13.7		± 13	± 13.7		V
Supply Current per Amplifier	I_{SY}	No load		525	625		525	625		525	625	μA
Supply Voltage	V_S	Operating range	± 2		± 20	± 2		± 20	± 2		± 20	V
Slew Rate	SR		0.05	0.15		0.05	0.15		0.05	0.15		V/ μs
Gain Bandwidth Product	GBWP	$Av = +1$		500			500			500		kHz
Channel Separation	CS	$V_{OUT} = 20$ V p-p, $f_{OUT} = 10$ Hz		150			150			150		dB
Input Capacitance	C_{IN}			3			3			3		pF

¹ Guaranteed by CMR test.

@ $V_S = \pm 15$ V, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	OP297E			OP297F			OP297G			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{os}			35	100		80	300		110	400	μV
Average Input Offset Voltage Drift	TCV_{os}			0.2	0.6		0.5	2.0		0.6	2.0	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	I_{os}	$V_{CM} = 0$ V		50	450		80	750		80	750	pA
Input Bias Current	I_B	$V_{CM} = 0$ V		+50	± 450		+80	± 750		+80	± 750	pA
Large Signal Voltage Gain	A_{vo}	$V_{OUT} = \pm 10$ V, $R_L = 2$ k Ω	1200	3200		1000	2500		800	2500		V/mV
Input Voltage Range ¹	V_{CM}		± 13	± 13.5		± 13	± 13.5		± 13	± 13.5		V
Common-Mode Rejection	CMRR	$V_{CM} = \pm 13$ V	114	130		108	130		108	130		dB
Power Supply Rejection	PSRR	$V_S = \pm 2.5$ V to ± 20 V	114			108			108			dB
Output Voltage Swing	V_{OUT}	$R_L = 10$ k Ω	± 13	± 13.4		± 13	± 13.4		± 13	± 13.4		V
Supply Current per Amplifier	I_{SY}	No load		550	750		550	750		550	750	μA
Supply Voltage	V_S	Operating range	± 2.5		± 20	± 2.5		± 20	± 2.5		± 20	V

¹ Guaranteed by CMR test.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	± 20 V
Input Voltage ¹	± 20 V
Differential Input Voltage ¹	40 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
Z-Suffix	-65°C to +175°C
P-Suffix, S-Suffix	-65°C to +150°C
Operating Temperature Range	
OP297E (Z-Suffix)	-40°C to +85°C
OP297F, OP297G (P-Suffix, S-Suffix)	-40°C to +85°C
Junction Temperature	
Z-Suffix	-65°C to +175°C
P-Suffix, S-Suffix	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

¹ For supply voltages less than ± 20 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for worst-case mounting conditions, that is, θ_{JA} is specified for device in socket for CERDIP and PDIP packages; θ_{JA} is specified for device soldered to printed circuit board for the SOIC package.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead CERDIP (Z-Suffix)	134	12	°C/W
8-Lead PDIP (P-Suffix)	96	37	°C/W
8-Lead SOIC (S-Suffix)	150	41	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

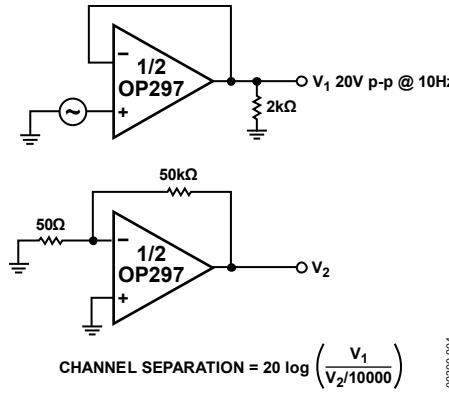
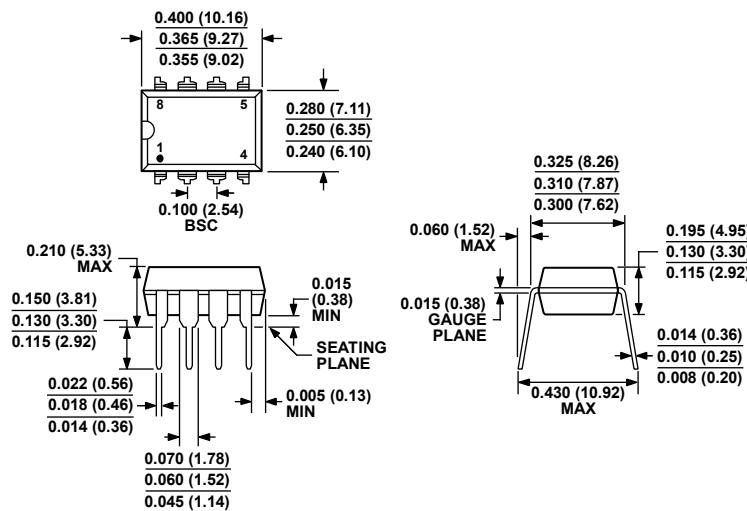


Figure 4. Channel Separation Test Circuit

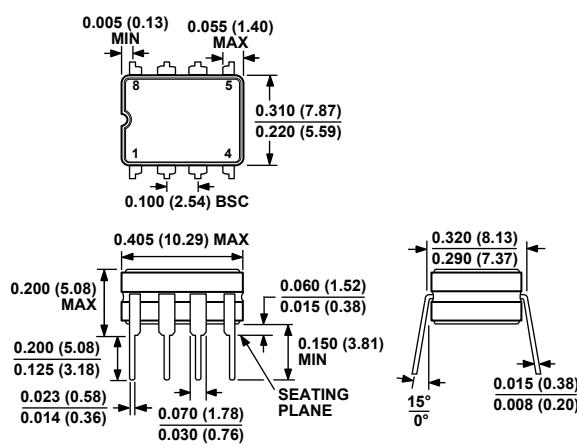
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
 CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

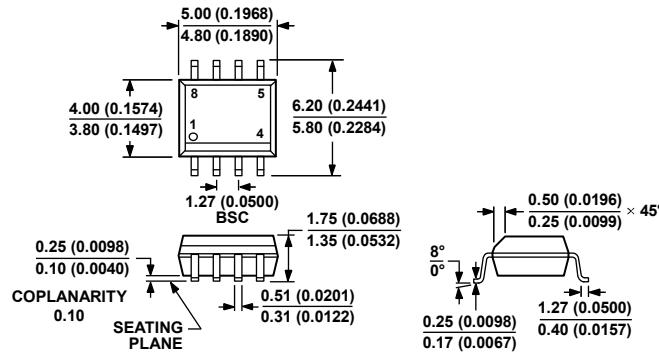
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Figure 37. 8-Lead Plastic Dual In-Line Package [PDIP]
P-Suffix (N-8)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
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Figure 38. 8-Lead Ceramic Dual In-Line Package [CERDIP]
Z-Suffix (Q-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA
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(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
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Figure 39. 8-Lead Standard Small Outline Package [SOIC_N]

Narrow Body

S-Suffix (R-8)

Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
OP297EZ	-40°C to +85°C	8-Lead CERDIP	Q-8 (Z-Suffix)
OP297FP	-40°C to +85°C	8-Lead PDIP	N-8 (P-Suffix)
OP297FPZ ¹	-40°C to +85°C	8-Lead PDIP	N-8 (P-Suffix)
OP297FS	-40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)
OP297FS-REEL	-40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)
OP297FS-REEL7	-40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)
OP297FSZ ¹	-40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)
OP297FSZ-REEL ¹	-40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)
OP297FSZ-REEL7 ¹	-40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)
OP297GP	-40°C to +85°C	8-Lead PDIP	N-8 (P-Suffix)
OP297GPZ ¹	-40°C to +85°C	8-Lead PDIP	N-8 (P-Suffix)
OP297GS	-40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)
OP297GS-REEL	-40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)
OP297GS-REEL7	-40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)
OP297GSZ ¹	-40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)
OP297GSZ-REEL ¹	-40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)
OP297GSZ-REEL7 ¹	-40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)

¹ Z = RoHS Compliant Part.