HCTL-2032
Quadrature Decoder IC

Description

The HCTL-2032 is CMOS ICs that perform the quadrature decoder, counter, and bus interface function. The HCTL-2032 is designed to improve system performance in digital closed loop motion control systems and digital data input systems. It does this by shifting time intensive quadrature decoder functions to a cost effective hardware solution. The HCTL-2032 consists of 4x/2x/1x-quadrature decoder, a binary up/down state counter, and an 8-bit bus interface. The HCTL-2032 has the dual-axis capability and index channel counter. The use of Schmitt-triggered CMOS inputs and input noise filters allows reliable operation in noisy environments. The HCTL-2032 contains 32-bit counter. It also contains quadrature decoder output signals and cascade signals for use with many standard computer ICs. The HCTL-2032 provides LSTLL compatible tri-state output buffers. Operation is specified for a temperature range from -40^{o}C to 100^{o}C at clock frequencies up to 33MHz.

Lifecycle status: Active

Request customization of this product

Lead (PB) Free
RoHS 6 fully compliant

Features

- Interfaces Encoder to Microprocessor
- 33 MHz Clock Operation
- Programmable Count ModesQuadrature (1x, 2x or 4x)
- Dual Axis Support
- Index Channel Support
- High Noise Immunity:Schmitt Trigger Inputs Digital Noise Filter
- 32-Bit Binary Up/Down Counter
- Latched Outputs
- 8-Bit Tristate Interface
- 8, 16, 24, or 32-Bit Operating Modes
- Quadrature Decoder Output Signals, Up/Down and Count
- Cascade Output Signals, Up/Down and Count
- Substantially Reduced System Software
- 5V Operation (VDD - VSS)
- TTL/CMOS Compatible I/O
- Operating Temperature: -40^{o}C to 100^{o}C

32-Pin PDIP, 32-Pin SOIC

Applications

Interface Quadrature Incremental Encoders to Microprocessors

Interface Digital Potentiometers to Digital Data Input Buses

Benefits

- 33 MHz Clock Operation -Typically operates between 2MHz and 33MHz allowing the flexibility of operation with a wide range of motor speeds

- Single or Dual Axis Support -One HCTL-2032 IC can support single or dual axes. Hence the benefits in terms of less components on board and cost savings are inevitable

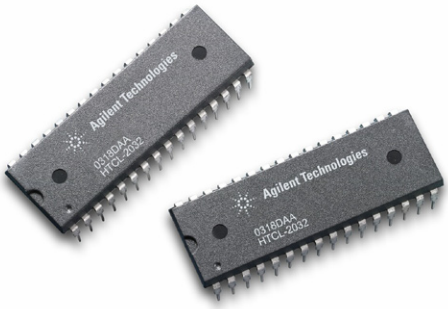
- 32-Bit Binary Up/Down Counter -The large counter allows the IC to operate without the support of extra memory. This feature reduces the number of supporting components needed on board and in turn is a cost saving.

- Operating Temperature: -40 degrees C to 100 degrees C-The wider operating temperature range makes the IC suitable for industrial automation operations which typically apply similar temperature ranges. This feature is not available in our existing products and also our direct competitors product range.

HCTL-2032, HCTL-2032-SC, HCTL-2032-SCT, HCTL-2022

Quadrature Decoder/ Counter Interface ICs

Data Sheet



Description

The HCTL-20XX-XX is CMOS ICs that perform the quadrature decoder, counter, and bus interface function. The HCTL-20XX-XX is designed to improve system performance in digital closed loop motion control systems and digital data input systems. It does this by shifting time intensive quadrature decoder functions to a cost effective hardware solution. The HCTL-20XX-XX consists of a quadrature decoder logic, a binary up/down state counter, and an 8-bit bus interface. The use of Schmitt-triggered CMOS inputs and input noise filters allows reliable operation in noisy environments. The HCTL-20XX-XX contains 32-bit counter and provides LSTLL compatible tri-state output buffers. Operation is specified for a temperature range from -40 to +100°C at clock frequencies up to 33MHz.

The HCTL-2032 and HCTL-2032-SC have dual-axis capability and index channel support. Both devices can be programmed as 4x/2x/1x count mode. The HCTL-2032 and HCTL2032-SC also provides quadrature decoder output signals and cascade signals for use with many standard computer ICs.

The HCTL-2022 has most of the HCTL-2032 features, but it can only supports single axis and fixed at 4x count mode. The HCTL-2022 doesn't provide decoder output and cascade signals.

Features

- Interfaces Encoder to Microprocessor
- 33 MHz Clock Operation
- Programmable Count Modes (1x, 2x or 4x)
- Single or Dual Axis Support
- Index Channel Support
- High Noise Immunity:
- Schmitt Trigger Inputs and Digital Noise Filter
- 32-Bit Binary Up/Down Counter
- Latched Outputs
- 8-Bit Tristate Interface
- 8, 16, 24, or 32-Bit Operating Modes
- Quadrature Decoder Output Signals, Up/Down and Count
- Cascade Output Signals, Up/Down and Count
- Substantially Reduced System Software
- 5V Operation (V_{DD} - V_{SS})
- TTL/CMOS Compatible I/O
- Operating Temperature: -40°C to 100°C
- 32-Pin PDIP, 32-Pin SOIC, 20-Pin PDIP

Applications

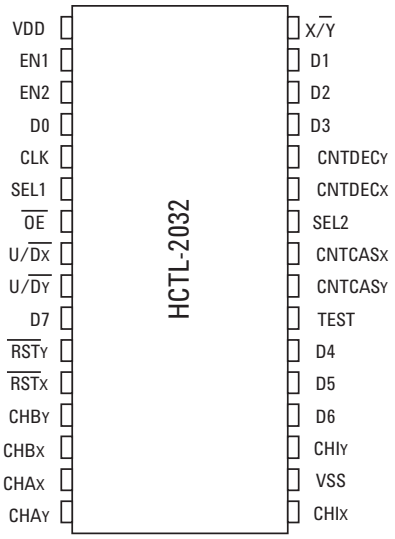
- Interface Quadrature Incremental Encoders to Microprocessors
- Interface Digital Potentiometers to Digital Data Input Buses

ESD WARNING: Standard CMOS handling precautions should be observed with the HCTL-2032 family ICs.

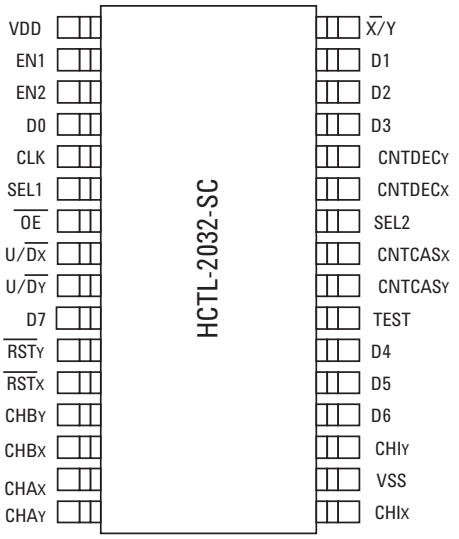
Devices

Part Number	Description	Package Drawing
HCTL-2032	32-bit counter, dual axis, decoder and cascade outputs, index channel support, programmable count modes, and 33 Mhz clock operation.	A
HCTL-2032-SC	All features of HCTL-2032.	B
HCTL-2022	Most of the HCTL-2032 features. The device supports single axis, and no decoder output and cascade signals. The programmable count mode is set to 4x internally.	C

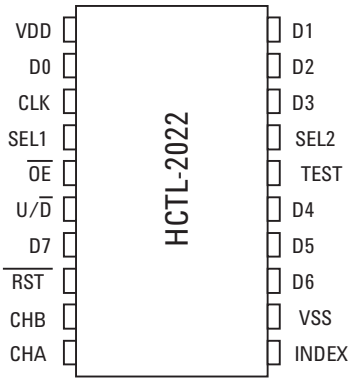
PINOUT A



PINOUT B

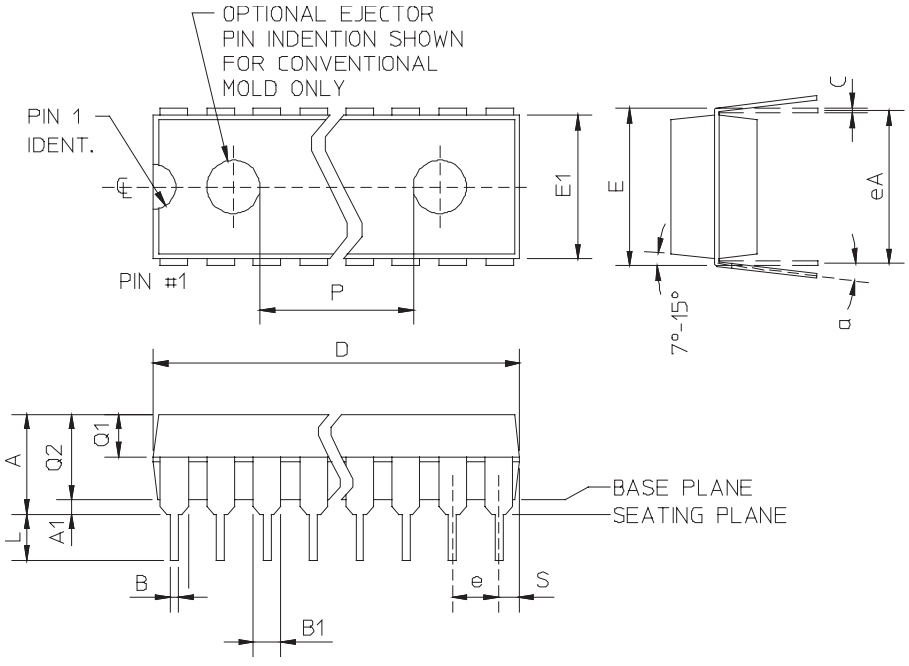


PINOUT C



Package Dimensions (dimensions in inches)

1) HCTL - 2032



SYMBOL	MIN.	NOM.	MAX.
A	-	-	-
A1	-	-	-
B	.016	.018	.020
B1	.045	.050	.055
C	-	.010	-
D	1.640	1.650	1.660
E	.590	.610	.630
E1	.546	.550	.554
e	.100 TYP		
eA	-		
L	.100	-	-
a	-	-	-
Q1	.066	.070	.074
Q2	-	-	-
S	-	-	-

Operating Characteristics

Table 1. Absolute Maximum Ratings

(All voltages below are referenced to V_{SS})

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	-0.3 to +6.0	V
Input Voltage	V_{IN}	-0.3 to (V_{DD} +0.3)	V
Storage Temperature	T_S	-55 to +150	°C
Operating Temperature [1]	T_A	-40 to +100	°C

Table 2. Recommended Operating Conditions

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	4.5 to 5.5	V
Ambient Temperature [1]	T_A	-40 to +100	°C

Table 3. DC Characteristics V_{DD} = 5V ± 5%; T_A = -40 to 100°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL} [2]	Low-Level Input Voltage				1.5	V
V_{IH} [2]	High-Level Input Voltage		3.5			V
V_{T+}	Schmitt-Trigger Positive-Going Threshold			3.5	4.0	V
V_{T-}	Schmitt-Trigger Negative-Going Threshold		1.0	1.5		V
V_H	Schmitt-Trigger Hysteresis		1.0	2.0		V
I_{IN}	Input Current	V_{IN}=V_{SS} or V_{DD}	-10	1	+10	µA
V_{OH} [2]	High-Level Output Voltage	I_{OH} = -3.75 mA	2.4	4.5		V
V_{OL} [2]	Low-Level Output Voltage	I_{OL} = +3.75mA		0.2	0.4	V
I_{OZ}	High-Z Output Leakage Current	V_O=V_{SS} or V_{DD}	-10	1	+10	µA
I_{DD}	Quiescent Supply Current	V_{IN}=Vss or V_{DD}		1	10	µA
C_{IN} [3]	Input Capacitance	Any Input		5		pF
C_{OUT} [3]	Output Capacitance	Any Output		5		pF

Notes

1. Free Air
2. In general, for any V_{DD} between the allowable limits (+4.5V to +5.5V), V_{IL} = 0.3V_{DD} and V_{IH} = 0.7V_{DD}; typical values are V_{OH} = V_{DD} - 0.5V and V_{OL} = V_{SS} + 0.2V
3. Including package capacitance

Switching Characteristics

Table 5. Switching Characteristics

Max/Min specifications at V_{DD} = 5V ± 5%; T_A = -40 to 100°C, C_L = 40 pf

Symbol		Description	Min.	Max.	Units
1	t_{CLK}	Clock Period		33	MHz
2	t_{CHH}	Pulse width, clock high	1/f		ns
3	t_{CD}	Delay time, rising edge of clock to valid, updated count information on D0-7		31	ns
4	t_{ODE}	Delay time, OEN fall to valid data		29	ns
5	t_{ODZ}	Delay time, OEN rise to Hi-Z state on D0-7		29	ns
6	t_{SDV}	Delay time, SEL0~SEL1 valid to stable, selected data byte (delay to High Byte = delay to Low Byte)		29	ns
7	t_{XNYDV}	Delay time, XNY valid to stable, selected data byte.		29	ns
8	t_{CLH}	Pulse width, clock low	15		ns
9	t_{SS}	Setup time, SEL1~SEL2 before clock fall	12		ns
10	t_{OS}	Setup time, OEN before clock fall	12		ns
11	t_{XNYS}	Setup time, XNY before clock fall	12		ns
12	t_{SH}	Hold time, SEL1~SEL2 after clock fall	0		ns
13	t_{OH}	Hold time, OEN after clock fall	0		ns
14	t_{XNYH}	Hold time, XNY after clock fall	0		ns
15	t_{RST}	Pulse width, RSTNX~RSTNY low	10		ns
16	t_{DCD}	Hold time, last position count stable on D0-7 after clock rise	2		ns
17	t_{DSD}	Hold time, last data byte stable after next SEL state change	2		ns
18	t_{DOD}	Hold time, data byte stable after OEN rise	2		ns
19	t_{DXNYD}	Hold time, data byte stable after XNY change	2		ns
20	t_{UDDX}	Delay time, U/DNX valid after clock rise	4	29	ns
21	t_{UDDY}	Delay time, U/DNY valid after clock rise	4	29	ns
22	t_{CHXD}	Delay time, CNTDECX or CNTCASX high after clock rise	4	31	ns
23	t_{CHYD}	Delay time, CNTDECY or CNTCASY high after clock rise	4	31	ns
24	t_{CLXD}	Delay time, CNTDECX or CNTCASX low after clock fall	4	31	ns
25	t_{CLYD}	Delay time, CNTDECY or CNTCASY low after clock fall	4	31	ns
26	t_{UDXH}	Hold time, U/DNX stable after clock rise	2		ns
27	t_{UDYH}	Hold time, U/DNY stable after clock rise	2		ns
28	t_{UDCXS}	Setup time, U/DNX valid before CNTDECX or CNTCASX rise	Note 1		ns
29	t_{UDCYS}	Setup time, U/DNY valid before CNTDECY or CNTCASY rise	Note 1		ns
30	t_{UDCXH}	Hold time, U/DNX stable after CNTDECX or CNTCASX rise	Note 2		ns
31	t_{UDCYH}	Hold time, U/DNY stable after CNTDECY or CNTCASY: rise	Note 2		ns

Notes
1. tclk - max delay (item 20/21) + min delay (item 22/23)
2. tclk - max delay (item 22/23) + min delay (item 20/21)