Dual Precision, Low Cost, High Speed BiFET Op Amp

AD712

FEATURES

- **Enhanced replacement for LF412 and TL082**
- **AC performance**
  - **Settles to ±0.01% in 1.0 µs**
  - **16 V/µs minimum slew rate (AD712J)**
  - **3 MHz minimum unity-gain bandwidth (AD712J)**
- **DC performance**
  - **200 V/mV minimum open-loop gain (AD712K)**
  - **Surface mount available in tape and reel in accordance with the EIA-481A standard**
  - **MIL-STD-883B parts available**
  - **Single version available: AD711**
  - **Quad version: AD713**
  - **Available in PDIP, SOIC_N, and CERDIP packages**

CONNECTION DIAGRAM

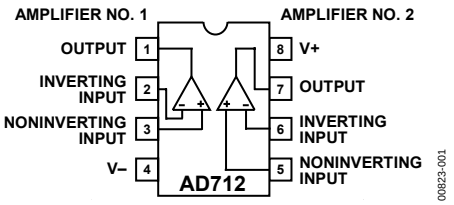


Figure 1. 8-Lead PDIP (N-Suffix), SOIC_N (R-Suffix), and CERDIP (Q-Suffix)

GENERAL DESCRIPTION

The AD712 is a high speed, precision, monolithic operational amplifier offering high performance at very modest prices. Its very low offset voltage and offset voltage drift are the results of advanced laser wafer trimming technology. These performance benefits allow the user to easily upgrade existing designs that use older precision BiFETs and, in many cases, bipolar op amps.

The superior ac and dc performance of this op amp makes it suitable for active filter applications. With a slew rate of 16 V/µs and a settling time of 1 µs to ±0.01%, the AD712 is ideal as a buffer for 12-bit digital-to-analog and analog-to-digital converters and as a high speed integrator. The settling time is unmatched by any similar IC amplifier.

The combination of excellent noise performance and low input current also make the AD712 useful for photo diode preamps. Common-mode rejection of 88 dB and open-loop gain of 400 V/mV ensure 12-bit performance even in high speed unity-gain buffer circuits.

The AD712 is pinned out in a standard op amp configuration and is available in seven performance grades. The AD712J and AD712K are rated over the commercial temperature range of 0°C to 70°C. The AD712A is rated over the industrial temperature range of −40°C to +85°C. The AD712S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available, specified over the commercial and industrial temperature ranges. PLUS screening includes 168-hour burn-in, in addition to other environmental and physical tests.

The AD712 is available in 8-lead PDIP, SOIC_N, and CERDIP packages.

PRODUCT HIGHLIGHTS

1. The AD712 offers excellent overall performance at very competitive prices.
2. The Analog Devices, Inc. advanced processing technology and 100% testing guarantee a low input offset voltage (3 mV maximum, J grade). Input offset voltage is specified in the warmed-up condition.
3. Together with precision dc performance, the AD712 offers excellent dynamic response. It settles to ±0.01% in 1 µs and has a minimum slew rate of 16 V/µs. Thus, this device is ideal for applications such as DAC and ADC buffers that require a combination of superior ac and dc performance.

SPECIFICATIONS

V_S = ±15 V @ T_A = 25°C, unless otherwise noted. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Table 1.

	AD712J/A/S			AD712K			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT OFFSET VOLTAGE[1]							
Initial Offset		0.3	**3/1/1**		0.2	**1.0**	mV
T_{MIN} to T_{MAX}			4/2/**2**			**2.0**	mV
vs. Temp		7	20/20/**20**		7	**10**	µV/°C
vs. Supply	**76**	95		**80**	100		dB
T_{MIN} to T_{MAX}	76/76/**76**			**80**			dB
Long-Term Offset Stability		15			15		µV/month
INPUT BIAS CURRENT[2]							
V_{CM} = 0 V		25	**75**		20	**75**	pA
V_{CM} = 0 V @ T_{MAX}		0.6/1.6/26	1.7/4.8/77		0.5	1.7	nA
V_{CM} = ±10 V			**100**			**100**	pA
INPUT OFFSET CURRENT							
V_{CM} = 0 V		10	**25**		5	**25**	pA
V_{CM} = 0 V @ T_{MAX}		0.3/0.7/11	0.6/1.6/26		0.1	0.6	nA
MATCHING CHARACTERISTICS							
Input Offset Voltage			**3/1/1**			**1.0**	mV
T_{MIN} to T_{MAX}			4/2/**2**			**2.0**	mV
Input Offset Voltage Drift			20/20/**20**			**10**	µV/°C
Input Bias Current			**25**			**25**	pA
Crosstalk							
@ f = 1 kHz		120			120		dB
@ f = 100 kHz		90			90		dB
FREQUENCY RESPONSE							
Small Signal Bandwidth	3.0	4.0		3.4	4.0		MHz
Full Power Response		200			200		kHz
Slew Rate	**16**	20		**18**	20		V/µs
Settling Time to 0.01%		1.0	1.2		1.0	1.2	µs
Total Harmonic Distortion		0.0003			0.0003		%
INPUT IMPEDANCE							
Differential		3×10^{12}||5.5			3×10^{12}||5.5		Ω||pF
Common Mode		3×10^{12}||5.5			3×10^{12}||5.5		Ω||pF
INPUT VOLTAGE RANGE							
Differential[3]		±20			±20		V
Common-Mode Voltage[4]		+14.5, −11.5			+14.5, −11.5		V
T_{MIN} to T_{MAX}	**$-V_S$ + 4**		**$+V_S$ − 2**	**$-V_S$ + 4**		**$+V_S$ − 2**	V
Common-Mode Rejection Ratio							
V_{CM} = ±10 V	**76**	88		**80**	88		dB
T_{MIN} to T_{MAX}	76/76/**76**	84		**80**	84		dB
V_{CM} = ±11 V	**70**	84		**76**	84		dB
T_{MIN} to T_{MAX}	70/70/**70**	80		**74**	80		dB
INPUT VOLTAGE NOISE		2			2		µV p-p
		45			45		nV/√Hz
		22			22		nV/√Hz
		18			18		nV/√Hz
		16			16		nV/√Hz

Parameter	AD712J/A/S Min	AD712J/A/S Typ	AD712J/A/S Max	AD712K Min	AD712K Typ	AD712K Max	Unit
INPUT CURRENT NOISE		0.01			0.01		pA/√Hz
OPEN-LOOP GAIN	**150**	400		**200**	400		V/mV
	100/100/**100**			**100**			V/mV
OUTPUT CHARACTERISTICS							
Voltage	**+13, −12.5**	+13.9, −13.3		**+13, −12.5**	+13.9, −13.3		V
	±12/±12/**±12**	+13.8, −13.1		**±12**	+13.8, −13.1		V
Current		+25			+25		mA
POWER SUPPLY							
Rated Performance		±15			±15		V
Operating Range	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current		+5.0	**+6.8**		+5.0	**+6.0**	mA

[1] Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = 25°C.
[2] Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = 25°C. For higher temperatures, the current doubles every 10°C.
[3] Defined as voltage between inputs, such that neither exceeds ±10 V from ground.
[4] Typically exceeding −14.1 V negative common-mode voltage on either input results in an output phase reversal.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Internal Power Dissipation[1]	
Input Voltage[2]	±18 V
Output Short-Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range	
Q-Suffix	−65°C to +150°C
N-Suffix and R-Suffix	−65°C to +125°C
Operating Temperature Range	
AD712J/K	0°C to 70°C
AD712A	−40°C to +85°C
AD712S	−55°C to +125°C
Lead Temperature Range (Soldering 60 sec)	300°C

[1] Thermal characteristics:
8-lead PDIP package: θ_{JA} = 165°C/W
8-lead CERDIP package: θ_{JC} = 22°C/W; θ_{JA} = 110°C/W
8-lead SOIC package: θ_{JA} = 100°C/W

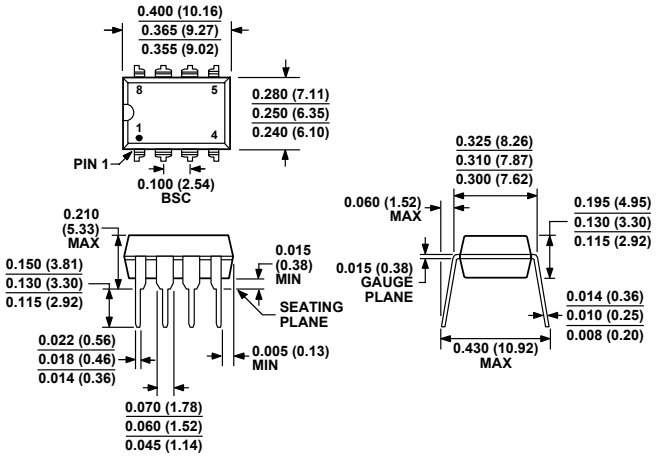
[2] For supply voltages less than ±18 V, the absolute maximum voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

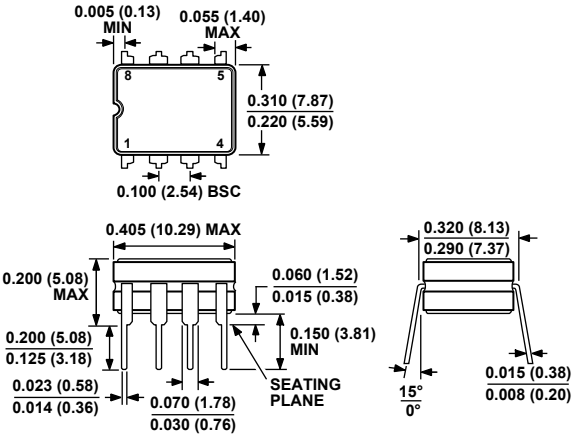
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

OUTLINE DIMENSIONS



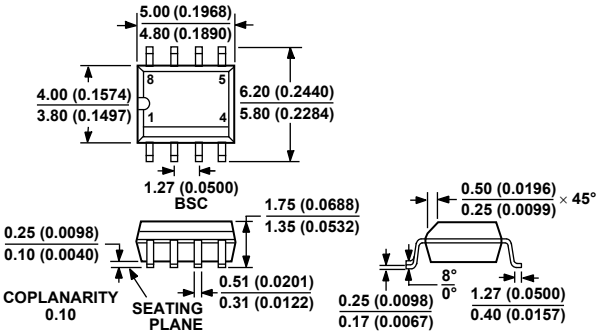
COMPLIANT TO JEDEC STANDARDS MS-001-BA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 53. 8-Lead Plastic Dual In-Line Package [PDIP]
(N-8)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 54. 8-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 55. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD712AQ	−40°C to +85°C	8-Lead CERDIP	Q-8
AD712JN	0°C to 70°C	8-Lead PDIP	N-8
AD712JNZ[1]	0°C to 70°C	8-Lead PDIP	N-8
AD712JR	0°C to 70°C	8-Lead SOIC_N	R-8
AD712JR-REEL	0°C to 70°C	8-Lead SOIC_N	R-8
AD712JR-REEL7	0°C to 70°C	8-Lead SOIC_N	R-8
AD712JRZ[1]	0°C to 70°C	8-Lead SOIC_N	R-8
AD712JRZ-REEL[1]	0°C to 70°C	8-Lead SOIC_N	R-8
AD712JRZ-REEL7[1]	0°C to 70°C	8-Lead SOIC_N	R-8
AD712KN	0°C to 70°C	8-Lead PDIP	N-8
AD712KNZ[1]	0°C to 70°C	8-Lead PDIP	N-8
AD712KR	0°C to 70°C	8-Lead SOIC_N	R-8
AD712KR-REEL	0°C to 70°C	8-Lead SOIC_N	R-8
AD712KR-REEL7	0°C to 70°C	8-Lead SOIC_N	R-8
AD712KRZ[1]	0°C to 70°C	8-Lead SOIC_N	R-8
AD712KRZ-REEL[1]	0°C to 70°C	8-Lead SOIC_N	R-8
AD712KRZ-REEL7[1]	0°C to 70°C	8-Lead SOIC_N	R-8
AD712SQ/883B	−55°C to +125°C	8-Lead CERDIP	Q-8

[1] Z = Pb-free part.