
Features

- Fast Read Access Time – 150 ns
- Automatic Page Write Operation
 - Internal Address and Data Latches for 64 Bytes
- Fast Write Cycle Times
 - Page Write Cycle Time: 10 ms Maximum (Standard)
2 ms Maximum (Option – Ref. AT28HC64BF Datasheet)
 - 1 to 64-byte Page Write Operation
- Low Power Dissipation
 - 40 mA Active Current
 - 100 μ A CMOS Standby Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling and Toggle Bit for End of Write Detection
- High Reliability CMOS Technology
 - Endurance: 100,000 Cycles
 - Data Retention: 10 Years
- Single 5V \pm 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-wide Pinout
- Industrial Temperature Ranges
- Green (Pb/Halide-free) Packaging Option

1. Description

The AT28C64B is a high-performance electrically-erasable and programmable read-only memory (EEPROM). Its 64K of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 220 mW. When the device is deselected, the CMOS standby current is less than 100 μ A.

The AT28C64B is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ POLLING of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

Atmel's AT28C64B has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.



**64K (8K x 8)
Parallel
EEPROM with
Page Write and
Software Data
Protection**

AT28C64B



5. DC and AC Operating Range

AT28C64B-15	
Operating Temperature (Case)	-40°C - 85°C
V _{CC} Power Supply	5V ±10%

6. Operating Modes

Mode	\overline{CE}	\overline{OE}	\overline{WE}	I/O
Read	V _{IL}	V _{IL}	V _{IH}	D _{OUT}
Write ⁽²⁾	V _{IL}	V _{IH}	V _{IL}	D _{IN}
Standby/Write Inhibit	V _{IH}	X ⁽¹⁾	X	High Z
Write Inhibit	X	X	V _{IH}	
Write Inhibit	X	V _{IL}	X	
Output Disable	X	V _{IH}	X	High Z
Chip Erase	V _{IL}	V _H ⁽³⁾	V _{IL}	High Z

- Notes:
1. X can be V_{IL} or V_{IH}.
 2. See "AC Write Waveforms" on page 8.
 3. V_H = 12.0V ±0.5V.

7. Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V _{CC} + 0.6V
Voltage on \overline{OE} and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

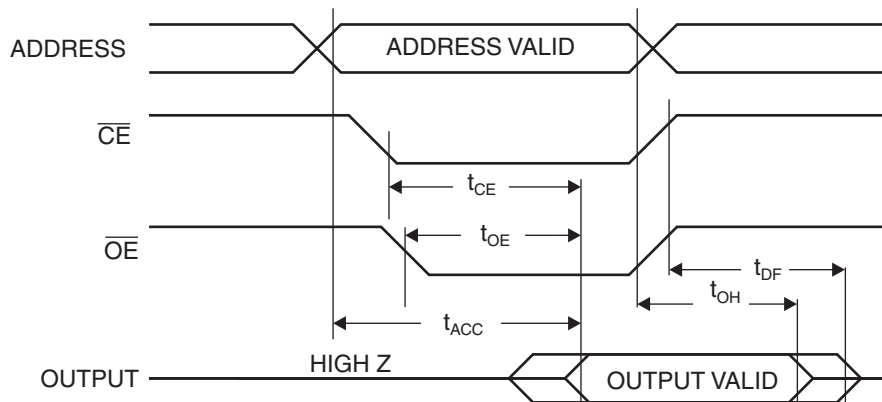
8. DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I _{LI}	Input Load Current	V _{IN} = 0V to V _{CC} + 1V		10	μA
I _{LO}	Output Leakage Current	V _{I/O} = 0V to V _{CC}		10	μA
I _{SB1}	V _{CC} Standby Current CMOS	\overline{CE} = V _{CC} - 0.3V to V _{CC} + 1V		100	μA
I _{SB2}	V _{CC} Standby Current TTL	\overline{CE} = 2.0V to V _{CC} + 1V		2	mA
I _{CC}	V _{CC} Active Current	f = 5 MHz; I _{OUT} = 0 mA		40	mA
V _{IL}	Input Low Voltage			0.8	V
V _{IH}	Input High Voltage		2.0		V
V _{OL}	Output Low Voltage	I _{OL} = 2.1 mA		0.40	V
V _{OH}	Output High Voltage	I _{OH} = -400 μA	2.4		V

9. AC Read Characteristics

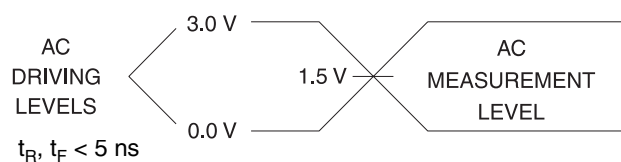
Symbol	Parameter	AT28C64B-15		Units
		Min	Max	
t_{ACC}	Address to Output Delay		150	ns
$t_{CE}^{(1)}$	\overline{CE} to Output Delay		150	ns
$t_{OE}^{(2)}$	\overline{OE} to Output Delay	0	70	ns
$t_{DF}^{(3)(4)}$	\overline{CE} or \overline{OE} to Output Float	0	50	ns
t_{OH}	Output Hold from \overline{OE} , \overline{CE} or Address, whichever occurred first	0		ns

10. AC Read Waveforms⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

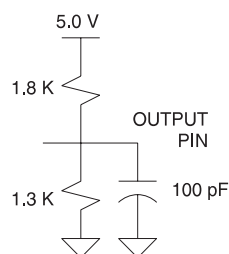


- Notes:
- \overline{CE} may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC} .
 - \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC} .
 - t_{DF} is specified from \overline{OE} or \overline{CE} whichever occurs first ($C_L = 5$ pF).
 - This parameter is characterized and is not 100% tested.

11. Input Test Waveforms and Measurement Level



12. Output Test Load



13. Pin Capacitance

$f = 1 \text{ MHz}, T = 25^\circ\text{C}^{(1)}$

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	$V_{IN} = 0V$
C_{OUT}	8	12	pF	$V_{OUT} = 0V$

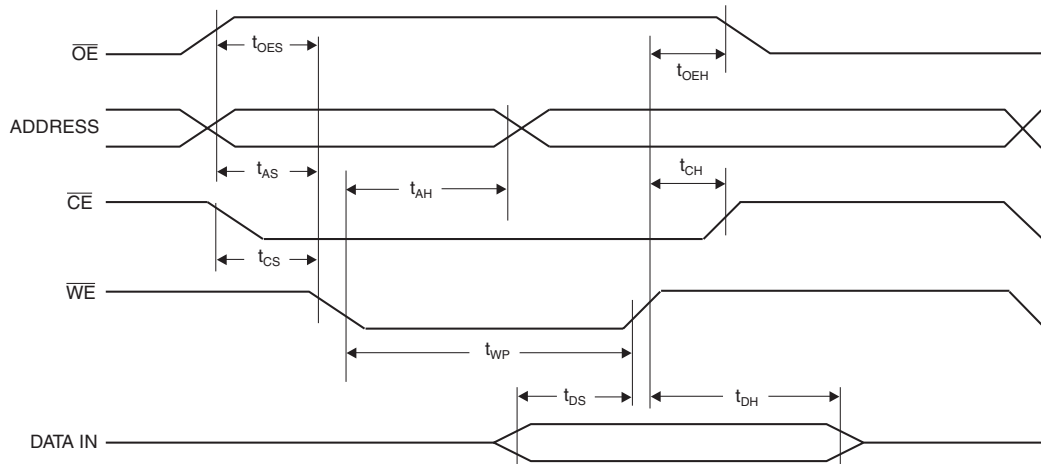
Note: 1. This parameter is characterized and is not 100% tested.

14. AC Write Characteristics

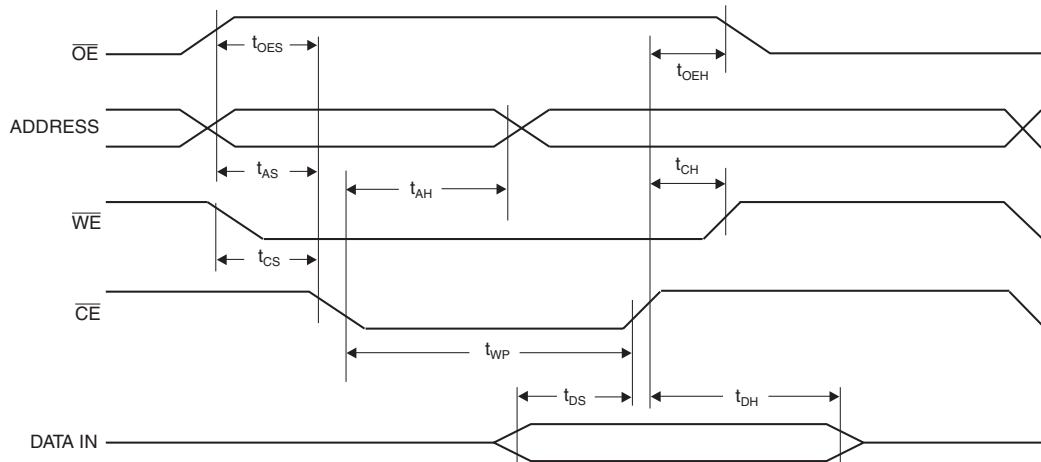
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, \overline{OE} Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Setup Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width (\overline{WE} or \overline{CE})	100		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}, t_{OEH}	Data, \overline{OE} Hold Time	0		ns

15. AC Write Waveforms

15.1 \overline{WE} Controlled



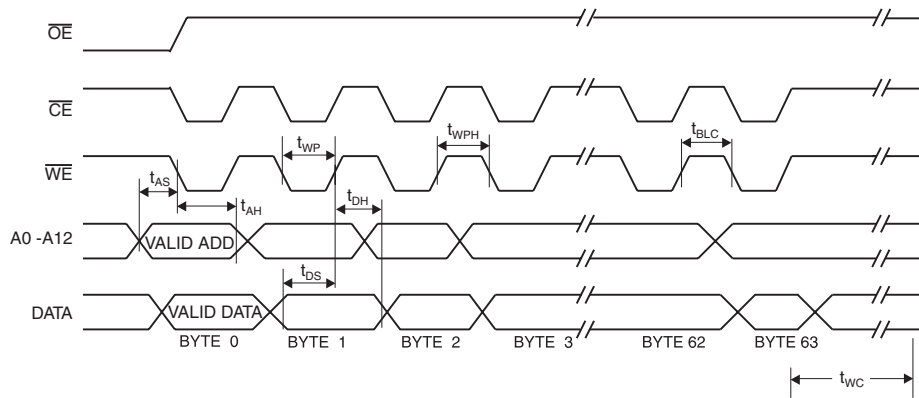
15.2 \overline{CE} Controlled



16. Page Mode Characteristics

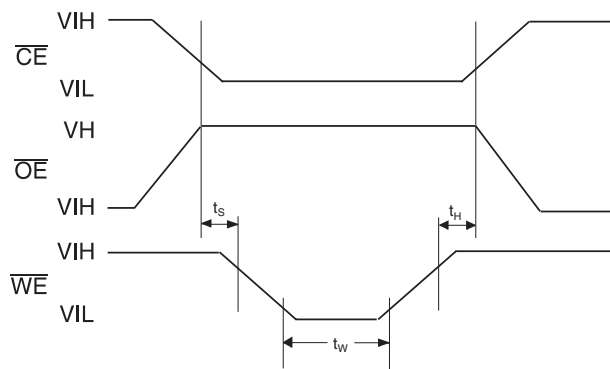
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{WC}	Write Cycle Time (option available – Ref. AT28HC64BF datasheet)		2	ms
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	μ s
t_{WPH}	Write Pulse Width High	50		ns

17. Page Mode Write Waveforms⁽¹⁾⁽²⁾



- Notes: 1. A6 through A12 must specify the same page address during each high to low transition of \overline{WE} (or \overline{CE}).
 2. \overline{OE} must be high only when \overline{WE} and \overline{CE} are both low.

18. Chip Erase Waveforms



$t_s = t_h = 1 \mu$ s (min.)
 $t_w = 10$ ms (min.)
 $V_H = 12.0V \pm 0.5V$

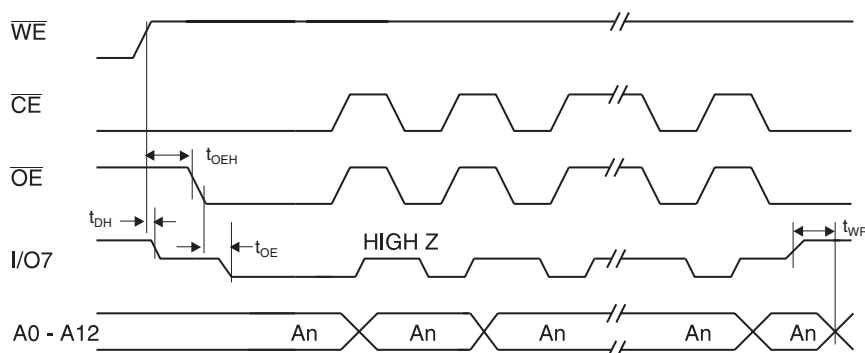


22. Data Polling Characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
$t_{OE\overline{H}}$	\overline{OE} Hold Time	0			ns
t_{OE}	\overline{OE} to Output Delay ⁽¹⁾				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested. See “AC Read Characteristics” on page 6.

23. Data Polling Waveforms



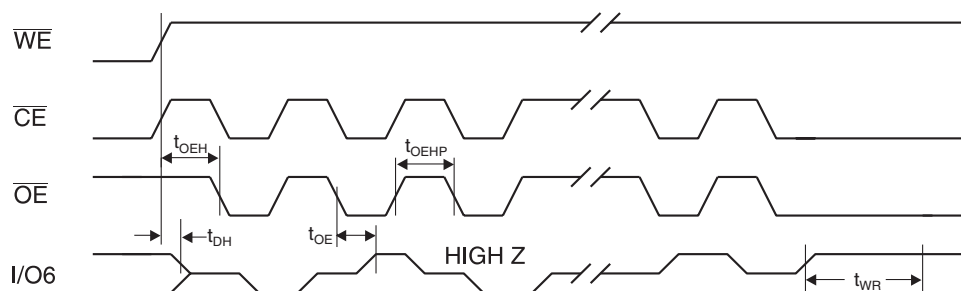
24. Toggle Bit Characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
$t_{OE\overline{H}}$	\overline{OE} Hold Time	10			ns
t_{OE}	\overline{OE} to Output Delay ⁽²⁾				ns
t_{OEHP}	\overline{OE} High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.

2. See “AC Read Characteristics” on page 6.

25. Toggle Bit Waveforms⁽¹⁾⁽²⁾⁽³⁾



Notes: 1. Toggling either \overline{OE} or \overline{CE} or both \overline{OE} and \overline{CE} will operate toggle bit.

2. Beginning and ending state of I/O6 will vary.

3. Any address location may be used but the address should not vary.

27. Ordering Information⁽¹⁾

27.1 Standard Package

t _{ACC} (ns)	I _{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	40	0.1	AT28C64B-15JI AT28C64B-15PI AT28C64B-15SI AT28C64B-15TI	32J 28P6 28S 28T	Industrial (-40° C to 85° C)

Note: 1. See "Valid Part Numbers" on page 13.

27.2 Green Package Option (Pb/Halide-free)

t _{ACC} (ns)	I _{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	40	0.1	AT28C64B-15JU AT28C64B-15SU AT28C64B-15TU AT28C64B-15PU	32J 28S 28T 28P6	Industrial (-40° C to 85° C)

28. Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C64B	15	JJ, JU, PI, SI, SU, TI, TU, PU

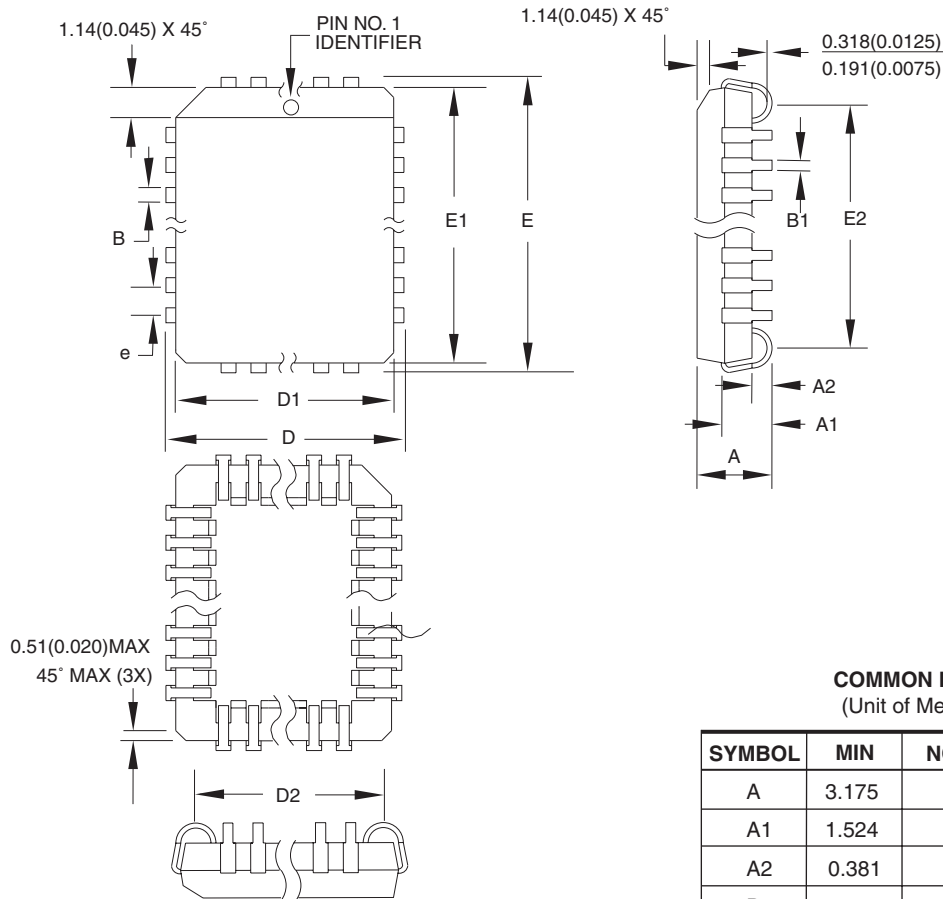
29. Die Products

Reference Section: Parallel EEPROM Die Products

Package Type	
32J	32-lead, Plastic J-leaded Chip Carrier (PLCC)
28P6	28-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28-lead, Plastic Thin Small Outline Package (TSOP)

30. Packaging Information

30.1 32J – PLCC



- Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
 3. Lead coplanarity is 0.004" (0.102 mm) maximum.



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San Jose, CA 95131

TITLE

32J, 32-lead, Plastic J-leaded Chip Carrier (PLCC)

DRAWING NO.

32J

REV.

B