LC²MOS Dual 12-Bit DACPORTs

AD7237A/AD7247A

FEATURES

Complete Dual 12-Bit DAC Comprising
- **Two 12-Bit CMOS DACs**
- **On-Chip Voltage Reference**
- **Output Amplifiers**
- **Reference Buffer Amplifiers**

Improved AD7237/AD7247:
- **12 V to 15 V Operation**
- **Faster Interface –30 ns typ Data Setup Time**

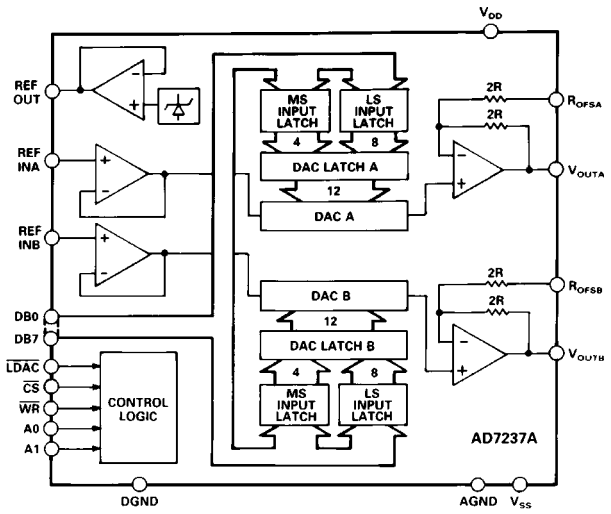
Parallel Loading Structure: AD7247A

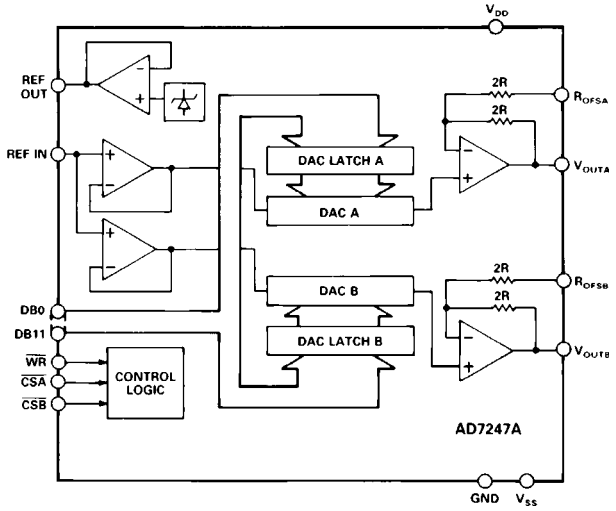
(8+4) Loading Structure: AD7237A

Single or Dual Supply Operation

Low Power—165 mW typ in Single Supply

FUNCTIONAL BLOCK DIAGRAMS





GENERAL DESCRIPTION

The AD7237A/AD7247A is an enhanced version of the industry standard AD7237/AD7247. Improvements include operation from 12 V to 15 V supplies, faster interface times and better reference variations with V_{DD}. Additional features include faster settling times.

The AD7237A/AD7247A is a complete, dual, 12-bit, voltage output digital-to-analog converter with output amplifiers and Zener voltage reference on a monolithic CMOS chip. No external user trims are required to achieve full specified performance.

Both parts are microprocessor compatible, with high speed data latches and interface logic. The AD7247A accepts 12-bit parallel data which is loaded into the respective DAC latch using the $\overline{WR}$ input and a separate Chip Select input for each DAC. The AD7237A has a double buffered interface structure and an 8-bit wide data bus with data loaded to the respective input latch in two write operations. An asynchronous $\overline{LDAC}$ signal on the AD7237A updates the DAC latches and analog outputs.

A REF OUT/REF IN function is provided which allows either the on-chip 5 V reference or an external reference to be used as a reference voltage for the part. For single supply operation, two output ranges of 0 V to +5 V and 0 V to +10 V are available, while these two ranges plus an additional ±5 V range are available with dual supplies. The output amplifiers are capable of developing +10 V across a 2 kΩ load to GND.

The AD7237A/AD7247A is fabricated in Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. Both parts are available in a 24-pin, 0.3" wide plastic and hermetic dual-in-line package (DIP) and are also packaged in a 24-lead small outline (SOIC) package.

PRODUCT HIGHLIGHTS

1. The AD7237A/AD7247A is a dual 12-bit DACPORT® on a single chip. This single chip design and small package size offer considerable space saving and increased reliability over multichip designs.
2. The improved interface times of the parts allow easy, direct interfacing to most modern microprocessors, whether they have 8-bit or 16-bit data bus structures.
3. The AD7237A/AD7247A features a wide power supply range allowing operation from 12 V supplies.

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REV. 0

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AD7237A/AD7247A–SPECIFICATIONS (V_{DD} = +12 V to +15 V,[1] V_{SS} = 0 V or –12 V to –15 V,[1] AGND = DGND = 0 V [AD7237A], GND = 0 V [AD7247A], REF IN = +5 V, R_L = 2 kΩ, C_L = 100 pF. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A[2]	B[2]	T[2]	Units	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	12	12	12	Bits	
Relative Accuracy[3]	±1	±1/2	±1/2	LSB max	
Differential Nonlinearity[3]	±0.9	±0.9	±0.9	LSB max	Guaranteed Monotonic
Unipolar Offset Error[3]	±3	±3	±4	LSB max	V_{SS} = 0 V or –12 V to –15 V[4]. DAC Latch Contents All 0s
Bipolar Zero Error[3]	±6	±4	±6	LSB max	V_{SS} = –12 V to –15 V[4]. DAC Latch Contents 1000 0000 0000
Full-Scale Error[3, 5]	±5	±5	±6	LSB max	
Full-Scale Mismatch[5]	±1	±1	±1	LSB typ	
REFERENCE OUTPUT					
REF OUT	4.97/5.03	4.97/5.03	4.95/5.05	V min/max	
Reference Temperature Coefficient	±25	±25	±25	ppm/°C typ	
Reference Load Change (ΔREF OUT vs. ΔI)	–1	–1	–1	mV max	Reference Load Current Change (0-100 μA)
REFERENCE INPUT					
Reference Input Range	4.75/5.25	4.75/5.25	4.75/5.25	V min/max	5 V ± 5%
Input Current[6]	±5	±5	±5	μA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	
Input Current I_{IN} (Data Inputs)	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance[6]	8	8	8	pF max	
ANALOG OUTPUTS					
Output Range Resistors	15/30	15/30	15/30	kΩ min/max	
Output Voltage Ranges[7]	+5, +10	+5, +10		V	Single Supply; (V_{SS} = 0 V)
Output Voltage Ranges[7]	+5, +10, ±5	+5, +10, ±5	+5, +10, ±5		Dual Supply; (V_{SS} = –12 V to –15 V[4])
DC Output Impedance	0.5	0.5	0.5	Ω typ	
AC CHARACTERISTICS[6]					
Voltage Output Settling Time					Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	8	8	10	μs max	DAC Latch all 0s to all 1s. Typically 5 μs
Negative Full-Scale Change	8	8	10	μs max	DAC Latch all 1s to all 0s. Typically 5 μs V_{SS} = –12 V to –15 V[4].
Digital-to-Analog Glitch Impulse[3]	30	30	30	nV secs typ	DAC Latch Contents Toggled Between all 0s and all 1s
Digital Feedthrough[3]	10	10	10	nV secs typ	
Digital Crosstalk[3]	30	30	30	nV secs typ	
POWER REQUIREMENTS					
V_{DD}	+10.8/+16.5	+11.4/+15.75	+11.4/+15.75	V min/max	For Specified Performance Unless Otherwise Stated
V_{SS}	–10.8/–16.5	–11.4/–15.75	–11.4/–15.75	V min/max	For Specified Performance Unless Otherwise Stated
I_{DD}	15	15	15	mA max	Output Unloaded. Typically 10 mA
I_{SS} (Dual Supplies)	5	5	5	mA max	Output Unloaded. Typically 3 mA

NOTES
[1]Power Supply tolerance is ±10% for A version and ±5% for B and T versions.
[2]Temperature ranges are as follows: A, B Versions, –40°C to +85°C; T Version, –55°C to +125°C.
[3]See Terminology.
[4]With appropriate power supply tolerances.
[5]Measured with respect to REF IN and includes unipolar/bipolar offset error.
[6]Sample tested @ +25°C to ensure compliance.
[7]0 V to +10 V range is only available with $V_{DD} \geq 14.25$ V.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +12 V to +15 V,[3] V_{SS} = 0 V or –12 V to –15 V,[3] AGND = DGND = 0 V [AD7237A], GND = 0 V [AD7247A])

Parameter	Limit at T_{MIN}, T_{MAX} (A, B Versions)	Limit at T_{MIN}, T_{MAX} (T Version)	Units	Conditions/Comments
t_1	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_3	80	100	ns min	$\overline{WR}$ Pulse Width
t_4	80	80	ns min	Data Valid to $\overline{WR}$ Setup Time
t_5[4]	10	10	ns min	Data Valid to $\overline{WR}$ Hold Time
t_6	0	0	ns min	Address to $\overline{WR}$ Setup Time
t_7	0	0	ns min	Address to $\overline{WR}$ Hold Time
t_8[5]	80	100	ns min	$\overline{LDAC}$ Pulse Width

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figures 5 and 7.
[3]Power Supply tolerance is ±10% for A version and ±5% for B and T versions.
[4]If 0 ns < t_2 < 10 ns, add t_2 to t_5. If $t_2 \geq$ 10 ns, add 10 ns to t_5.
[5]AD7237A only.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND (AD7247A) . . . . . –0.3 V to +17 V
V_{DD} to AGND, DGND (AD7237A) . . . . . –0.3 V to +17 V
V_{DD} to V_{SS} . . . . . –0.3 V to +34 V
AGND to DGND (AD7237A) . . . . . –0.3 V, V_{DD} +0.3 V
V_{OUTA},[2] V_{OUTB}[2] to AGND (GND) . . V_{SS} –0.3 V to V_{DD} +0.3 V
REF OUT to AGND (GND) . . . . . 0 V to V_{DD}
REF IN to AGND (GND) . . . . . –0.3 V to V_{DD} +0.3 V
Digital Inputs to DGND (GND) . . . . . –0.3 V to V_{DD} +0.3 V
Operating Temperature Range
  Industrial (A, B Versions) . . . . . –40°C to +85°C
  Extended (T Version) . . . . . –55°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 1000 mW
Derates above +75°C by . . . . . 10 mW/°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Short-circuit current is typically 80 mA. The outputs may be shorted to voltages in this range provided the power dissipation of the package is not exceeded.

ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy (LSB)	Package Option[2]
AD7237AAN	–40°C to +85°C	±1 max	N-24
AD7237ABN	–40°C to +85°C	±1/2 max	N-24
AD7237AAR	–40°C to +85°C	±1 max	R-24
AD7237ABR	–40°C to +85°C	±1/2 max	R-24
AD7237ATQ	–55°C to +125°C	±1/2 max	Q-24
AD7247AAN	–40°C to +85°C	±1 max	N-24
AD7247ABN	–40°C to +85°C	±1/2 max	N-24
AD7247AAR	–40°C to +85°C	±1 max	R-24
AD7247ABR	–40°C to +85°C	±1/2 max	R-24
AD7247ATQ	–55°C to +125°C	±1/2 max	Q-24

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact local sales office for military data sheet and availability.
[2]N = Plastic DIP; Q = Cerdip; R = Small Outline (SOIC).

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7237A/AD7247A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD7237A PIN FUNCTION DESCRIPTION (DIP PIN NUMBERS)

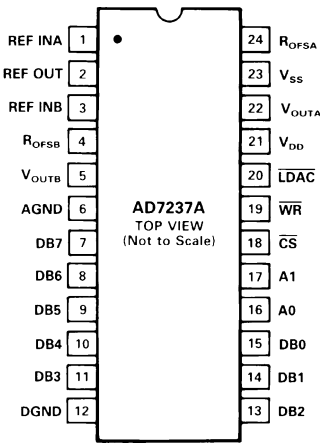
Pin	Mnemonic	Description
1	REF INA	Voltage Reference Input for DAC A. The reference voltage for DAC A is applied to this pin. It is internally buffered before being applied to the DAC. The nominal reference voltage for correct operation of the AD7237A is 5 V.
2	REF OUT	Voltage Reference Output. The internal 5 V analog reference is provided at this pin. To operate the part with internal reference, REF OUT should be connected to REF INA, REF INB.
3	REF INB	Voltage Reference Input for DAC B. The reference voltage for DAC B is applied to this pin. It is internally buffered before being applied to the DAC. The nominal reference voltage for correct operation of the AD7237A is 5 V.
4	R_{OFSB}	Output Offset Resistor for DAC B. This input configures the output ranges for DAC B. It is connected to V_{OUTB} for the +5 V range, to AGND for the +10 V range and to REF INB for the ±5 V range.
5	V_{OUTB}	Analog Output Voltage from DAC B. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 V to +5 V, 0 V to +10 V and ±5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
6	AGND	Analog Ground. Ground reference for DACs, reference and output buffer amplifiers.
7	DB7	Data Bit 7.
8-10	DB6-DB4	Data Bit 6 to Data Bit 4.
11	DB3	Data Bit 3/Data Bit 11 (MSB).
12	DGND	Digital Ground. Ground reference for digital circuitry.
13	DB2	Data Bit 2/Data Bit 10.
14	DB1	Data Bit 1/Data Bit 9.
15	DB0	Data Bit 0 (LSB)/Data Bit 8.
16	A0	Address Input. Least significant address input for input latches. A0 and A1 select which of the four input latches data is written to (see Table II).
17	A1	Address Input. Most significant address input for input latches.
18	$\overline{CS}$	Chip Select. Active low logic input. The device is selected when this input is active.
19	$\overline{WR}$	Write Input. $\overline{WR}$ is an active low logic input which is used in conjunction with $\overline{CS}$, A0 and A1 to write data to the input latches.
20	$\overline{LDAC}$	Load DAC. Logic input. A new word is loaded into the DAC latches from the respective input latches on the falling edge of this signal.
21	V_{DD}	Positive Supply (+12 V to +15 V).
22	V_{OUTA}	Analog Output Voltage from DAC A. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 V to +5 V, 0 V to +10 V and ±5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
23	V_{SS}	Negative Supply (0 V or –12 V to –15 V).
24	R_{OFSA}	Output Offset Resistor for DAC A. This input configures the output ranges for DAC A. It is connected to V_{OUTA} for the +5 V range, to AGND for the +10 V range and to REF INA for the ±5 V range.

AD7247A PIN FUNCTION DESCRIPTION (DIP PIN NUMBERS)

Pin	Mnemonic	Description
1	REF OUT	Voltage Reference Output. The internal 5 V analog reference is provided at this pin. To operate the part with internal reference, REF OUT should be connected to REF IN.
2	R_{OFSB}	Output Offset Resistor for DAC B. This input configures the output ranges for DAC B. It is connected to V_{OUTB} for the +5 V range, to GND for the +10 V range and to REF IN for the ±5 V range.
3	V_{OUTB}	Analog Output Voltage from DAC B. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 V to +5 V, 0 V to +10 V and ±5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
4	DB11	Data Bit 11 (MSB).
5	DB10	Data Bit 10.
6	GND	Ground. Ground reference for all on-chip circuitry.
7–15	DB9-DB1	Data Bit 9 to Data Bit 1.
16	DB0	Data Bit 0 (LSB).
17	$\overline{CSB}$	Chip Select Input for DAC B. Active low logic input. DAC B is selected when this input is active.
18	$\overline{CSA}$	Chip Select Input for DAC A. Active low logic input. DAC A is selected when this input is active.
19	$\overline{WR}$	Write Input. $\overline{WR}$ is an active low logic input which is used in conjunction with $\overline{CSA}$ and $\overline{CSB}$ to write data to the DAC latches.
20	V_{DD}	Positive Supply (+12 V to +15 V).
21	V_{OUTA}	Analog Output Voltage from DAC A. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 V to +5 V, 0 V to +10 V and ±5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
22	V_{SS}	Negative Supply (0 V or –12 V to –15 V).
23	R_{OFSA}	Output Offset Resistor for DAC A. This input configures the output ranges for DAC A. It is connected to V_{OUTA} for the +5 V range, to GND for the +10 V range and to REF IN for the ±5 V range.
24	REF IN	Voltage Reference Input. The common reference voltage for both DACs is applied to this pin. It is internally buffered before being applied to both DACs. The nominal reference voltage for correct operation of the AD7247A is 5 V.

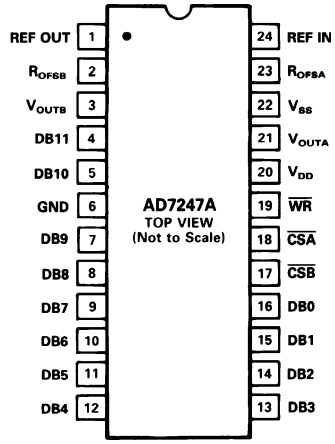
AD7237A PIN CONFIGURATION

DIP and SOIC



AD7247A PIN CONFIGURATION

DIP and SOIC



TERMINOLOGY

RELATIVE ACCURACY (LINEARITY)

Relative Accuracy, or endpoint linearity, is a measure of the maximum deviation of the DAC transfer function from a straight line passing through the endpoints of the transfer function. It is measured after allowing for zero and full-scale errors and is expressed in LSBs or as a percentage of full-scale reading.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB or less over the operating temperature range ensures monotonicity.

SINGLE SUPPLY LINEARITY AND GAIN ERROR

The output amplifiers of the AD7237A/AD7247A can have true negative offsets even when the part is operated from a single +12 V to +15 V supply. However, because the negative supply rail (V_{SS}) is 0 V, the output cannot actually go negative. Instead, when the output offset voltage is negative, the output voltage sits at 0 V, resulting in the transfer function shown in Figure 1. This "knee" is an offset effect, not a linearity error, and the transfer function would have followed the dotted line if the output voltage could have gone negative.

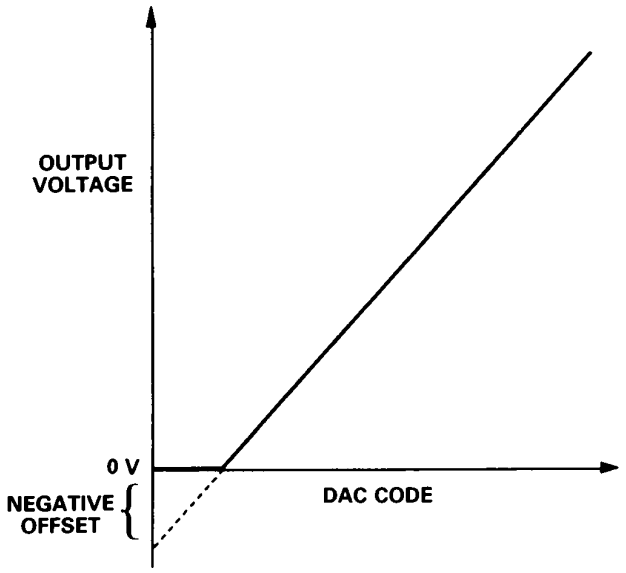


Figure 1. Effect of Negative Offset (Single Supply)

Normally, linearity is measured between zero (all 0s input code) and full scale (all 1s input code) after offset and full scale have been adjusted out or allowed for, but this is not possible in single supply operation if the offset is negative, due to the knee in the transfer function. Instead, linearity of the AD7237A/AD7247A in the unipolar mode is measured between full scale and the lowest code which is guaranteed to produce a positive output voltage. This code is calculated from the maximum specification for negative offset, i.e., linearity is measured between Codes 3 and 4095.

UNIPOLAR OFFSET ERROR

Unipolar Offset Error is the measured output voltage from V_{OUTA} or V_{OUTB} with all zeros loaded into the DAC latches when the DACs are configured for unipolar output. It is a combination of the offset errors of the DAC and output amplifier.

BIPOLAR ZERO ERROR

Bipolar Zero Error is the voltage measured at V_{OUTA} or V_{OUTB} when the DAC is connected in the bipolar mode and loaded with code 2048. It is due to a combination of offset errors in the DAC, amplifier offset and mismatch in the application resistors around the amplifier.

FULL-SCALE ERROR

Full-Scale Error is a measure of the output error when the amplifier output is at full scale (for the bipolar output range full scale is either positive or negative full scale). It is measured with respect to the reference input voltage and includes the offset errors.

DIGITAL FEEDTHROUGH

Digital Feedthrough is the glitch impulse injected for the digital inputs to the analog output when the data inputs change state, but the data in the DAC latches is not changed.

For the AD7237A it is measured with $\overline{\text{LDAC}}$ held high. For the AD7247A it is measured with $\overline{\text{CSA}}$ and $\overline{\text{CSB}}$ held high.

DIGITAL CROSSTALK

Digital crosstalk is the glitch impulse transferred to the output of one converter due to a change in digital code to the DAC latch of the other converter. It is specified in nV secs.

DIGITAL-TO-ANALOG GLITCH IMPULSE

This is the voltage spike that appears at the output of the DAC when the digital code changes before the output settles to its final value. The energy in the glitch is specified in nV secs and is measured for a 1 LSB change around the major carry transition (0111 1111 1111 to 1000 0000 0000).