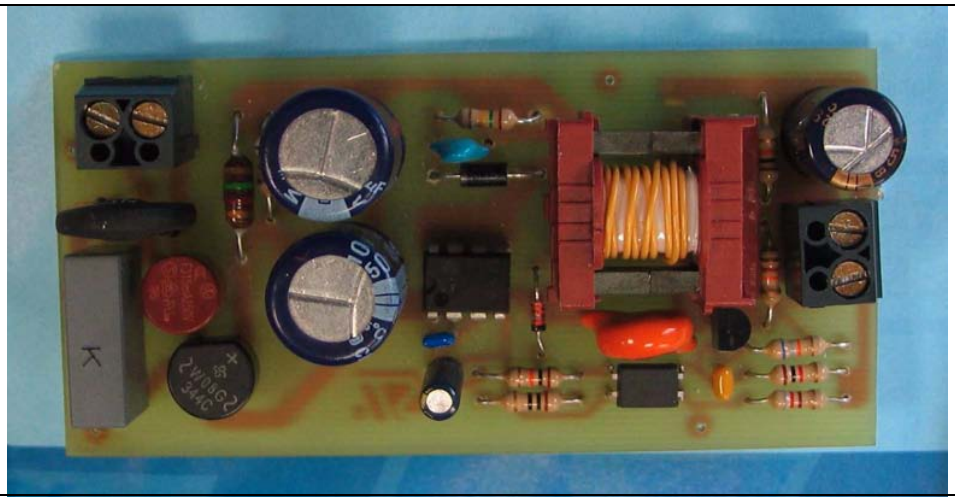
AN2272
Application Note

VIPer12A-based Low Power AC/DC Adapter

Introduction

This application note describes a low power, (output power of 4.1W) general purpose adapter which is able to handle a wide range input voltages ($88V_{AC}$ to $265V_{AC}$). The adapter (Order Code STEVAL-ISA011V1) is based on the Viper12A monolithic device that has the power switch as well as the basic control function needed to implement a current mode flyback converter.



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1 STEVAL-ISA011V1 Board Design

In order to improve regulation, the feedback loop is designed to have enough bandwidth so the converter can react on time to load changes. As is shown in the *Section 2.3: Dynamic Load Regulation Tests on page 20*, the board is able to handle high load step changes with very low variations in the output voltage.

The flyback converter is designed to work in Discontinuous Conduction Mode (DCM) in all operating conditions (i.e. Minimum Input Voltage, Maximum Load), because it provides better dynamic performance.

1.1 Primary Side

1.1.1 Step 1, Input Capacitor Selection

The first design step is to calculate the input capacitor value (C2a + C2b see *STEVAL-ISA011V Demo Board Schematic on page 30*). *Equation 1* is useful for this purpose:

Equation 1

$$C_{IN} = \frac{2 \cdot P_{IN} \cdot \Delta T}{V^2_{AC(min)pk} - V^2_{DC(min)}}$$

Where,

C_{IN} = input capacitor value,

P_{IN} = input power,

ΔT = the time between the two conduction cycles of the input bridge diodes,

$V_{AC(min)pk}$ = sinusoidal input waveform peaks (when AC voltage is at its minimum), and

$V_{DC(min)}$ = selected minimum input voltage required for the flyback (converter) stage.

In this case, the P_{IN} value used is calculated as P_O/η, where P_O is the maximum output power and η is the overall expected efficiency (70% in this example).

An acceptable value for $V_{DC(min)}$ is 80% of $V_{AC(min)pk}$:

Equation 2

$$V_{DC(min)} = 0.8V_{AC(min)pk} = \sqrt{2}V_{AC(min)}$$

ΔT is expressed as:

Equation 3

$$\Delta T = \frac{1}{2 \cdot \pi \cdot f_{line}} \cdot \left[\pi - \arccos\left(\frac{V_{DC(min)}}{V_{AC(min)pk}}\right)\right]$$

Where,

ΔT = the time between the two conduction cycles of the input bridge diodes, and

f_{line} = line frequency.

The calculated value of C_{IN} using *Equation 1* is 16µF. For the board, two capacitors (C2a and C2b, see *STEVAL-ISA011V Demo Board Schematic on page 30*) of 10µF were used. This means that C_{IN} = 20µF. This value was selected because the tolerance for an electrolytic capacitor is usually around 20%.

1.1.2 Step 2, Transformer Selection

The next step is selecting a transformer with a Primary Inductance (L_P) that allows the system to work at the boundary between Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). The worst case is minimum input voltage and full load. This value is expressed as:

Equation 4

$$L_{MAX} = \frac{(V_{DC(min)} \cdot D_{MAX})^2}{2 \cdot P_{IN} \cdot f_{SW}} \Rightarrow L_{MAX} = 3.5mH$$

Where,

L_{MAX} = maximum inductance for discontinuous mode operation,

$V_{DC(min)}$ = selected minimum input voltage required for the flyback (converter) stage,

D_{MAX} = maximum duty cycle,

P_{IN} = input power,

f_{SW} = switching frequency (internally fixed in the VIper12A to 60kHz), and

V_R = reflected voltage (fixed to 90V).

The D_{MAX} at the boundary between CCM and DCM is expressed as:

Equation 5

$$D_{MAX} = \frac{V_R}{V_{DC(min)} + V_R} \Rightarrow D_{MAX} = 0.47$$

The transformer selected for this application provides an L_P of 3mH, which is a little less than the maximum inductance (L_{MAX}) calculated in the first equation (3.5mH). This ensures that the system is not working at boundary and will always function in DCM.

Using the transformer's L_P, the designer can calculate the:

- Peak Primary Current, expressed as,

Equation 6

$$I_{PEAK} = \sqrt{\frac{2 \cdot P_{IN}}{f_{SW} \cdot L_P}} \Rightarrow I_{PEAK} = 258mA$$

Where,

I_{PEAK} = peak primary current,

P_{IN} = input power,

f_{SW} = switching frequency, and

L_P = primary inductance.

- actual Maximum Duty Cycle (D_{MAX}), expressed as,

Equation 7

$$D_{MAX} = \sqrt{\frac{2 \cdot P_{IN} \cdot f_{SW} \cdot L_P}{f_{SW} \cdot L_P}} \Rightarrow D_{MAX} = 0.42$$

and

- the primary side Root Mean Square (RMS) current value ($I_{PRMS(max)}$), which is the current that flows through the main switch and primary winding. It is expressed as:

Equation 8

$$I_{PRMS(max)} = I_{PEAK} \cdot \sqrt{\frac{D_{MAX}}{3}} \Rightarrow I_{PRMS(max)} = 97mA$$

Where,

$I_{PRMS(max)}$ = Primary Current root mean square,

The conduction losses in the main switch depend on the VIPer12A $I_{PRMS(max)}$ and ON resistance, and are expressed as:

Equation 9

$$P_{VIPer12A} = r_{ds(on)} \cdot I^2_{PRMS(max)}$$

Where,

$P_{VIPer12A}$ = VIPer12A conduction losses, and

$r_{ds(on)}$ = VIPer12A ON resistance.

1.2 Secondary Side

In order to select the output rectifier (secondary) diode D_{11}, the designer needs to know the maximum reverse voltage that the diode has to sustain, as well as the average and root mean square of the current flowing through it (see *STEVAL-ISA011V1 Schematic on page 30*). $V_{R(max)}$ is calculated as follows:

Equation 10

$$V_{R(max)} = V_{OUT} + \frac{V_{OUT}}{V_R} \cdot V_{DC(max)}$$

Where,

$V_{R(max)}$ = maximum reverse voltage,

V_{OUT} = output voltage,

V_R = reflected voltage, and

$V_{DC(max)}$ = selected maximum input voltage.

A commonly used selection method is to choose a diode with a 40% to 50% safety margin from the value given by the $V_{R(max)}$ calculation when a Schottky diode is used, or a safety margin of 20% to 30% if a standard “fast” diode is used. The safety margin prevents diode breakdown from oscillation caused by circuit parasitic elements (e.g. transformer secondary inductance leakage or parasitic diode capacitance) when the MOSFET is turned ON.

If the calculated $V_{R(max)}$ is 23V and a Schottky diode is used (adding a 50% safety margin), the D_{11} value is about 34V. This makes the STPS340U (with 40V breakdown voltage) an excellent choice for this application.

1.2.1 D_{11} Current and Power Dissipation

- The average current flowing through D_{11} is the output current while the I_{DRMS} value is expressed as:

Equation 11

$$I_{DRMS} = I_{PKS} \cdot \sqrt{\frac{D_{s\_cond}}{3}}$$

Where,

I_{DRMS} = current root mean square,

I_{PKS} = peak current at secondary winding, and

D_{s_cond} = conduction duty cycle of the secondary diode.

For one output flyback, I_{PKS} (peak current at the secondary winding) can be calculated as the primary peak current multiplied by the turns ratio.

Note: This formula applies only to DCM operation.

- D_{11} power dissipation is calculated as follows:

Equation 12

$$P_{lossD} = V_{dD} \cdot I_{D(avg)} + r_{dD} \cdot I^2_{DRMS}$$

Where,

P_{lossD} = diode power dissipation,

V_{dD} = drop voltage (when the diode is forward-biased),

$I_{D(avg)}$ = diode average current, and

r_{dD} = dynamic resistance.

Note: The formula and the correct values for V_{dD} and r_{dD} are in the diode datasheets.

1.2.2 Transformer Turns Ratio and D_{11} Peak Current

- The turns ratio that is selected for the transformer depends on the output voltage, the chosen reflected voltage, and the average voltage drop across the output diode.

  Keeping in mind the voltage drop across its dynamic resistance, $V_{DROP(avg)}$ is expressed as:

Equation 13

$$V_{DROP(avg)} = V_{dD} + r_{dD} \cdot I_O$$

Where,

$V_{DROP(avg)}$ = average voltage drop (across the output diode)

V_{dD} = drop voltage (when the diode is forward-biased),

r_{dD} = dynamic resistance,

I_O = diode output current, and

- Using the calculated $V_{DROP(avg)}$ value, the turns ratio is expressed as:

Equation 14

$$\frac{N_P}{N_S} = \frac{V_R}{V_O + V_{DROP(avg)}}$$

Where,

N_P = Primary Turns,

N_S = Secondary Turns,

V_R = reflected voltage, and

V_O = output voltage.

- Using the calculated turns ratio, I_{PKS} is then expressed as:

Equation 15

$$I_{PKS} = \frac{N_P}{N_S} \cdot I_{PKP}$$

Where,

I_{PKS} = peak current at secondary winding, and

I_{PKP} = peak power current

Note: The worst case (maximum power dissipation) will be in full load condition.

- The D_{11} conduction duty cycle is expressed as:

Equation 16

$$D_{s\_cond} = \frac{I_{PKP} \cdot L_P \cdot f_{SW}}{V_R}$$

Where,

D_{s_cond} = Secondary Diode conduction duty cycle,

L_P = primary inductance, and

f_{SW} = switching frequency.

1.2.3 C_{11} Output Capacitor Selection

The output capacitor selection (C_{11}, see *STEVAL-ISA011V1 Schematic on page 30*) depends on the output voltage ripple specification (ΔV_O = 300mV), and the ripple current rate of the capacitor itself. The output voltage ripple is mainly due to the Equivalent Series Resistor (ESR), so we have to select a capacitor with an ESR lower than the maximum allowed ESR value:

Equation 17

$$ESR_{MAX} = \frac{\Delta V_O}{I_{PKS}}$$

Where,

ESR_{MAX} = maximum allowed ESR rating,

ΔV_O = output voltage ripple, and

I_{PKS} = peak current at secondary winding.

The AC component of the current flowing through the output diode is also that of the current flowing through the capacitor. The C11 capacitor current rate has to be higher than the calculated current, which is expressed as:

Equation 18

$$I_{CAPRMS} = \sqrt{I^2_{DRMS} - I^2_O}$$

Where,

I_{CAPRMS} = capacitor current root mean square,

I_{DRMS} = diode current root mean square, and

I_O = output current.

The MBZ Type 1500 µF 10V by RUBYCON capacitor was selected for this application.

1.3 Completed Transformer Design

All of the calculations for the transformer design are complete. They include:

- Primary Inductance,
- Turns Ratio, and
- Winding Current Values (RMS, Average, and Peak).

Notes:

1. In order to prevent transformer saturation during the start-up phase, the current limit of the VIPer12A (I_{LIM} = 480mA, see datasheet for details) must be considered as the peak current.
2. For thermal limits (power dissipated in the magnetic core), the peak current (calculated in *Equation 6: on page 7*) must be used.
3. The RMS value of the current flowing through the windings is used first for calculating the power dissipated in the windings, then for winding size selection.

The transformer (reference number SRW16ES_E44H013) was designed and manufactured by TDK using aforementioned the data.

1.4 Feedback Loop

The transfer function 'control-to-output' for a flyback converter operating in DCM is given by the following formula:

Equation 19

$$\Delta V_O(s)/\Delta I_{FB}(s) = G_{fly} \cdot \frac{\left(1 + \frac{s}{z_{fly}}\right)}{\left(1 + \frac{s}{p_{fly}}\right)}$$

Where,

ΔV_O = output voltage ripple,

ΔI_{FB} = VIPer12A feedback pin current,

G_{fly} = flyback gain,

z_{fly} = flyback zero compensation reference,

p_{fly} = flyback pole reference, and

Using the VIPer12A input current (I_{FB}) to the feedback pin and G_{fly} values,

Equation 20

$$G_{fly} = \frac{V_O}{I_{PK}} \cdot G_{ID}$$

Where,

G_{fly} = flyback gain,

V_O = voltage output,

I_{PK} = primary peak current, and

G_{ID} = feedback current-to-drain current gain (see VIPer12A datasheet for details).

- The flyback pole value is expressed as:

Equation 21

$$p_{fly} = \frac{2}{C_{OUT} \cdot (R_L + 2 \cdot ESR_{OUT})}$$

Where,

p_{fly} = flyback pole reference,

C_{OUT} = output capacitor (see C_{11}, *STEVAL-ISA011V1 Schematic on page 30*),

R_L = inductor resistance, and

ESR_{OUT} = equivalent series resistor output.

- The flyback zero value (for two poles, one zero compensation network) is expressed as:

Equation 22

$$z_{fly} = \frac{1}{C_{OUT} \cdot ESR_{OUT}}$$

Where,

z_{fly} = flyback zero.

One pole is located at zero frequency in order to maximize the precision of the regulation. Compensation zero was used in order to compensate the p_{fly} and, typically, it has to be located between one-half and double the p_{fly} frequency. The last pole of the compensation network is used to compensate flyback zero due to the ESR.

- Loop Gain crossover frequency is the last calculation required to define the compensation network. In this design, the crossover frequency selected is as high as 2.5kHz to provide the converter with good bandwidth.

  The Transfer Function output control is expressed as:

Equation 23

$$\frac{\Delta I_{FB}(s)}{\Delta V_O(s)} = \frac{CTR}{R_6 \cdot R_8 \cdot C_8} \cdot \frac{(1 + s \cdot R_9 \cdot C_8)}{s \cdot (1 + s \cdot R_{FB} \cdot C_5)}$$

Where,

ΔI_{FB} = VIPer12A feedback pin current,

ΔV_O = output voltage ripple,

CTR = optocoupler Current Transfer Ratio

R_{FB} = VIPer12A feedback pin input impedance.

Note: Using these resistance and capacitance values as guidelines will provide the user with a stable loop as well as the required converter bandwidth.

2 STEVAL-ISA011V1 Board Tests

The tests performed with the STEVAL-ISA011V1 demo board are used to evaluate the converter behavior in terms of:

- efficiency,
- safe operating area of the devices,
- line regulation, and
- load regulation.

2.1 Start-up Tests

The diagnostic board will handle a wide range of AC input voltage ($88V_{AC}$ to $265V_{AC}$), and its maximum output power is 4.1W with one output of 4.5V. Its maximum output current is 900mA (see *Table 1*).

For flyback converters, the most critical conditions for the main switch in terms of Maximum Drain Current and of Maximum Drain Voltage (when no abnormal event occurs), are those that exist during the start-up phase. The maximum values for drain voltage and current are measured in both full load and no load conditions (the two extreme points in terms of load), and for minimum, maximum, and nominal input voltages (see *Table*).

All the measured values are within the rated maximum values of the VIPer12A so they are not critical for device operation.

Table 1. Electrical Characteristics

Symbol	Description	Limits or Value	Units
$V_{AC(max)}$	Maximum AC Input Voltage	$265V_{RMS}$	V
$V_{AC(min)}$	Minimum AC Input Voltage	$88V_{RMS}$	V
V_O	Output Voltage	4.5	V
ΔV_O	Maximum Output Voltage Ripple	300	mV
I_O	Maximum Output Current	900	mV
$\eta 230$	Efficiency (at full Load and $230V_{AC}$)	70	%
$\eta 115$	Efficiency (at full Load and $115V_{AC}$)	70	%

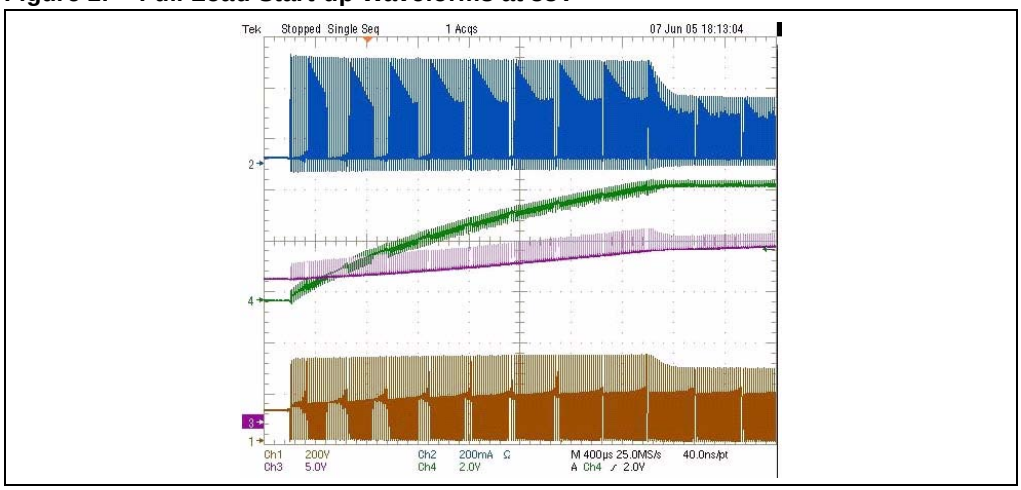
Table 2. Start up Measures

V_{INAC} (V_{RMS})	$V_{DRAIN(max)}$ (V)		$I_{DRAIN(max)}$ (mA)	
	Full load	No load	Full load	No load
88	352	353	0.460	0.458
115	393	401	0.472	0.470
230	581	581	0.507	0.505
265	638	633	0.515	0.515

2.1.1 Full Load Start-up Waveforms

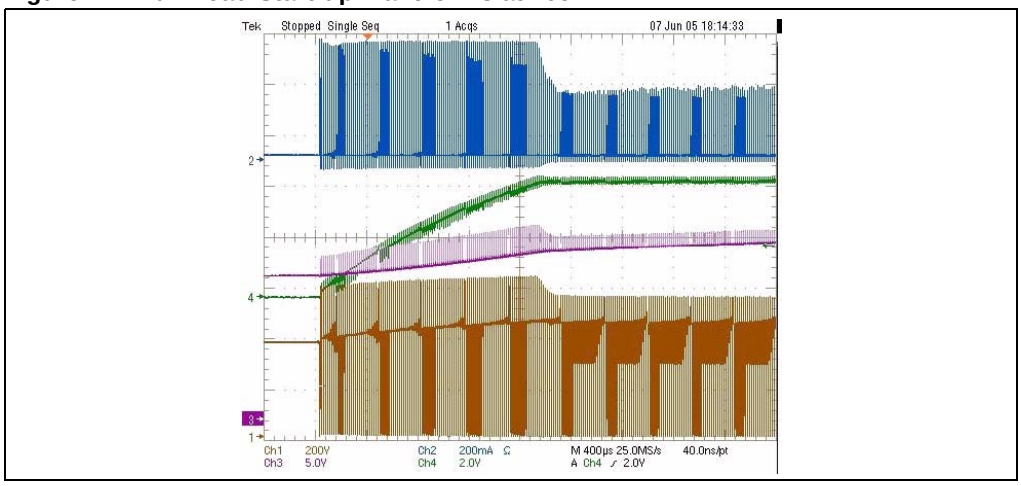
Figure 1, *Figure 2*, *Figure 3*, and *Figure 4 on page 17* show the most pertinent waveforms that occur during the circuit start-up phase when it is in Full Load condition, for the minimum ($88V_{AC}$), maximum ($265V_{AC}$), and nominal voltages ($115V_{AC}$ and $230V_{AC}$).

Figure 1. Full Load Start-up Waveforms at 88V



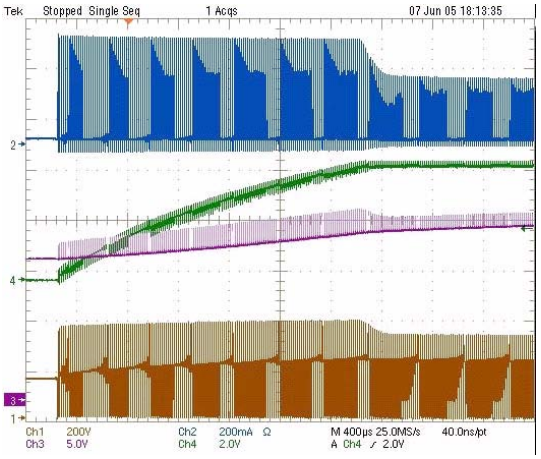
Notes: Cyan/Blue (Ch2) = drain current,
Green (Ch4) = output voltage,
Magenta/Red (Ch3) = auxiliary output voltage for the VIPer12A self-supply (on V_{DD} pin), and
Yellow (Ch1) = drain voltage.

Figure 2. Full Load Start-up Waveforms at 265V



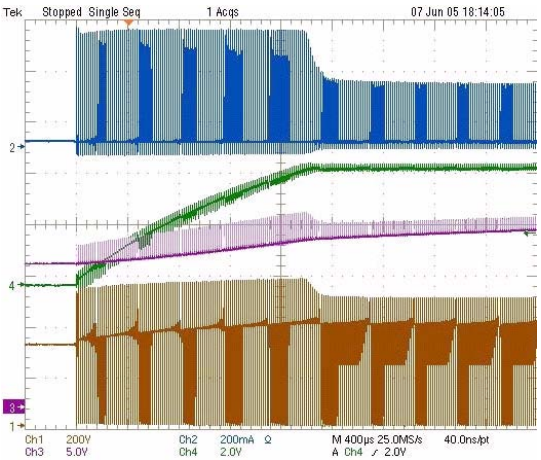
Notes: Cyan/Blue (Ch2) = drain current,
Green (Ch4) = output voltage,
Magenta/Red (Ch3) = auxiliary output voltage for the VIPer12A self-supply (on V_{DD} pin), and
Yellow (Ch1) = drain voltage.

Figure 3. Full Load Start-up Waveforms at 115V



Notes: Cyan/Blue (Ch2) = drain current,
Green (Ch4) = output voltage,
Magenta/Red (Ch3) = auxiliary output voltage for the VIPer12A self-supply (on V_{DD} pin), and
Yellow (Ch1) = drain voltage.

Figure 4. Full Load Start-up Waveforms at 230V

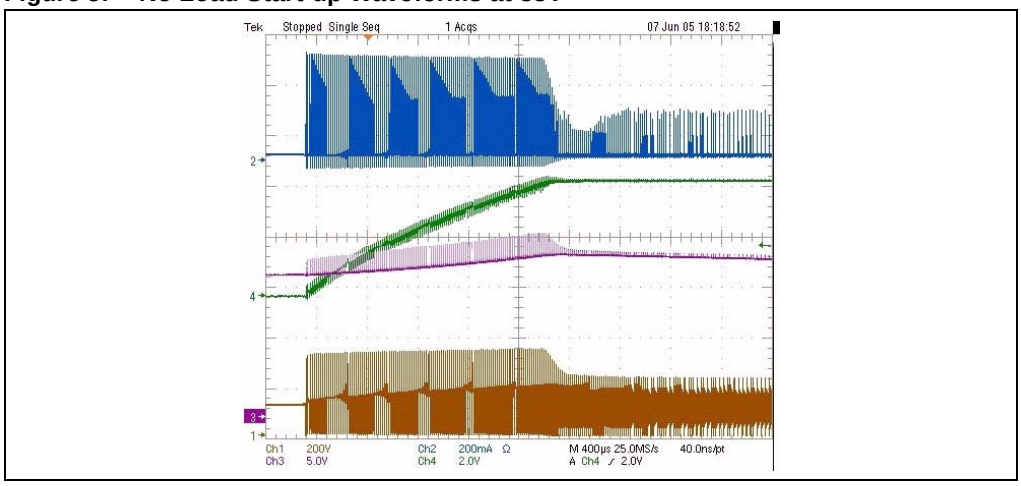


Notes: Cyan/Blue (Ch2) = drain current,
Green (Ch4) = output voltage,
Magenta/Red (Ch3) = auxiliary output voltage for the VIPer12A self-supply (on V_{DD} pin), and
Yellow (Ch1) = drain voltage.

2.1.2 No Load Start-up Waveforms

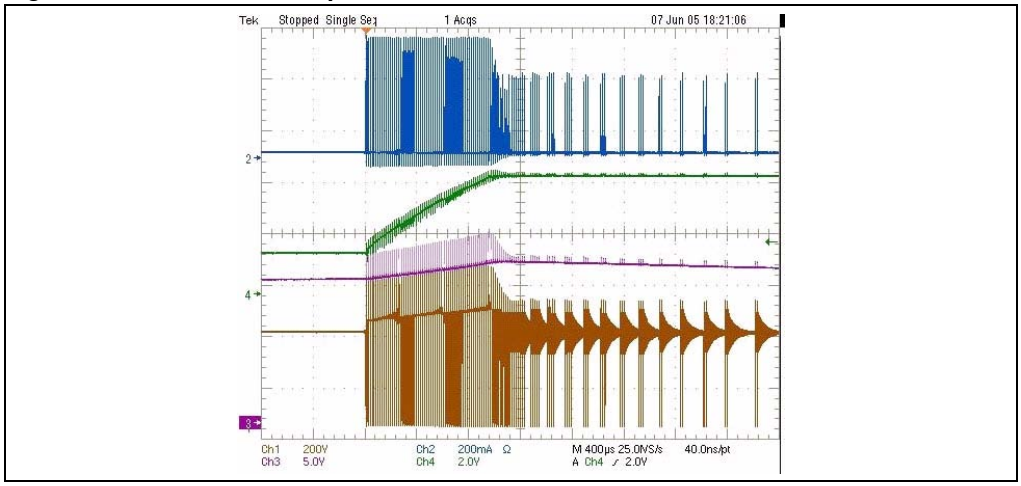
Figure 5, *Figure 6*, *Figure 7*, and *Figure 8 on page 19* show the same waveforms (*Section 2.1.1*) as they occur during the circuit start-up phase when no load is applied, for the minimum ($88V_{AC}$), maximum ($265V_{AC}$), and nominal voltages ($115V_{AC}$ and $230V_{AC}$).

Figure 5. No Load Start-up Waveforms at 88V



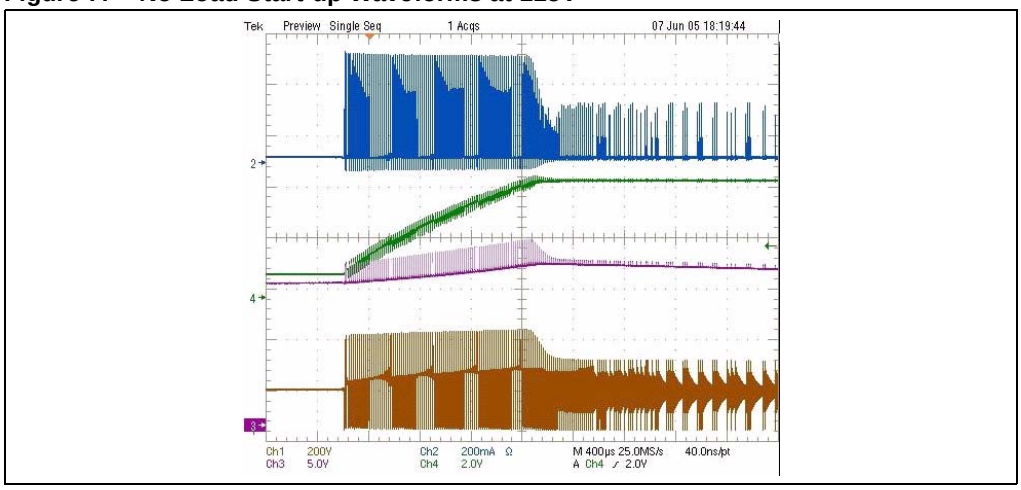
Notes: Cyan/Blue (Ch2) = drain current,
Green (Ch4) = output voltage,
Magenta/Red (Ch3) = auxiliary output voltage for the VIPer12A self-supply (on V_{DD} pin), and
Yellow (Ch1) = drain voltage.

Figure 6. No Load Start-up Waveforms at 265V



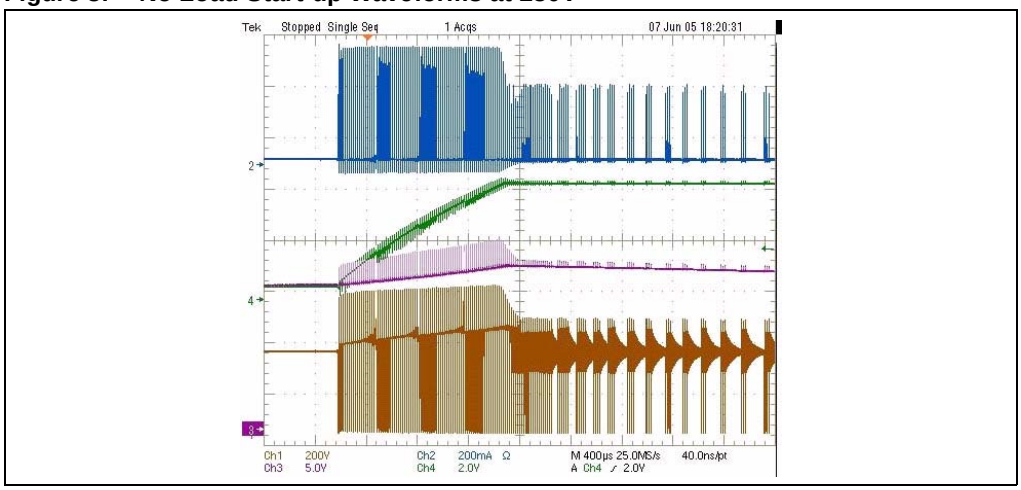
Notes: Cyan/Blue (Ch2) = drain current,
Green (Ch4) = output voltage,
Magenta/Red (Ch3) = auxiliary output voltage for the VIPer12A self-supply (on V_{DD} pin), and
Yellow (Ch1) = drain voltage.

Figure 7. No Load Start-up Waveforms at 115V



Notes: Cyan/Blue (Ch2) = drain current,
Green (Ch4) = output voltage,
Magenta/Red (Ch3) = auxiliary output voltage for the VIPer12A self-supply (on V_{DD} pin), and
Yellow (Ch1) = drain voltage.

Figure 8. No Load Start-up Waveforms at 230V



Notes: Cyan/Blue (Ch2) = drain current,
Green (Ch4) = output voltage,
Magenta/Red (Ch3) = auxiliary output voltage for the VIPer12A self-supply (on V_{DD} pin), and
Yellow (Ch1) = drain voltage.

2.2 Temperature Tests

These tests verify the board's device and component temperatures. *Table 3* shows critical temperatures (the most stress measured, in terms of power dissipation) for the board's main components.

Note: The tests were performed at 25°C (ambient temperature), in Full Load conditions.

Table 3. Component Critical Temperature Measurements

V_{INAC} (V_{RMS})	VIPer12A	Transformer	Clamp Resistor	Output Diode	Units
88V	38	37	36	45	°C
115V	39	36	37	45	°C
230V	42	38	38	45	°C
265V	45	35	39	45	°C

2.3 Dynamic Load Regulation Tests

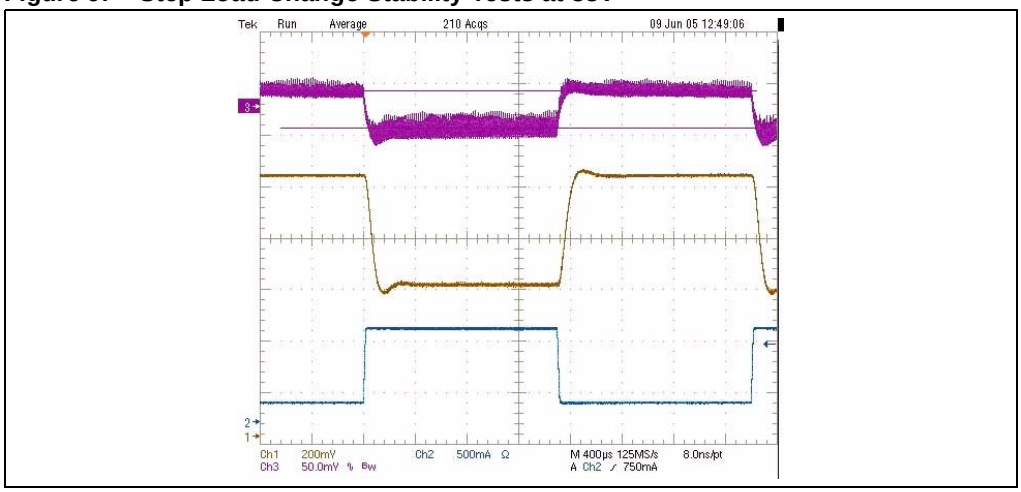
These tests monitor and verify the stability and quality of the system response to load changes, in terms of speed and overshoot. *Figure 9*, and *Figure 10 on page 21*, and *Figure 11*, and *Figure 12 on page 22* show the waveforms as they occur during the circuit load changes, for the minimum ($88V_{AC}$), maximum ($265V_{AC}$), and nominal voltages ($115V_{AC}$ and $230V_{AC}$).

During these tests, load changes from a minimum of 180mA to a maximum of 900mA are applied to the circuit as squarewaves, with 3ms periods and a duty cycle of 50%.

- The output voltage (Ch3) has a variation of some tenths of a mV (about 40mV), with some mV overshoots. These results indicate very good dynamic behavior on the part of the system.
- The VIPer12A feedback pin voltage (Ch1) in *Figure 10 on page 21* shows that when the input voltage is $265V_{AC}$, the load is 180mV (its minimum value) while the output and feedback pin voltages show some oscillation. This oscillation is not related to a low phase margin of the Loop Gain, but is related to the VIPer12A Burst mode operation.

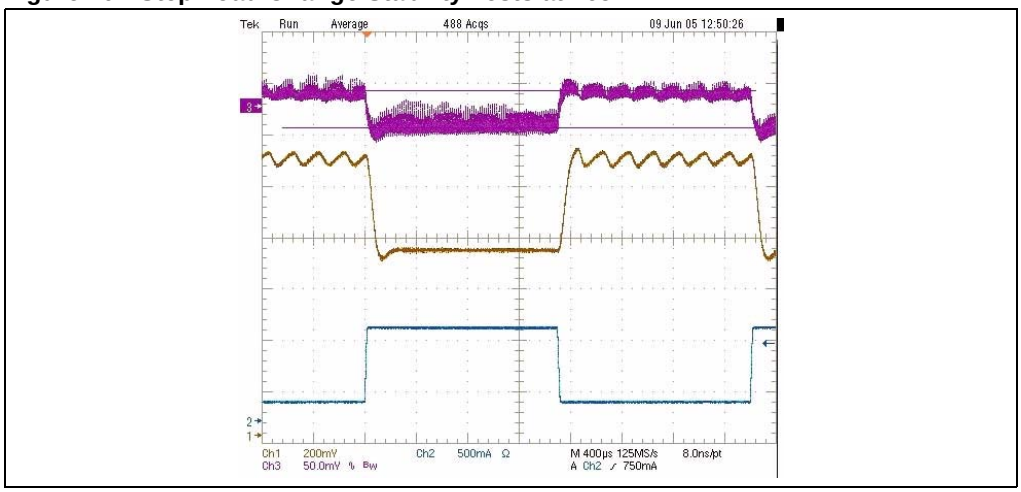
  Note: Even with the oscillation, the output voltages are still regulated well.

Figure 9. Step Load Change Stability Tests at 88V



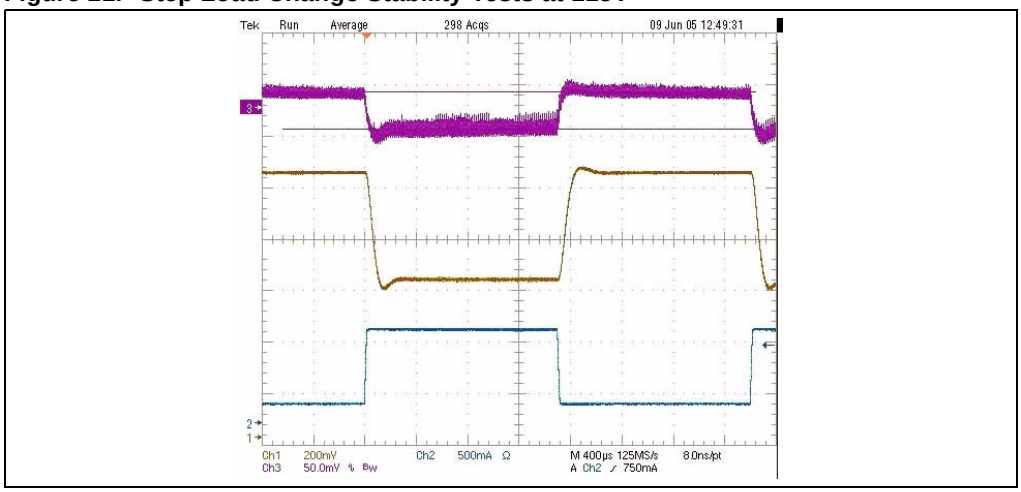
Notes: Magenta/Red (Ch3) = output voltage (set to 50mV/division),
Yellow (Ch1) = VIPer12A feedback pin voltage, and
Cyan/Blue (Ch2) = output (load) current.

Figure 10. Step Load Change Stability Tests at 265V



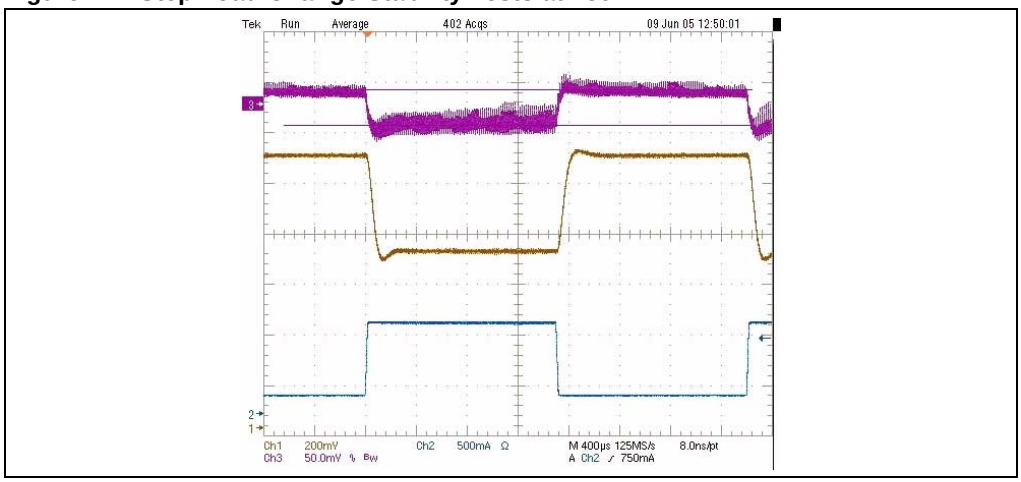
Notes: Magenta/Red (Ch3) = output voltage,
Yellow (Ch1) = feedback pin voltage, and
Cyan/Blue (Ch2) = output current.

Figure 11. Step Load Change Stability Tests at 115V



Notes: Magenta/Red (Ch3) = output voltage,
Yellow (Ch1) = feedback pin voltage, and
Cyan/Blue (Ch2) = output current.

Figure 12. Step Load Change Stability Tests at 230V



Notes: Magenta/Red (Ch3) = output voltage,
Yellow (Ch1) = feedback pin voltage, and
Cyan/Blue (Ch2) = output current.

2.4 Steady-State Tests

These tests evaluate the converter's behavior (see *Table 4*). The measurements include:

- converter efficiency for the minimum ($88V_{AC}$), maximum ($265V_{AC}$), and nominal input voltages ($115V_{AC}$ and $230V_{AC}$),
- output voltage quality (Static Load regulation, where voltage output is measured in both full load and no load conditions), and
- voltage ripple which is superimposed on the output voltage at the switching frequency (see *Table 5*).

Note: The tests were performed in Full Load conditions.

Table 4. Steady-state Full Load Condition Measurements

V_{INAC} (V_{RMS})	P_{IN} (W)	P_{OUT} (W)	V_O (V)	η (%)
88V	5.9	4.13	4.59	70
115V	5.9	4.13	4.59	70
230V	5.9	4.13	4.59	70
265V	6.1	4.13	4.59	68

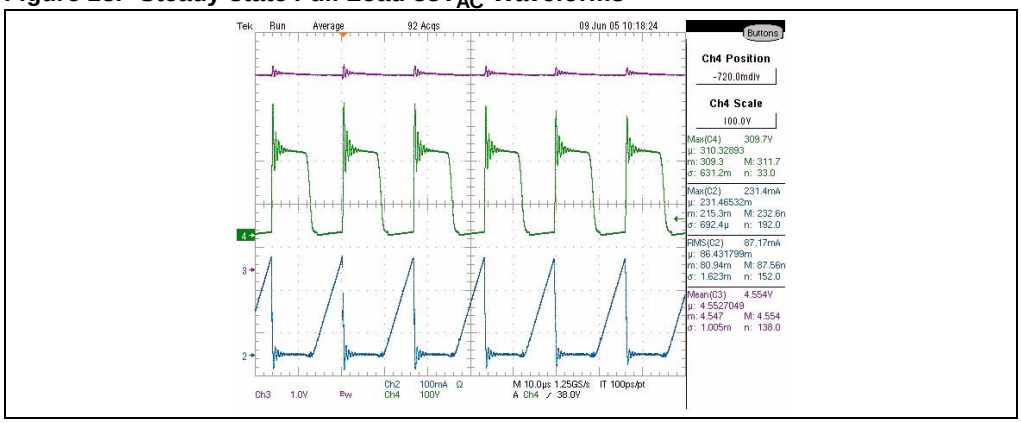
Table 5. Steady-state Output Voltage Ripple

Input Voltage (V_{RMS})	ΔV_O at Full Load
88V	210mV
115V	214mV
230V	215mV
265V	220mV

2.4.1 Steady-State Full Load Waveforms

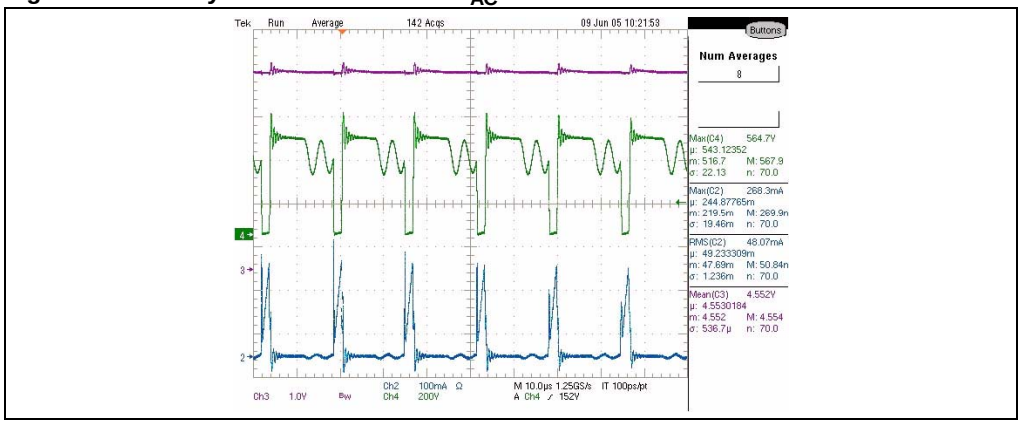
Figure 13 and *Figure 14*, and *Figure 15* and *Figure 16 on page 25* show the waveforms that occur during converter steady-state testing when it is in Full Load condition, for the minimum ($88V_{AC}$), maximum ($265V_{AC}$), and nominal voltages ($115V_{AC}$ and $230V_{AC}$).

Figure 13. Steady-state Full Load $88V_{AC}$ Waveforms



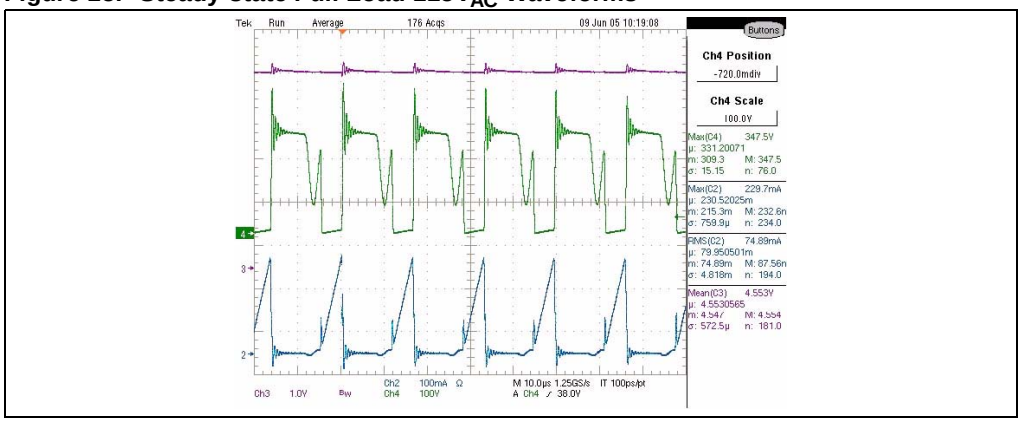
Notes: Magenta/Red (Ch3) = output voltage,
Green (Ch4) = drain voltage, and
Cyan/Blue (Ch2) = drain current.

Figure 14. Steady-state Full Load $265V_{AC}$ Waveforms



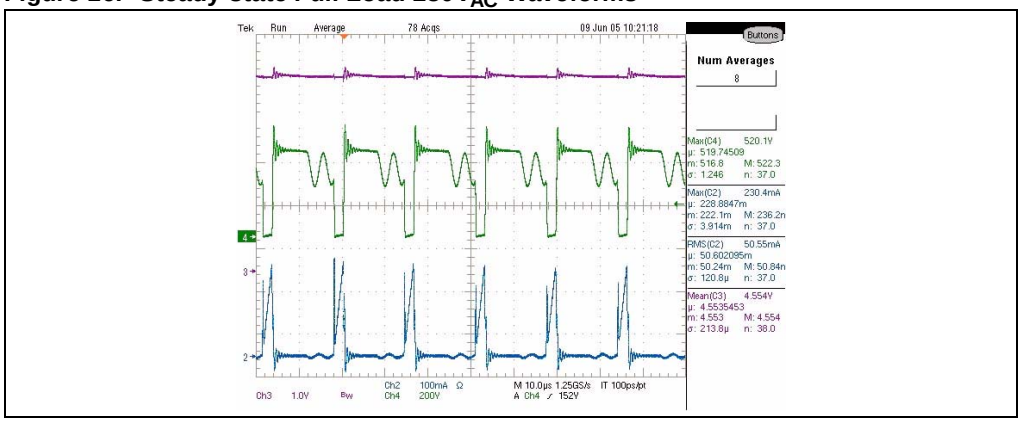
Notes: Magenta/Red (Ch3) = output voltage,
Green (Ch4) = drain voltage, and
Cyan/Blue (Ch2) = drain current.

Figure 15. Steady-state Full Load 115V_{AC} Waveforms



Notes: Magenta/Red (Ch3) = output voltage,
Green (Ch4) = drain voltage, and
Cyan/Blue (Ch2) = drain current.

Figure 16. Steady-state Full Load 230V_{AC} Waveforms

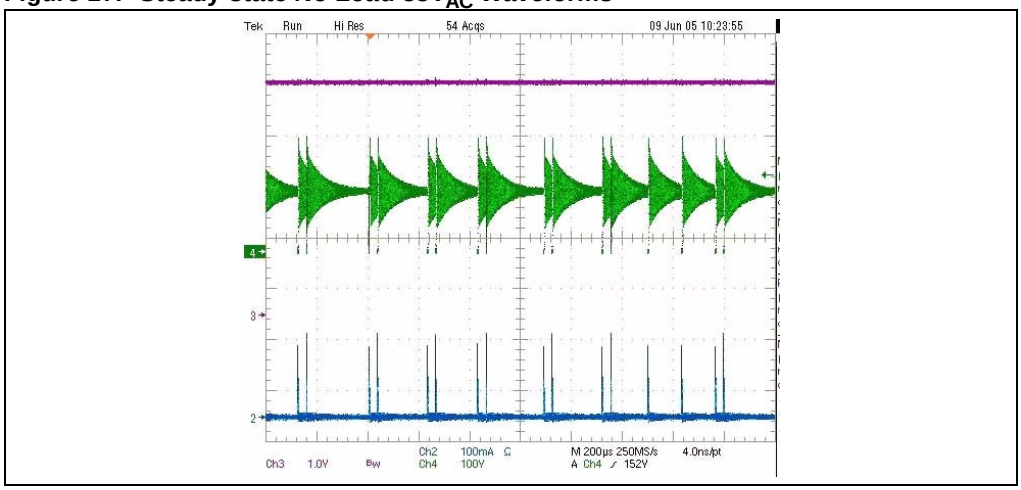


Notes: Magenta/Red (Ch3) = output voltage,
Green (Ch4) = drain voltage, and
Cyan/Blue (Ch2) = drain current.

2.4.2 Steady-State No Load Waveforms

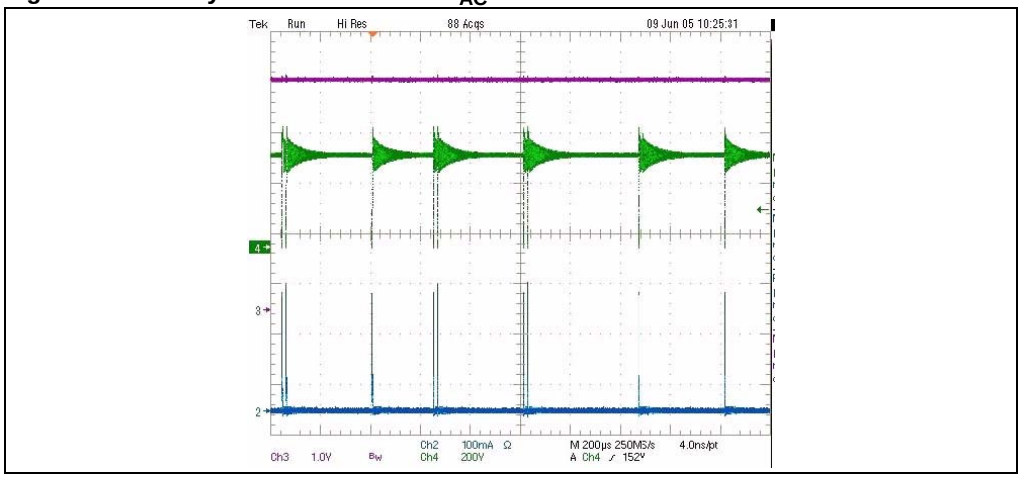
Figure 17 and *Figure 18*, and *Figure 19* and *Figure 20 on page 27* show the waveforms that occur during converter steady-state testing when it is in No Load condition, for the minimum ($88V_{AC}$), maximum ($265V_{AC}$), and nominal voltages ($115V_{AC}$ and $230V_{AC}$).

Figure 17. Steady-state No Load $88V_{AC}$ Waveforms



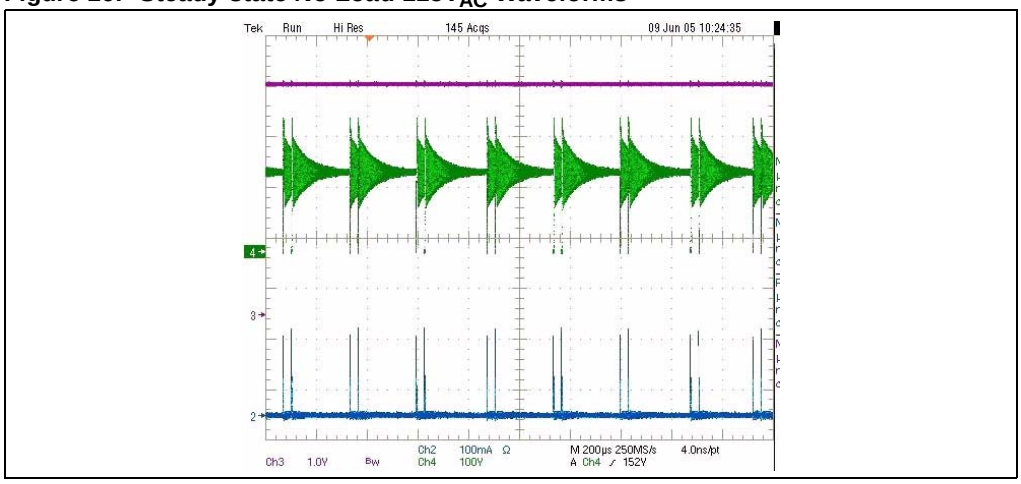
Notes: Magenta/Red (Ch3) = output voltage,
Green (Ch4) = drain voltage, and
Cyan/Blue (Ch2) = drain current.

Figure 18. Steady-state No Load $265V_{AC}$ Waveforms



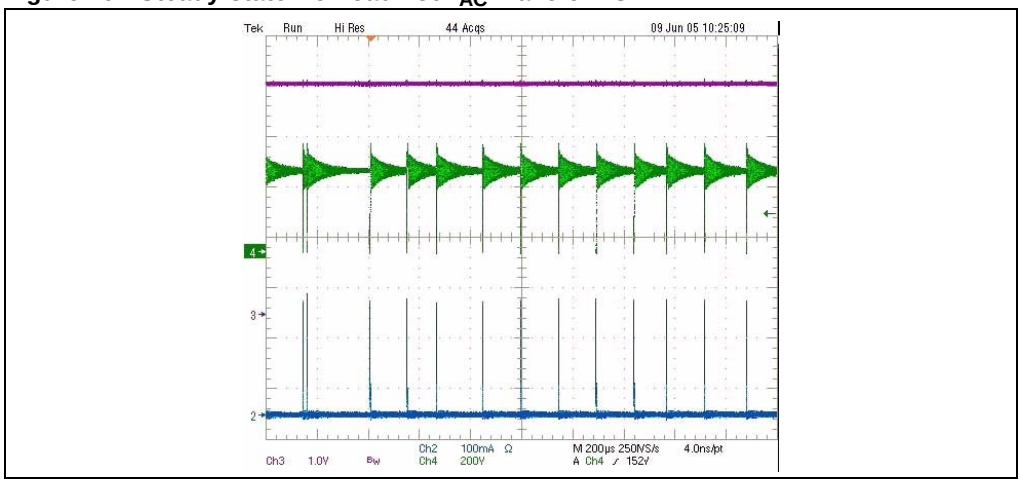
Notes: Magenta/Red (Ch3) = output voltage,
Green (Ch4) = drain voltage, and
Cyan/Blue (Ch2) = drain current.

Figure 19. Steady-state No Load 115V_{AC} Waveforms



Notes: Magenta/Red (Ch3) = output voltage,
Green (Ch4) = drain voltage, and
Cyan/Blue (Ch2) = drain current.

Figure 20. Steady-state No Load 230V_{AC} Waveforms



Notes: Magenta/Red (Ch3) = output voltage,
Green (Ch4) = drain voltage, and
Cyan/Blue (Ch2) = drain current.

2.5 EMI Tests

Pre-compliant tests with European Normative EN55022 for electromagnetic interference (EMI) were performed. *Figure 21* and *Figure 22*, and *Figure 23* and *Figure 24 on page 29* illustrate that the conducted EMI induced by the converter to the main are below the normative limits.

Note: *Figure 21* through *Figure 24* show the Input current spectrum to be inside the 150kHz to 30MHz frequency range.

Figure 21. $115V_{AC}$ Line Voltage

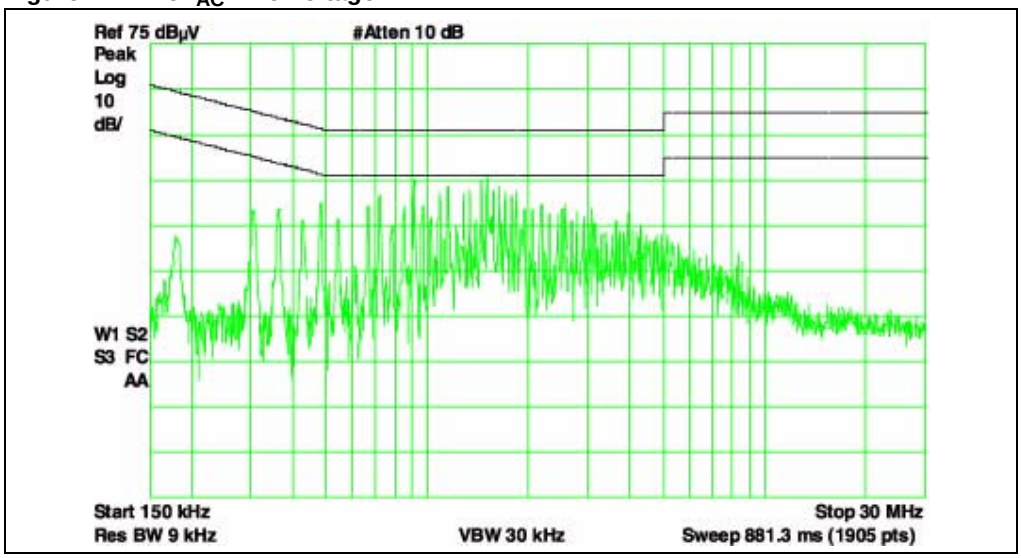


Figure 22. $115V_{AC}$ Line Neutral

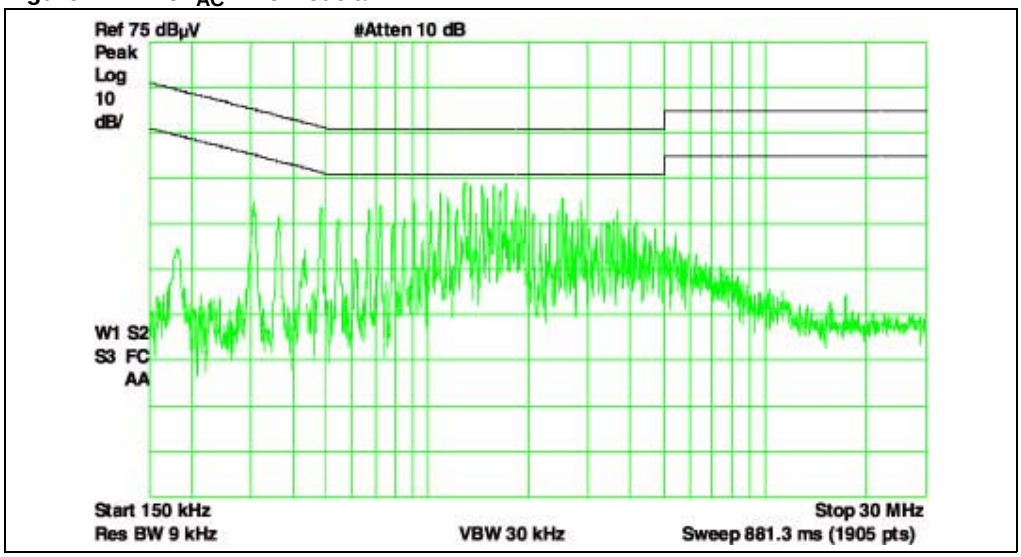


Figure 23. 230V_{AC} Line Voltage

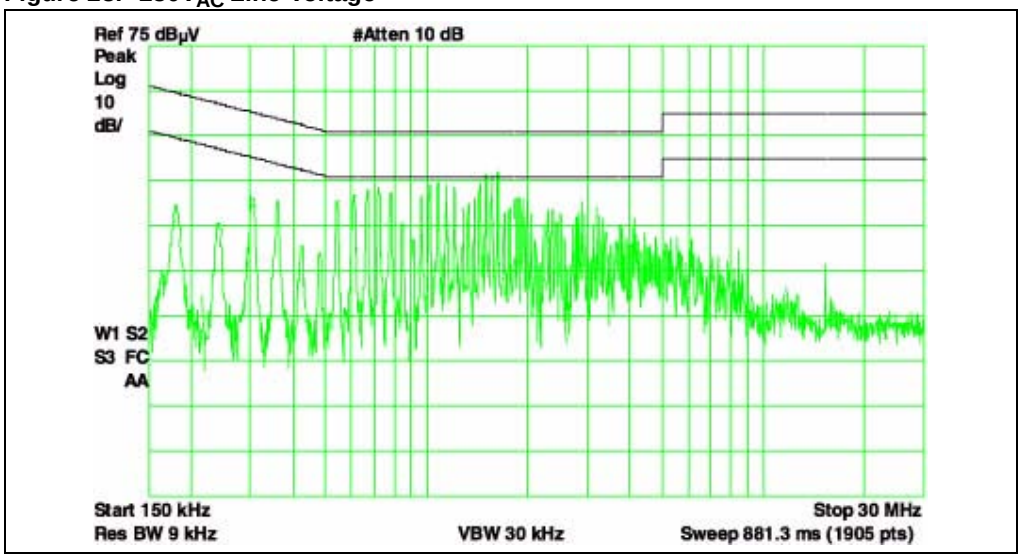
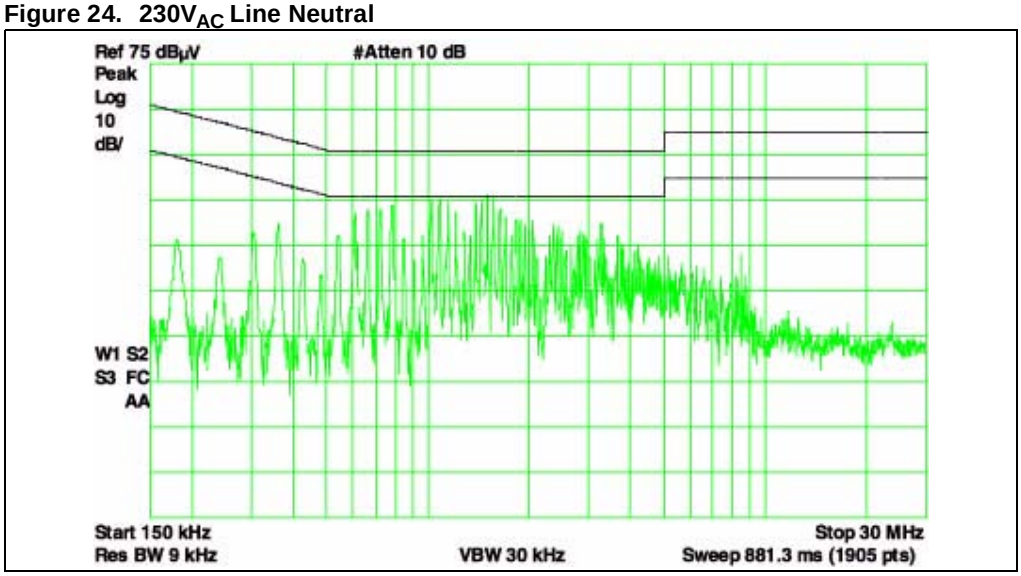
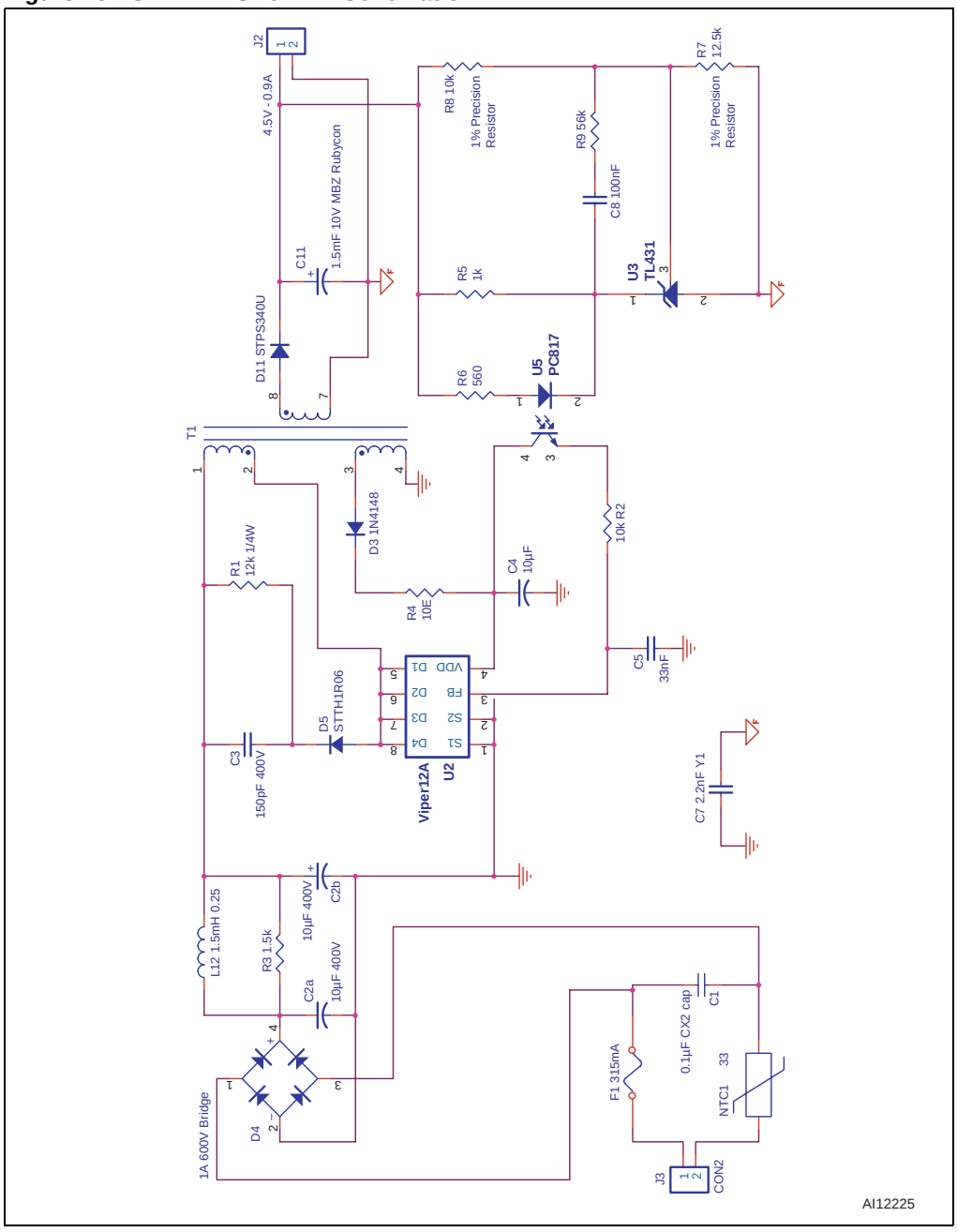


Figure 24. 230V_{AC} Line Neutral



Appendix A STEVAL-ISA011V Demo Board Schematic

Figure 25. STEVAL-ISA011V1 Schematic



Appendix B STEVAL-ISA011V1 Bill of Materials

Table 6. Bill Of Materials

Item	Qty	Reference	Value
1	1	C1	0.1uF CX2 cap
2	2	C2a, C2b	10uF 400V
3	1	C3	150pF 400V
4	1	C4	10uF
5	1	C5	33nF
6	1	C6	47pF 400V
7	1	C7	1.8nF Y1
8	1	C8	100nF
9	1	C11	1.5mF 10V MBZ (10X16) Rubycon (Low ESR Capacitor)
10	1	D3	1N4148
11	1	D4	1A 600V Bridge
12	1	D5	STTH1R06 STMicroelectronics Part
13	1	D11	STPS340U (SMB Package) STMicroelectronics Part
14	1	F1	250mA
15	1	L12	1.5mH 0.25A
16	1	NTC1	33Ω
17	1	R1	12K 1/4W
18	2	R2	10k
19	1	R3	1.5k
20	1	R4	10E
21	1	R5	1k
22	1	R6	560
23	1	R7	12.5k 1% Precision Resistor
24	1	R8	10k 1% Precision Resistor
25	1	R9	56k
26	1	T1	TDK SRW16ES_E44H013
27	1	U2	VIPer12A (ST Part)
28	1	U3	TL1431 (ST Part)
29	1	U4	PC817

3 Revision History

Table 7. Document revision history

Date	Revision	Changes
2-February-2006	1	First edition