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# 1 Main characteristics and circuit description

The main characteristics of the SMPS are:

- Line voltage range: 90 to 265 Vac
- Minimum line frequency ( $f_L$ ): 47 Hz
- Regulated output voltage: 400 V
- Rated output power: 100 W
- Maximum  $2 f_L$  output voltage ripple: 20 V peak-to-peak
- Hold-up time: 10 ms ( $V_{DROP}$  after hold-up time is 300 V)
- Minimum switching frequency: 40 kHz
- Minimum estimated efficiency 92% (at  $V_{in} = 90$  Vac,  $P_{out} = 100$  W)
- Maximum ambient temperature: 50 °C
- PCB type and size: Single-side, 35  $\mu$ m, CEM-1, 90 x 83 mm

This demonstration board implements a 100 W power factor correction (PFC) pre-regulator, continuous power, on a regulated 400 V rail from a wide range mains voltage and provides for the reduction of the mains harmonics, which allows meeting the European EN61000-3-2 or the Japanese JEITA-MITI standard. The regulated output voltage is typically the input for the cascaded isolated DC-DC converter that provides the output rails required by the load.

The board is designed to allow full-load operation in still air.

The power stage of the PFC is a conventional boost converter, connected to the output of the rectifier bridge D1. It is completed by the coil L2, the diode D3 and the capacitor C6. The boost switch is represented by the power MOSFET Q1. The NTC R1 limits the inrush current at switch-on. It is connected to the DC rail, in series to the output electrolytic capacitor, in order to improve the efficiency during low line operation because the RMS current flowing into the output stage is lower than current flowing into the input stage at the same input voltage, thus increasing efficiency. The board is equipped with an input EMI filter necessary to filter the commutation noise coming from the boost stage.

At startup the L6564 is powered by the Vcc capacitor C11 that is charged via the resistors R7 and R16. Then the L2 secondary winding and the charge pump circuit (C7, R4, D4 and D5) generate the Vcc voltage, powering the L6564 during normal operation. The L2 secondary winding is also connected to the L6564 pin #7 (ZCD) through the resistor R5. Its purpose is to supply the information that L2 has demagnetized, needed by the internal logic for triggering a new switching cycle.

The divider R9, R12, R17 and R19 provides the L6564 multiplier with the information of the instantaneous mains voltage that is used to modulate the peak current of the boost.

The resistors R2, R8, R10 with R13 and R14 are dedicated to sense the output voltage and send to the L6564 the feedback information necessary to regulate the output voltage. The components C9, R18 and C8 constitute the error amplifier compensation network necessary to keep the required loop stability.

The peak current is sensed by resistors R25 and R26 in series to the MOSFET and the signal is fed into pin #4 (CS) of the L6564. On pin #4 (CS) there is also a small filter composed of R24 and C15.

The capacitor C13 and the parallel resistor R32 complete an internal peak-holding circuit that obtains information on the RMS mains voltage. The voltage signal at pin #5, which is a

DC level equal to the peak voltage on pin #3 (MULT), is fed to a second input to the multiplier for the  $1/V^2$  function necessary to compensate the control loop gain dependence on the mains voltage. Additionally, the pin #5 ( $V_{FF}$ ) is internally connected to a comparator providing brownout (AC mains undervoltage) protection. A voltage below 0.8 V shuts down (does not latch) the IC and brings its consumption to a considerably lower level. The L6564 restarts as the voltage at the pin rises above 0.88 V.

The divider R3, R6, R11 and R15 provides the L6564 pin #6 (PFC\_OK) with the information regarding the output voltage level. This information is required by the L6564 output voltage monitoring and disable functions used for PFC protection purposes.

If the voltage on pin #6 exceeds 2.5 V, the IC stops switching and restarts as the voltage on the pin falls below 2.4 V, implementing the dynamic OVP and preventing the output voltage from becoming excessive in case of transients because of the slow response of the error amplifier. However, if at the same time, the voltage of the INV pin is lower than 2.4V and falls 40 mV below that of the pin PFC\_OK, a feedback failure is assumed. In this case the device is latched off. Normal operation can be resumed only by cycling Vcc, bringing its value lower than 6 V before rising up to the turn-on threshold.

Additionally, if the voltage on pin #6 (PFC\_OK) is tied below 0.23 V, the L6564 shuts down. To restart the L6564, the voltage on pin #6 (PFC\_OK) has to increase above 0.27 V. This function can be used as a remote on/off control input.

To allow interfacing the board with a D2D converter, the connector J3 allows powering the L6564 with an external Vcc and also controlling the IC operation via pin #6 (PFC\_OK).



## Bill of material

Table 1. EVL6564-100W TM PFC bill of material

Des.	Part type/part value	Case/package	Description	Supplier
C1	470N	DWG	X2 - FLM cap - R46-I 3470--M1-	Arcotronics
C4	470N	DWG	X2 - FLM cap - R46-I 3470--M1-	Arcotronics
C5	470N - 400V	DWG	400V - FLM cap - B32653A4474	Epcos
C6	47 $\mu$ F - 450V	Dia. 18X31.5 mm	450V - aluminium ELCAP - ED series - 105°C	Nippon-chemicon
C7	4N7	1206	100V CERCAP - general purpose	AVX
C8	680N	1206	25V CERCAP - general purpose	AVX
C9	68N	0805	50V CERCAP - general purpose	AVX
C10	100N	1206	50V CERCAP - general purpose	AVX
C11	47 $\mu$ F-50V	Dia. 5X10 mm	50V - aluminium ELCAP - YXF series - 105°C	Rubycon
C12	2N2	1206	50V CERCAP - general purpose	AVX
C13	1 $\mu$ F	0805	25V CERCAP - general purpose	AVX
C15	220p	0805	50V CERCAP - general purpose	AVX
C16	2N2	0805	50V CERCAP - general purpose	AVX
D1	GBU4J	STYLE GBU	Single phase bridge rectifier	Vishay
D2	1N4005	DO-41	Rectifier - general purpose	Vishay
D3	STTH2L06	DO-41	Ultrafast high voltage rectifier	STMicroelectronics
D4	LL4148	MINIMELF	High speed signal diode	Vishay
D5	BZX79-C18	DO - 35	Zener diode	Vishay
F1	FUSE 4A	DWG	Fuse T4A - time delay	Wichmann
HS1	HEAT-SINK	DWG	Heat sink for D1& Q1	
JPX3	0R0	1206	SMD jumper	VISHAY
J1	MKDS 1,5/ 3-5,08	DWG	PCB term. block, screw conn., pitch 5mm - 3 W.	Phoenix Contact



Table 1. EVL6564-100W TM PFC bill of material (continued)

Des.	Part type/part value	Case/package	Description	Supplier
J2	MKDS 1,5/ 2-5,08	DWG	PCB term. block, screw conn., pitch 5mm - 2 W.	Phoenix Contact
J3	CON3	DWG	PCB term. block, pitch 2.5mm - 3 W.	Molex
L1	HF2826-203Y1R5-T01	DWG	Input emi filter - 20mH-1.5A	TDK
L2	SRW2620PQ-X22V102	DWG	PFC inductor - 0.52mH (X08141-01-B)	TDK
Q1	STF7NM50N	TO-220FP	N-channel power mosfet	STMicroelectronics
R1	NTC 2R5-S237	DWG	NTC resistor P/N B57237S0259M000	EPCOS
R2	1M0	1206	SMD standard film res - 1/4W - 1% - 100ppm/°C	Vishay
R8	1M0	1206	SMD standard film res - 1/4W - 1% - 100ppm/°C	Vishay
R10	1M0	1206	SMD standard film res - 1/4W - 1% - 100ppm/°C	Vishay
R3	3M3	1206	SMD standard film res - 1/4W - 1% - 100ppm/°C	Vishay
R6	3M3	1206	SMD standard film res - 1/4W - 1% - 100ppm/°C	Vishay
R4	100R	1206	SMD standard film res - 1/4W - 5% - 250ppm/°C	Vishay
R5	68K	1206	SMD standard film res - 1/4W - 1% - 100ppm/°C	Vishay
R7	180K	1206	SMD standard film res - 1/4W - 5% - 250ppm/°C	Vishay
R16	180K	1206	SMD standard film res - 1/4W - 5% - 250ppm/°C	Vishay
R9	2M7	1206	SMD standard film res - 1/4W - 1% - 100ppm/°C	Vishay
R12	2M7	1206	SMD standard film res - 1/4W - 1% - 100ppm/°C	Vishay
R11	2M2	1206	SMD standard film res - 1/4W - 1% - 100ppm/°C	Vishay
R13	62K	0805	SMD standard film res - 1/8W - 1% - 100ppm/°C	Vishay
R14	27K	0805	SMD standard film res - 1/8W - 1% - 100ppm/°C	Vishay
R15	51K	0805	SMD standard film res - 1/8W - 1% - 100ppm/°C	Vishay
R17	1M5	1206	SMD standard film res - 1/4W - 1% - 100ppm/°C	Vishay
R18	82K	0805	SMD standard film res - 1/8W - 5% - 250ppm/°C	Vishay
R19	51K	1206	SMD standard film res - 1/4W - 5% - 250ppm/°C	Vishay
R21	27R	1206	SMD standard film res - 1/4W - 5% - 250ppm/°C	Vishay

**Table 1. EVL6564-100W TM PFC bill of material (continued)**

Des.	Part type/part value	Case/package	Description	Supplier
R22	100K	0805	SMD standard film res - 1/8W - 5% - 250ppm/°C	Vishay
R24	220R	PTH	SFR25 AXIAL STAND. FILM RES - 0.4W - 5% - 250ppm/°C	Vishay
R25	0R47	PTH	SFR25 AXIAL STAND. FILM RES - 0.4W - 5% - 250ppm/°C	Vishay
R26	0R68	PTH	SFR25 AXIAL STAND. FILM RES - 0.4W - 5% - 250ppm/°C	Vishay
R30	1K	0805	SMD standard film res - 1/8W - 5% - 250ppm/°C	Vishay
R31	10R	0805	SMD standard film res - 1/8W - 5% - 250ppm/°C	Vishay
R32	1M0	0805	SMD standard film res - 1/8W - 1% - 250ppm/°C	Vishay
U1	L6564D	SSOP-10	Transition-mode PFC controller	STMicroelectronics

### 3 Test results and significant waveforms

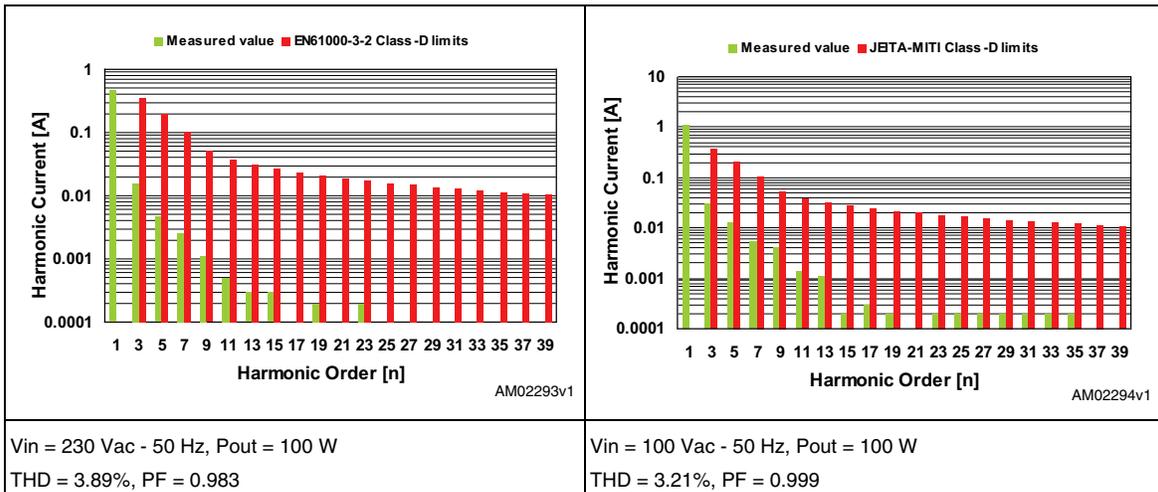
#### 3.1 Harmonic content measurement

One of the main purposes of a PFC pre-conditioner is the correction of input current distortion, decreasing the harmonic contents below the limits of the relevant regulations. Therefore, this demonstration board has been tested at full load at both the nominal input voltage mains according to the European standard EN61000-3-2 Class-D and Japanese standard JEITA-MITI Class-D.

The circuit is able to reduce the harmonics well below the limits of both regulations from full load down to light load (measurements are given in *Figure 3* and *Figure 4*). Please note that all measures and waveforms have been done using a Pi-filter (using a 20 mH common mode choke and two 470NF-X2 filter capacitors) to filter the noise coming from the circuit.

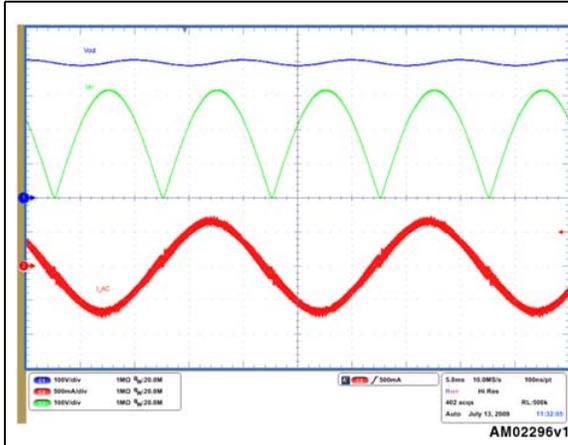
**Figure 3. EVL6564-100W TM PFC: compliance to EN61000-3-2 standard**

**Figure 4. EVL6564-100W TM PFC: compliance to JEITA-MITI standard**



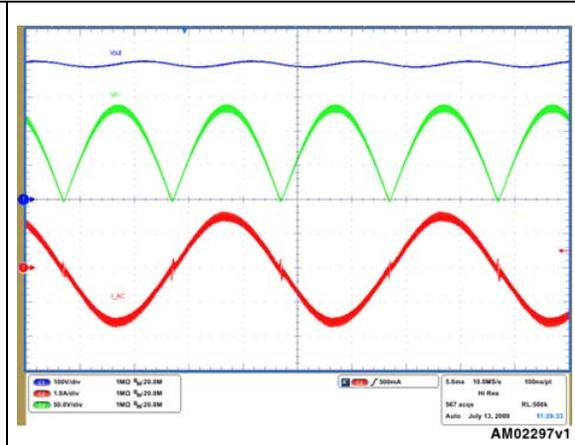
For user reference, waveforms of the input current and voltage at the nominal input voltage mains and different load conditions are given in [Figure 5](#) and [Figure 6](#).

**Figure 5. EVL6564-100W TM PFC: input current waveform at 230 V - 50 Hz 100 W load**



CH1: Vout  
CH2: I\_AC  
CH3: V bridge

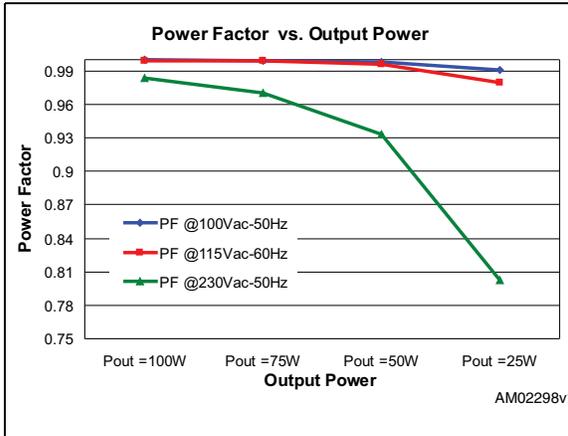
**Figure 6. EVL6564-100W TM PFC: input current waveform at 100 V - 50 Hz 100 W load**



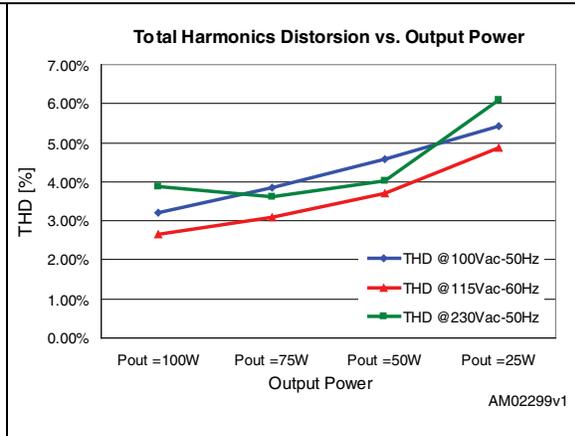
CH1: Vout  
CH2: I\_AC  
CH3: V bridge

The power factor (PF) and the total harmonic distortion (THD) have been measured too and the results are given in [Figure 7](#) and [Figure 8](#). As visible, the PF remains close to unity throughout the input voltage mains and the total harmonic distortion is very low.

**Figure 7. EVL6564-100W TM PFC: power factor vs. output power**

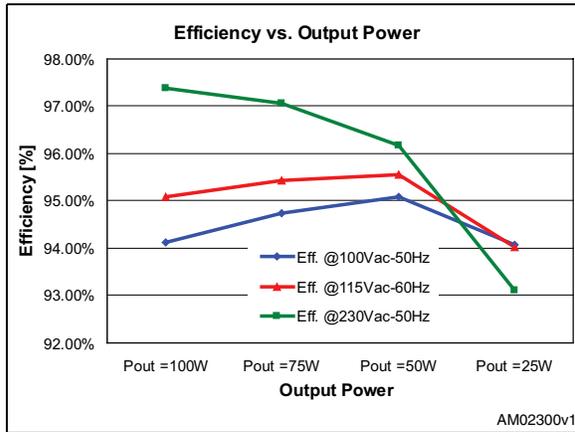


**Figure 8. EVL6564-100W TM PFC: THD vs. output power**

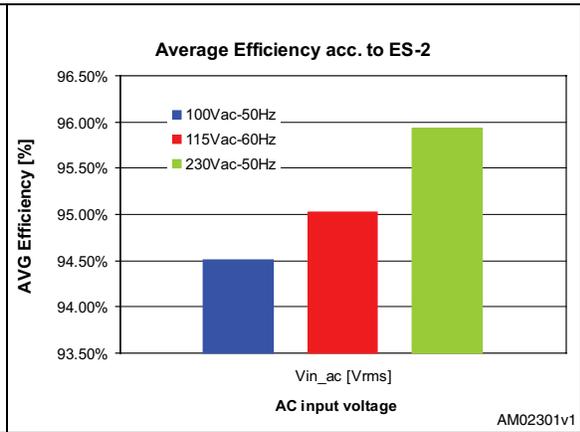


The efficiency, measured according to the ES-2 requirements, is very good at all load and line conditions ([Figure 9](#)). At full load it is always higher than 94%, making this design suitable for high-efficiency power supplies. The average efficiency, calculated according to the ES-2 requirements at different nominal mains voltages, is given in [Figure 10](#).

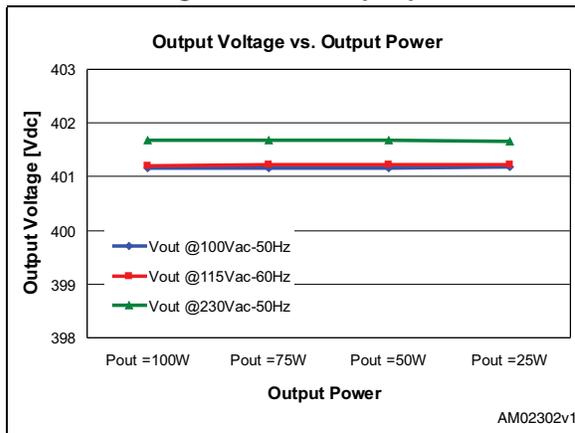
**Figure 9. EVL6564-100W TM PFC: efficiency vs. output power**



**Figure 10. EVL6564-100W TM PFC: average efficiency acc. to ES-2**



**Figure 11. EVL6564-100W TM PFC: static Vout regulation vs. output power**

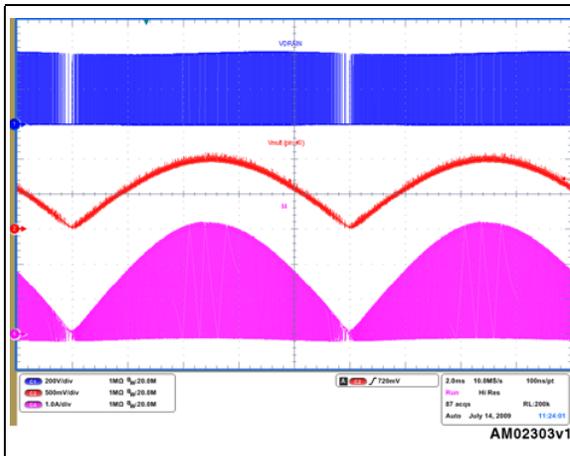


The measured output voltage at different line and static load conditions is given in [Figure 11](#). As visible, the voltage is very stable over the entire input voltage and output load range.

### 3.2 Inductor current in TM and L6564 THD optimizer

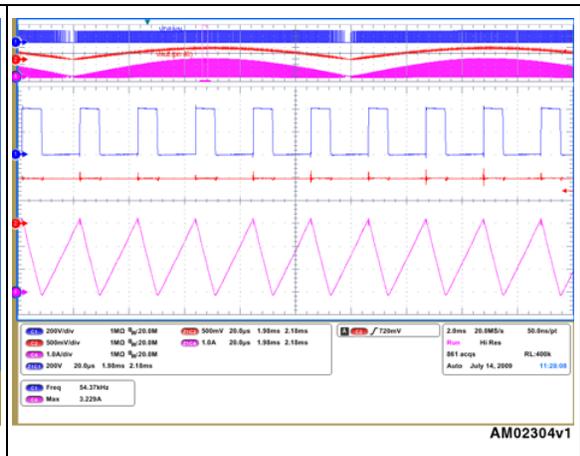
Figure 12 through 17 show the waveforms relevant to the inductor current at different voltage mains. As visible in Figure 12 and Figure 14 the peak inductor current waveform over a line half-period follows the MULT (pin #3) at both input mains voltage and therefore the line current is in phase with the input AC voltage, giving low distortion of the current waveform and high power factor. On both the drain voltage traces, close to the zero-crossing points of the sine wave, it is possible to note the action of the THD optimizer embedded in the L6564. It is a circuit that minimizes the conduction dead-angle occurring in the AC input current near the zero-crossings of the line voltage (crossover distortion). In this way, the THD (total harmonic distortion) of the current is considerably reduced. A major cause of this distortion is the inability of the system to transfer energy effectively when the instantaneous line voltage is very low. This effect is magnified by the high-frequency filter capacitor placed after the bridge rectifier, which retains some residual voltage that causes the diodes of the bridge rectifier to be reverse-biased and the input current flow to temporarily stop. To overcome this issue, the device forces the PFC pre-regulator to process more energy near the line voltage zero-crossings as compared to that commanded by the control loop. This results in both minimizing the time interval where energy transfer is lacking and fully discharging the high-frequency filter capacitor after the bridge. Essentially, the circuit artificially increases the ON-time of the power switch with a positive offset added to the output of the multiplier in the proximity of the line voltage zero-crossings. This offset is reduced as the instantaneous line voltage increases, so that it becomes negligible as the line voltage moves toward the top of the sinusoid. Furthermore, the offset is modulated by the voltage on the VFF pin so as to have little offset at low line, where energy transfer at zero-crossings is typically quite good, and a larger offset at high line where the energy transfer gets worse. To derive maximum benefit from the THD optimizer circuit, the high-frequency filter capacitors after the bridge rectifier should be minimized, to be compatible with EMI filtering needs. A large capacitance, in fact, introduces a conduction dead-angle of the AC input current in itself, thus reducing the effectiveness of the optimizer circuit.

Figure 12. EVL6564-100W TM PFC: Vds & inductor current at 100 Vac - 50 Hz - full load



CH1: Q1 drain voltage  
 CH2: MULT voltage - Pin #3  
 CH4: L2 inductor current

Figure 13. EVL6564-100W TM PFC: Vds & inductor current at 100 Vac - 50 Hz - full load

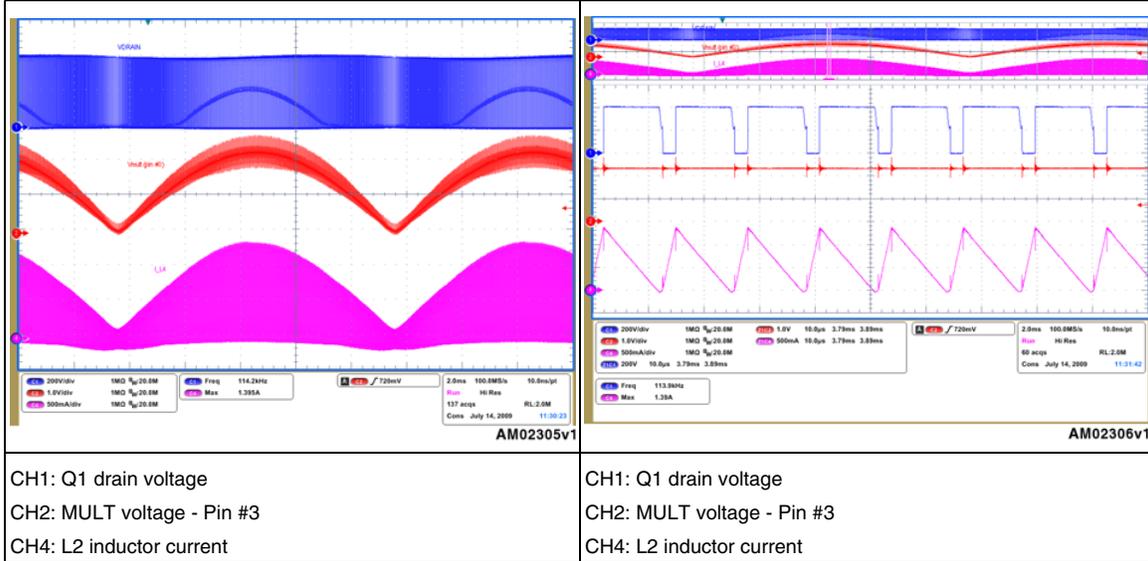


CH1: Q1 drain voltage  
 CH2: MULT voltage - Pin #3  
 CH4: L2 inductor current

In *Figure 13* and *Figure 15* the detail of the waveforms at the switching frequency allows measuring the operating frequency and the current peak at the top of the input sine wave during operation at 100 Vac and 230 Vac. A multiplier waveform has been captured as reference.

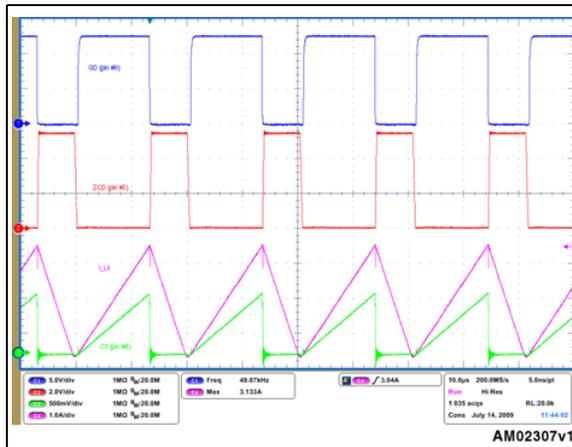
**Figure 14. EVL6564-100W TM PFC: Vds & inductor current at 230Vac - 50 Hz - full load**

**Figure 15. EVL6564-100W TM PFC: Vds & inductor current at 230Vac - 50 Hz - full load**



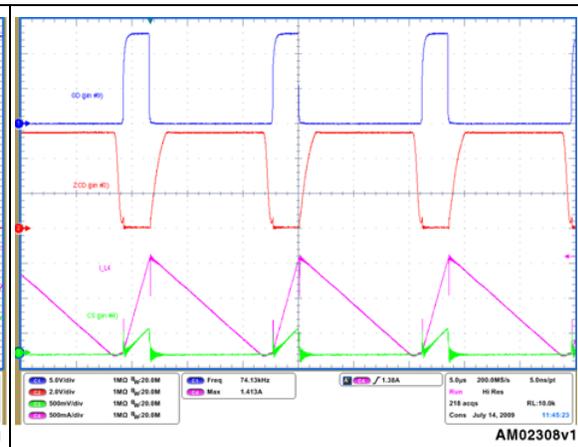
In *Figure 16* and *Figure 17* the detail of the waveforms at the switching frequency allows viewing the operation of the transition mode control. Once the inductor has transferred all the energy stored, a falling edge on the ZCD pin (pin #5) is detected which triggers a new on-time by setting the gate drive to high. As soon as the current signal on the CS pin (pin #4) has reached the level programmed by the internal multiplier circuitry according to the input mains instantaneous voltage and the error amplifier output level, the gate drive is set low and MOSFET conduction is stopped. A following off-time transfers the energy stored in the inductor into the output capacitor and to the load. At the end of the current conduction a new demagnetization is detected by the ZCD pin that provides for a new on-time of the MOSFET.

**Figure 16. EVL6564-100W TM PFC: Vds & inductor current at 230 Vac - 50 Hz - full load**



CH1: GD - Pin #9  
 CH2: ZCD - Pin #7  
 CH3: CS - Pin #4  
 CH4: L2 inductor current

**Figure 17. EVL6564-100W TM PFC: Vds & inductor current at 230 Vac - 50 Hz - full load**



CH1: GD - Pin #9  
 CH2: ZCD - Pin #7  
 CH3: CS - Pin #4  
 CH4: L2 inductor current

### 3.3 Voltage feed-forward and brownout functions

The power stage gain of PFC pre-regulators varies with the square of the RMS input voltage. Because the gain has a single pole characteristic, the crossover frequency  $f_c$  varies with the square of the RMS input voltage. This leads to large trade-off in the design. For example, setting the gain of the error amplifier to get  $f_c = 20$  Hz at 264 Vac means having  $f_c \approx 4$  Hz at 88 Vac, resulting in a sluggish control dynamics. Additionally, the slow control loop causes large transient current flow during rapid line or load changes that are limited by the dynamics of the multiplier output. This limit is considered when selecting the sense resistor to let the full load power pass under minimum line voltage conditions, with some margin. However a fixed current limit allows excessive power input at high line, whereas a fixed power limit requires the current limit to vary inversely with the line voltage.

Voltage feed-forward can compensate for the gain variation with the line voltage and allow overcoming all of the above-mentioned issues. It consists of deriving a voltage proportional to the input RMS voltage, feeding this voltage into a squared/divider circuit ( $1/V^2$  corrector) and providing the resulting signal to the multiplier that generates the current reference for the inner current control loop.

In this way, a change of the line voltage causes an inversely-proportional change of the half sine amplitude at the output of the multiplier (if the line voltage doubles the amplitude of the multiplier, the output is halved and vice versa) so that the current reference is adapted to the new operating conditions with (ideally) no need for invoking the slow dynamics of the error amplifier. Additionally, the loop gain is constant throughout the input voltage range, which improves significantly dynamic behavior at low line and simplifies loop design.

Actually, with other PFCs embedding the voltage feed-forward, deriving a voltage proportional to the RMS line voltage implies a form of integration, which has its own time constant. If it is too small, the voltage generated is affected by a considerable amount of

ripple at twice the mains frequency that causes distortion of the current reference (resulting in high THD and poor PF). If it is too large, there is a considerable delay in setting the right amount of feed-forward, resulting in excessive overshoot and undershoot of the pre-regulator's output voltage in response to large line voltage changes. Clearly a trade-off was required.

The L6564 implements an innovative voltage feed-forward which, with a technique that makes use of just two external parts, overcomes this time constant trade-off issue whichever voltage change occurs on the mains (either a surge or drop). A capacitor  $C_{FF}$  and a resistor  $R_{FF}$  both connected from the pin  $V_{FF}$  (pin #5) to ground, complete an internal peak-holding circuit that provides a DC voltage equal to the peak of the rectified sine wave applied on pin MULT (pin #3). In this way, in case of a sudden line voltage rise,  $C_{FF}$  is rapidly charged through the low impedance of the internal diode. In case of a line voltage drop, an internal "mains drop" detector enables a low impedance switch which suddenly discharges  $C_{FF}$  avoiding a long settling time before reaching the new voltage level. Consequently, an acceptably low steady-state ripple and low current distortion can be achieved without any considerable undershoot or overshoot on the pre-regulator's output like in systems with no feed-forward compensation.

**Figure 18. L6562A input mains surge 90 Vac to 140 Vac – no  $V_{FF}$  input**      **Figure 19. EVL6564 100W TM PFC: input mains surge 90 Vac to 140 Vac  $C_{FF} = 1 \mu F, R_{FF} = 1 M\Omega$**

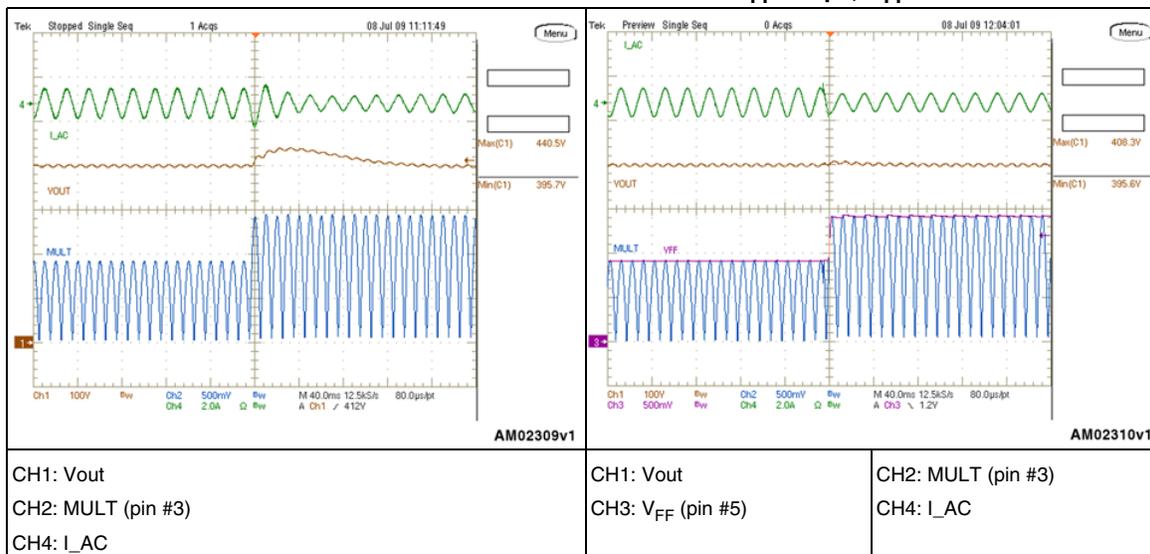


Figure 19 shows the behavior of the EVL6564-100W demonstration board in case of an input voltage surge from 90 to 140Vac. In the diagram it is evident that the  $V_{FF}$  function provides for the stability of the output voltage which is not affected by the input voltage surge. In fact, thanks to the  $V_{FF}$  function, the compensation of the input voltage variation is very fast and the output voltage remains stable at its nominal value. The opposite is confirmed in Figure 18 which shows the behavior of a PFC using the L6562A and delivering the same output power. The controller cannot compensate a mains surge and the output voltage stability is guaranteed by the feedback loop only. Unfortunately, as previously stated, its bandwidth is narrow and thus the output voltage has a significant deviation from the nominal value. The circuit has the same behavior in case of a mains surge at any input

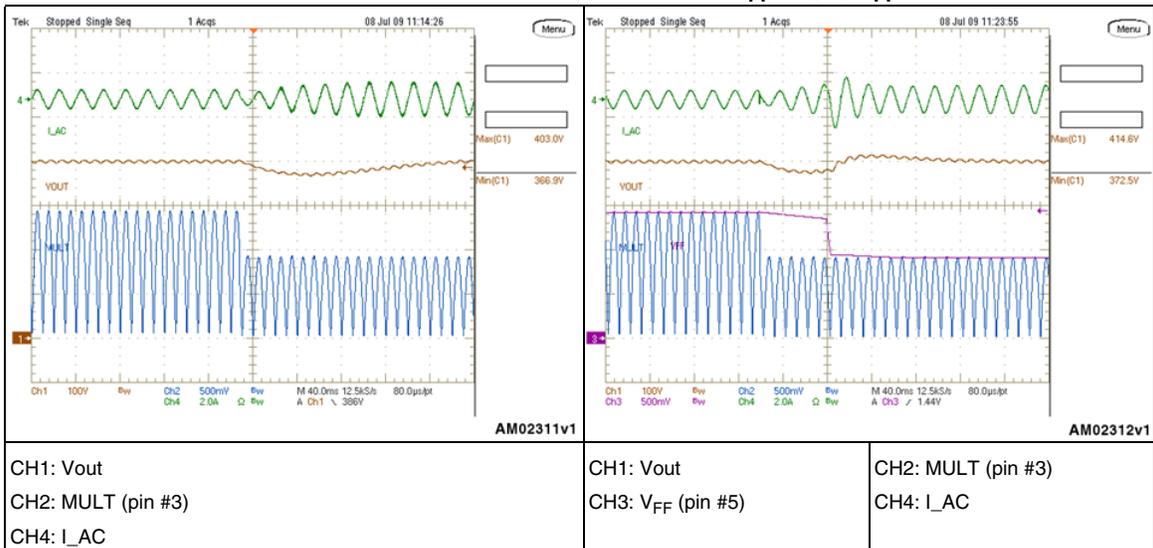
voltage, and it is not affected if the input mains surge happens at any point on the input sine wave.

Figure 21 shows the circuit behavior for a mains dip. As previously described, the internal circuitry has detected the decrease of the mains voltage and it has activated the  $C_{FF}$  internal fast discharge. As visible, in that case, the output voltage changes but in a few mains cycles it comes back to the nominal value. The situation is different if we check the performance of a controller without the  $V_{FF}$  function. Figure 20 shows the behavior of a PFC using the L6562A delivering similar output power. For a mains dip from 140 Vac to 90 Vac, the output voltage fluctuation is not very different, but the output voltage requires a longer time to restore the original value.

Testing with a wider voltage variation (e.g. 265 Vac to 90 Vac), the output voltage fluctuation of a PFC without the voltage feed-forward fast discharging is amplified and it requires more time to recover its original set value (400 V).

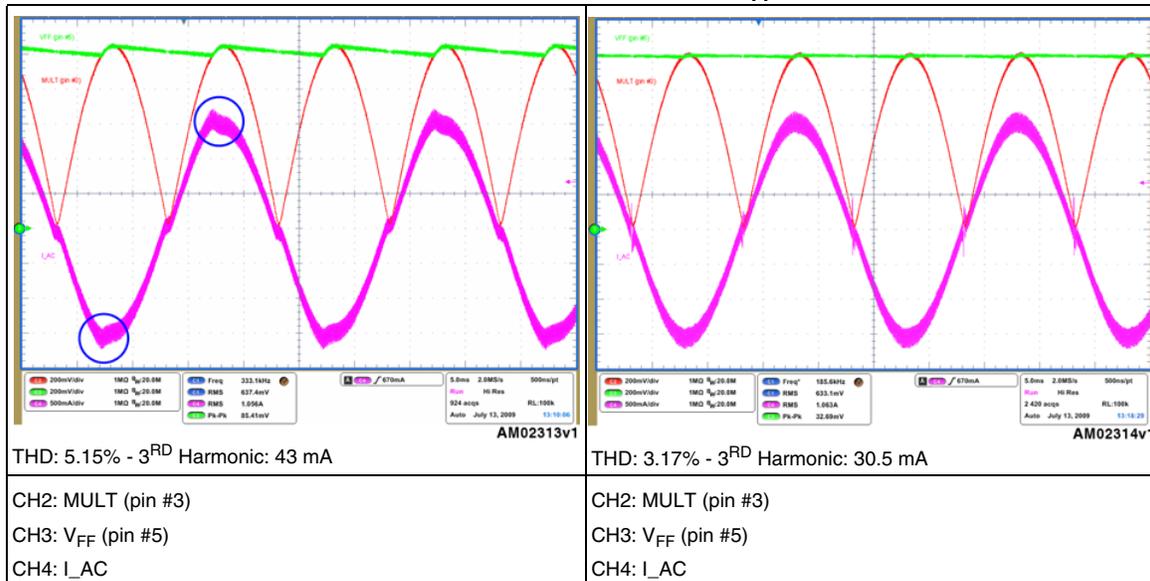
Figure 20. L6562A input mains dip 140 Vac to 90 Vac – no  $V_{FF}$  input

Figure 21. EVL6564-100W TM PFC: Input mains dip 140 Vac to 90 Vac  $C_{FF} = 1\mu F, R_{FF} = 1 M\Omega$



Comparing *Figure 22* and *Figure 23* we can see that the input current of *Figure 23* has a better shape and the 3<sup>rd</sup> harmonic current distortion is not noticeable. This demonstrates the benefits of the new voltage feed-forward circuit integrated in the L6564, allowing to get a fast response to mains disturbances but using a quite long  $V_{FF}$  time constant provides also very low THD and high PF at the same time as confirmed by the measurements below the waveforms.

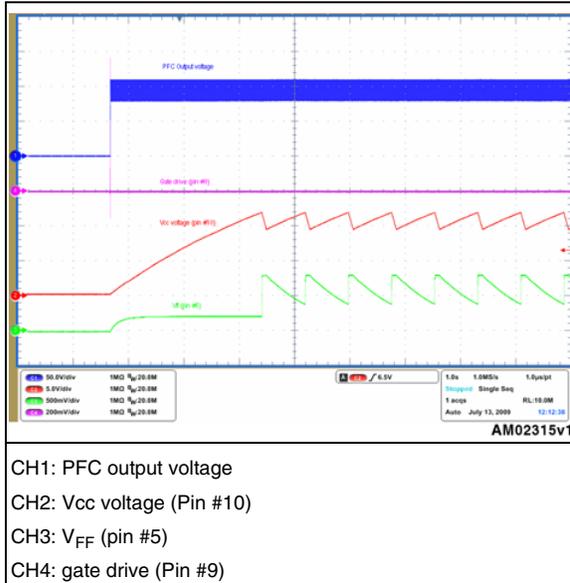
**Figure 22. L6563 input current at 100 Vac-50Hz** **Figure 23. EVL6564-100W TM PFC: input current at 100 Vac-50Hz**  
 $C_{FF} = 0.47 \mu F, R_{FF} = 390 k\Omega$   $C_{FF} = 1 \mu F, R_{FF} = 1 M\Omega$



Another function integrated in the L6564 is the brownout protection which is basically a non-latched shutdown function that must be activated when a mains undervoltage condition is detected. This abnormal condition may cause overheating of the primary power section due to an excess of RMS current. Brownout can also cause the PFC pre-regulator to work in open loop and this could be dangerous to the PFC stage itself and the downstream converter, should the input voltage return abruptly to its rated value. Another problem is the spurious restarts that may occur during converter power-down which cause the output voltage of the converter to not decay to zero monotonically. For these reasons it is usually preferable to shut down the unit in case of brownout.

Brownout thresholds are set internally at 0.88 V (typ.) for enabling and 0.8 V (typ.) for disabling the L6564. Sensing of the input mains condition is done by an internal comparator connected to pin V<sub>FF</sub> (pin #5) which delivers a voltage signal proportional to the input mains.

**Figure 24. EVL6564-100W startup attempt at 80 Vac - 60 Hz – full load**



Because in the L6564 the brownout thresholds are set internally, the startup and shutdown thresholds can be adjusted slightly by modifying the resistor values used for the MULT pin. In [Figure 24](#) a startup tentative below the startup threshold is captured. As shown at startup the brownout function does not allow the PFC startup even if Vcc has reached the L6564 turn-on threshold.

[Figure 25](#) and [Figure 26](#) show the circuit waveforms during brownout protection. In both cases the mains voltage were increased or decreased slowly. As visible at turn-on or at turn-off there are no bouncing or starting attempts by the PFC converter.

Figure 25. EVL6564-100W startup with slow input voltage increasing – full load

Figure 26. EVL6564-100W turn-off with slow input voltage decreasing – full load

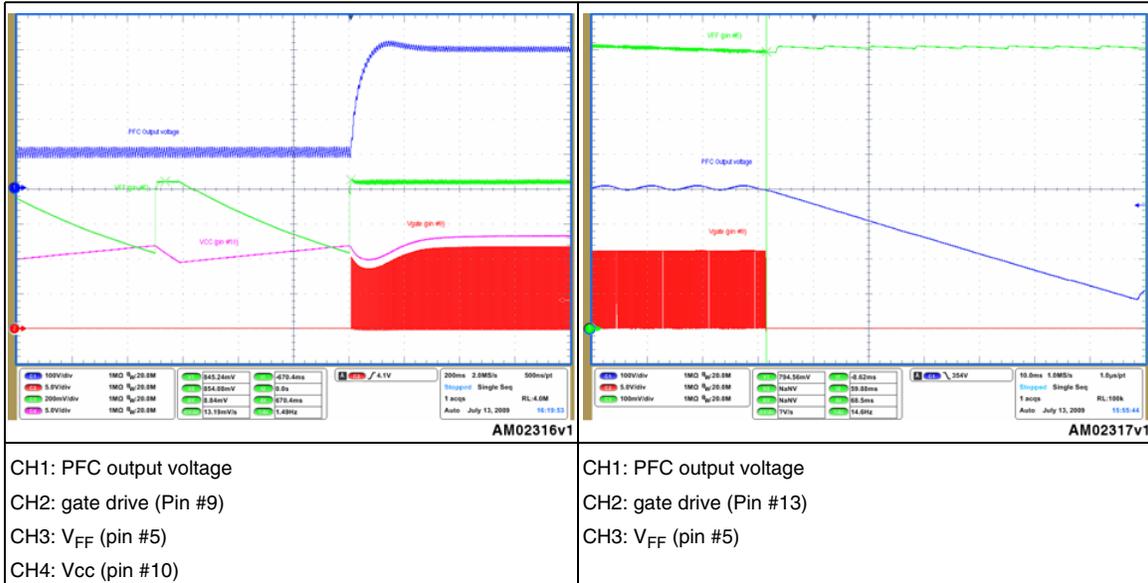
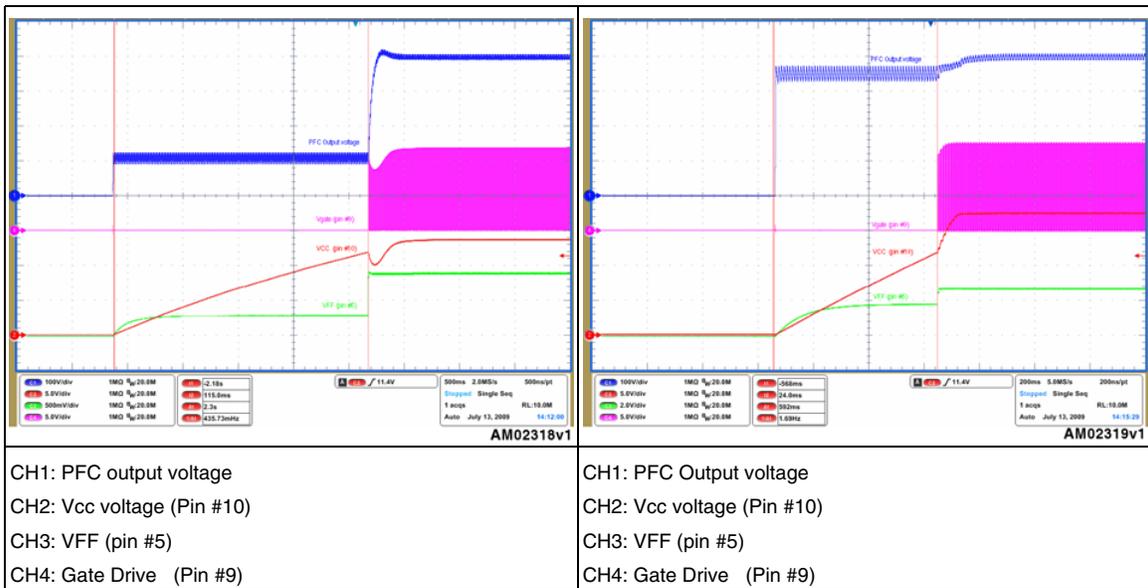


Figure 27 and Figure 28 show the waveforms during the startup of the circuit at mains plug-in. We can notice that the V<sub>cc</sub> voltage rises up to the turn-on threshold, and the L6564 starts operating. For a short time the energy is supplied by the V<sub>cc</sub> capacitor, and then the auxiliary winding with the charge pump circuit takes over. At the same time, the output voltage rises from the peak value of the rectified mains to the nominal value of the PFC output voltage. The good margin phase of the compensation network allows a clean startup, without any large overshoot.

Figure 27. EVL6564-100W startup at 90 Vac -60 Hz – full load

Figure 28. EVL6564-100W startup at 265 Vac-50 Hz – full load



### 3.4 PFC\_OK pin and feedback failure (open loop) protection

During normal operation, the voltage control loop provides for the output voltage ( $V_{out}$ ) of the PFC pre-regulator close to its nominal value, set by the resistors ratio of the feedback output divider. In the L6564, a pin of the device (PFC\_OK, pin #6) has been dedicated to monitor the output voltage with a separate resistor divider composed of R3, R4, R11 (high) and R15 (low), see [Figure 1](#). This divider is selected so that the voltage at the pin reaches 2.5 V if the output voltage exceeds a preset value ( $V_{ovp}$ ), usually larger than the maximum  $V_{out}$  that can be expected, also including worst-case load/line transients.

For the EVL6564-100W we have:

$$V_o = 400 \text{ V}, V_{ovp} = 434 \text{ V}.$$

$$\text{Select: } R_3+R_4+R_{11}=8.8\text{MW};$$

$$\text{then: } R_{15} = 8.8 \text{ M}\Omega \cdot 2.5 / (434-2.5) = 51 \text{ k}\Omega.$$

Once this function is triggered, the gate drive activity is immediately stopped until the voltage on the pin PFC\_OK drops below 2.4 V, see an example in [Figure 29](#).

Notice that both feedback dividers connected to L6564 pin #1 (INV) and pin #6 (PFC\_OK) can be selected without any constraints. The unique criterion is that both dividers have to sink a current from the output bus which needs to be significantly higher than the current biasing the error amplifier and PFC\_OK comparator.

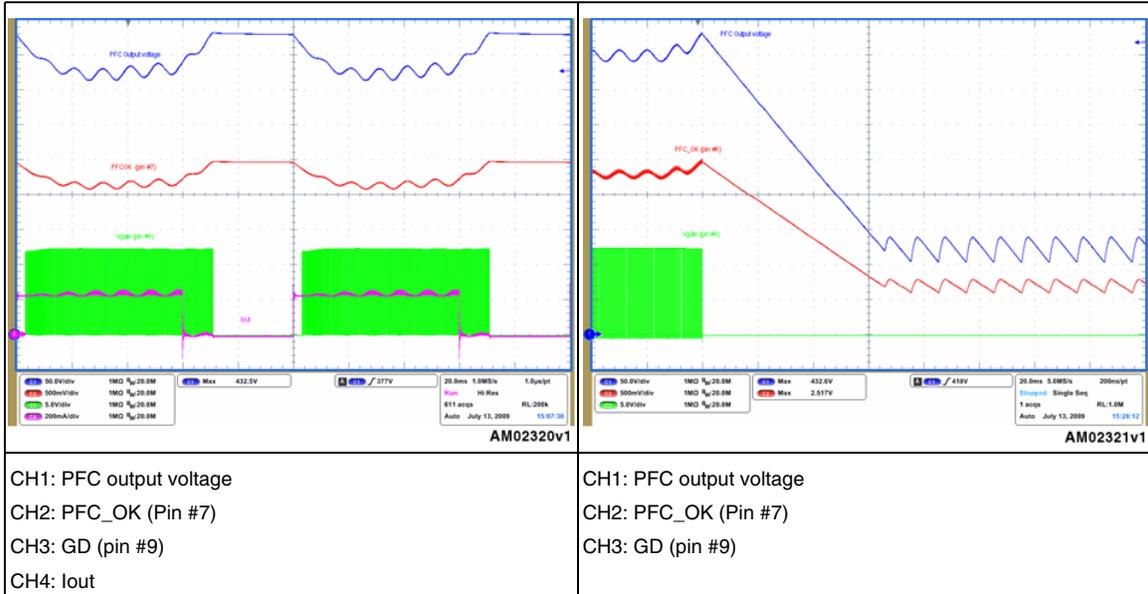
The OVP function described above is able to handle “normal” overvoltage conditions, i.e. those resulting from an abrupt load/line change or occurring at startup. In case the overvoltage is generated by a feedback disconnection, for instance, when one of the upper resistors of the output divider fails open, an additional circuitry behind the pin PFC\_OK detects the voltage gap with respect to pin INV. If the voltage gap is greater than 40 mV and the OVP is active, the feedback failure protection is triggered. Thus, the gate drive activity is immediately stopped, the device is shut down, its quiescent consumption is reduced below 180  $\mu\text{A}$  and the condition is latched as long as the supply voltage of the IC is above the UVLO threshold. To restart the system it is necessary to recycle the input power, so that the  $V_{cc}$  voltage of the L6564 goes below 6 V and that one of the PWM controller goes below its UVLO threshold.

Note that this function offers a complete protection against not only feedback loop failures or erroneous settings, but also against a failure of the protection itself. Either resistor of the PFC\_OK divider failing short or open or a PFC\_OK pin floating results in shutting down the IC and stopping the pre-regulator.

Moreover, the pin PFC\_OK doubles its function as a non-latched IC disable. A voltage below 0.23 V shuts down the IC, reducing its consumption below 2 mA. To restart the IC, simply let the voltage at the pin go above 0.27 V.

Figure 29. EVL6564-100W load transient at 115 Vac - 60 Hz - full load to no load

Figure 30. EVL6564-100W open loop at 115 Vac - 60 Hz - full load



The event of an open loop is captured in [Figure 30](#), we can notice the protection intervention latching the operation of the L6564.

## 4 Power management and housekeeping functions

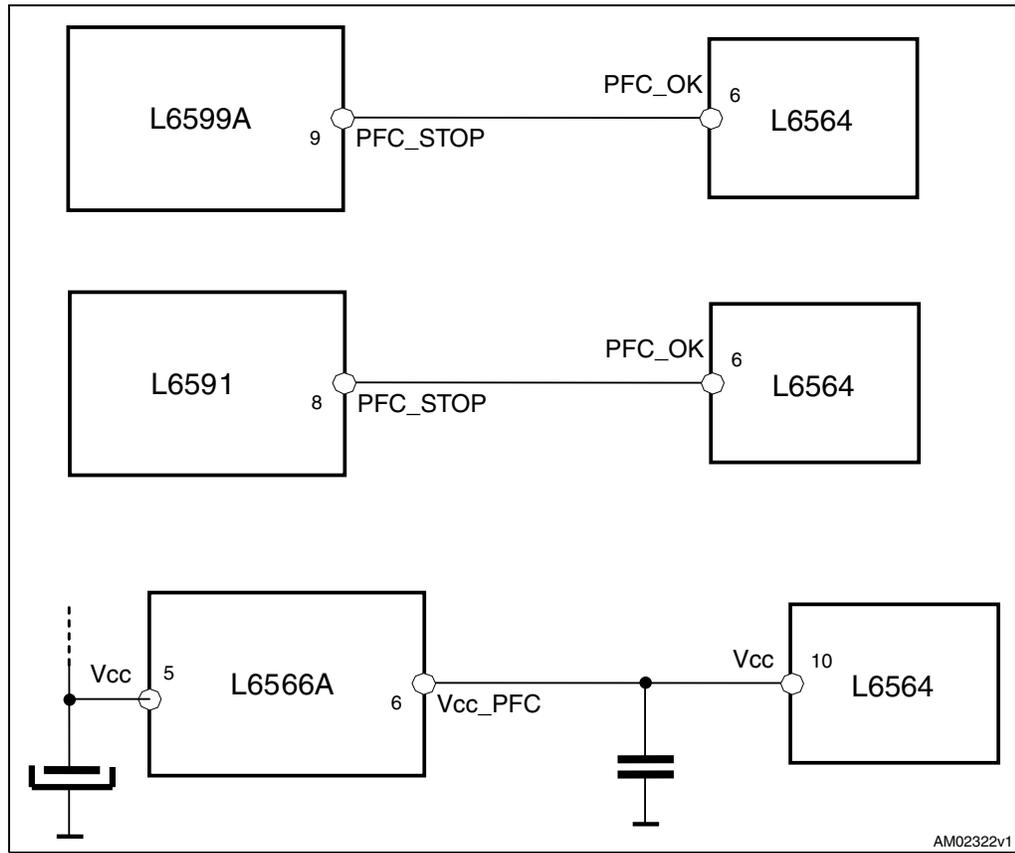
Unlike similar PFC controllers with more pins, the housekeeping functions of the L6564 are minimized but still there, and the device, in spite of the low pin count, has some main functionalities that make it suitable to be implemented in high-end applications.

For example, in order to save power during light load operation or to put the converter in a safe condition after detecting a failure of the DC-DC converter, a communication line can be established between the cascade converter and the PFC via the disable function included in the PFC\_OK pin (pin #6). Needless to say, this operation assumes that the cascaded PFC converter stage works as the master (thanks also to the integrated brownout function) and the DC-DC stage as the slave or, in other words, that the PFC stage starts first, it powers both controllers and enables/disables the operation of the downstream converter stage. Several PWM controllers by STMicroelectronics have integrated some housekeeping functions for the D2D and offer the possibility to interface directly the L6564 with the downstream PWM controller via dedicated pins.

Should the residual consumption of the chip be an issue, it is also possible to cut off the supply voltage. In this case, this operation assumes that the cascaded DC-DC converter stage works as the master and the PFC stage as the slave or, in other words, that the DC-DC stage starts first, it powers both controllers and enables/disables the operation of the PFC stage.

The EVL6564-100W offers the possibility to test the disable function by connecting it to the cascaded DC-DC converter using the J3 connector. The PFC\_OK pin, Vcc and ground are available via the series resistors R30 and R31.

Figure 31. Interface circuits that let DC-DC converter's controller IC disable the L6564



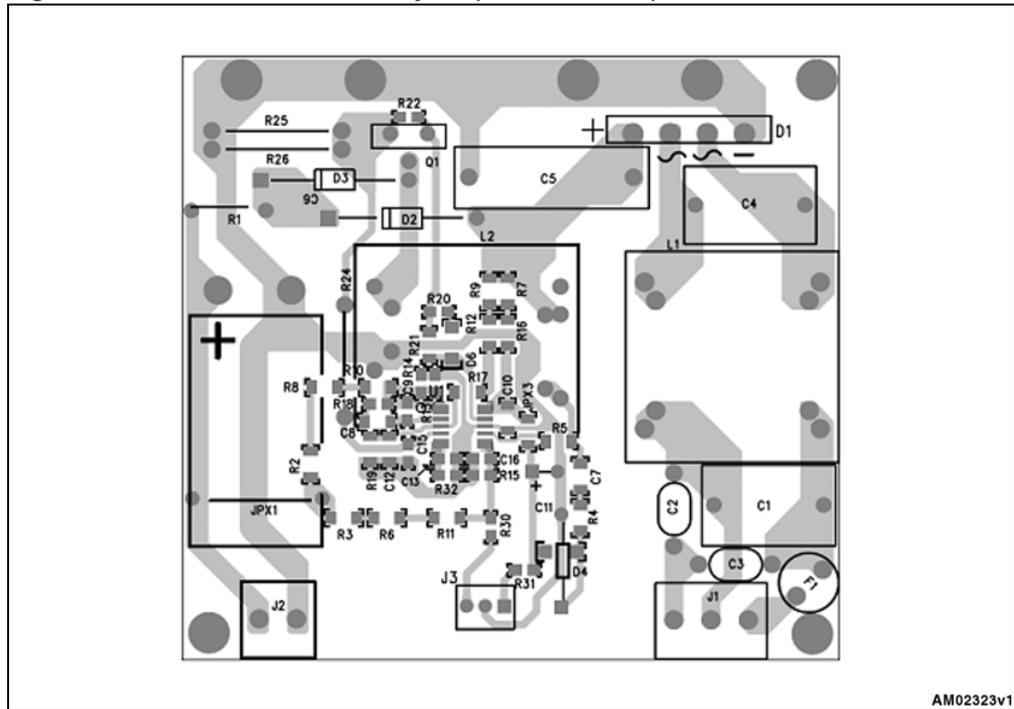
## 4.1 Layout hints

The layout of any converter is a very important phase in the design process needing attention by the design engineers like any other design phase. Even if it the layout phase sometimes looks time-consuming, a good layout does indeed save time during the functional debugging and the qualification phases. Additionally, a power supply circuit with a correct layout needs smaller EMI filters or less filter stages and which allows consistent cost savings.

Converters using the L6564 do not need any special or specific layout rule to be followed, just the general layout rules for any power converter have to be applied carefully. Basic rules are listed here below which can be used for other PFC circuits having any power level, working either in transition mode or with a fixed-off time control.

1. Keep power and signal RTN separated. Connect the return pins of components carrying high current such as the input filter, sense resistors, and output capacitor as close as possible. This point is the RTN star point. A downstream converter must be connected to this return point.
2. Minimize the length of the traces relevant to the boost inductor, MOSFET drain, boost rectifier and output capacitor.
3. Keep signal components as close as possible to each relevant pin of the L6564. Specifically, keep the tracks relevant to pin #1 (INV) as short as possible. Components and traces relevant to the error amplifier have to be placed far from traces and connections carrying signals with high  $dV/dt$  like the MOSFET drain.
4. Please connect heat sinks to power GND.
5. Add an external shield to the boost inductor and connect it to power GND.
6. Please connect the RTN of signal components including the feedback, PFC\_OK and MULT dividers close to the L6564 pin #8 (GND).
7. Connect a ceramic capacitor (100 - 470 nF) to pin #10 (Vcc) and to pin #8 (GND), close to the L6564. Connect this point to the RTN star point (see rule 1).

Figure 32. EVL6564-100W PCB layout (SMT side view)



## 5 EMI filtering and conducted EMI pre-compliance measurements

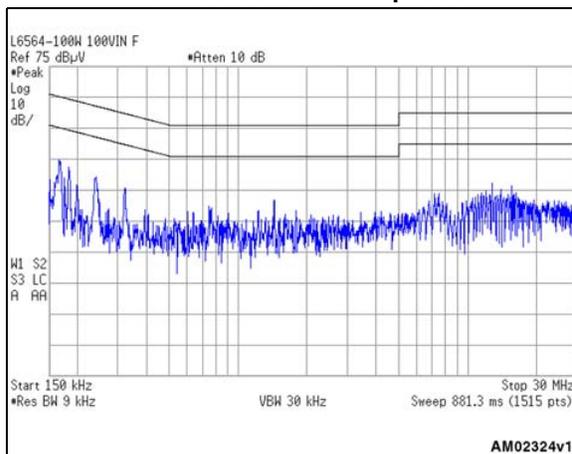
The following figures show the peak measurement of the conducted noise at full load and nominal mains voltages for both mains lines. The limits shown in the diagrams are EN55022 class-B which is the most popular regulation for domestic equipments using a two-wire mains connection.

It is also useful to remind that typically a PFC produces a significant differential mode noise with respect to other topologies and therefore in case an additional margin with respect to the limits is required, we suggest trying to increase the across-the-line (X) capacitors or the capacitor C5 after the rectifier bridge. This is more effective and cheaper than increasing the size of the common mode filter coil that in this case would filter the differential mode noise by the leakage inductance between the two windings only.

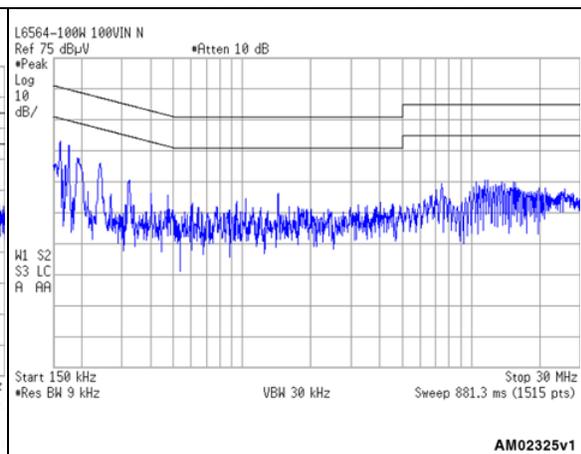
In order to recognize if the circuit is affected by common mode or differential mode noise, it is sufficient to compare the spectrum of phase and neutral line measurements. If the two measurements are very similar, the noise is almost totally common mode. If there is a significant difference between the two measurement spectrums, their difference represents the amount of differential mode noise. Of course to get a reliable comparison the two measurements have to be done under the same conditions. If the peak measurement is used (as in the following figures), some countermeasures must be used, like synchronizing the sweep of the spectrum analyzer with the input voltage. This is necessary as TM PFC has a switching frequency that is modulated along the sine wave.

Because the differential mode produces the common mode noise by the magnetic field induced by the current, decreasing the differential mode consequently limits the common mode.

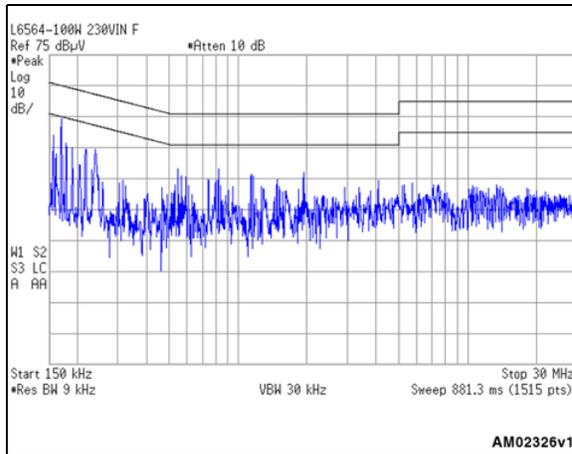
**Figure 33. EVL6564-100W conducted emission peak measurement at 100Vac - 50Hz FL phase**



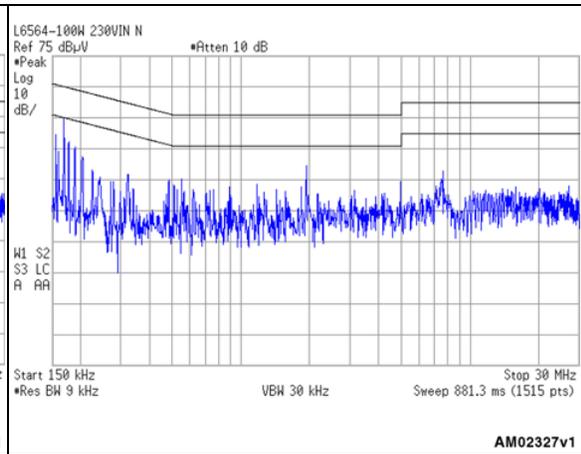
**Figure 34. EVL6564-100W conducted emission peak measurement at 100Vac - 50Hz FL neutral**



**Figure 35. EVL6564-100W conducted emission peak measurement at 230Vac - 50Hz FL phase**



**Figure 36. EVL6564-100W conducted emission peak measurement at 230Vac - 50Hz FL neutral**



As visible in the diagrams, in all test conditions there is a good margin of the measures with respect to the limits. The measurements have been done in peak detection to speed up the sweep, otherwise taking a long time. Please note that the harmonic measurements done in quasi-peak or average as required by the regulation will be much lower because of the jittering effect of the TM control that cannot be perceived in peak detection.

## 6 PFC coil specifications

### 6.1 General description and characteristics

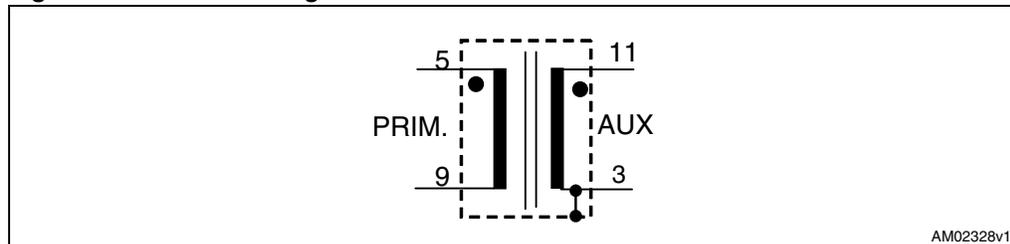
- Applications: consumer, home appliance
- Transformer: open
- Coil former: vertical, 6+6 pins
- Max. temp. rise: 45 °C
- Max. operating ambient temp.: 60 °C
- Mains insulation: N.A.
- Unit finishing: varnish

### 6.2 Electrical characteristics

- Converter topology: boost, transition mode
- Core: PQ26/20 – PC44
- Min. operating frequency: 40 kHz
- Typical operating frequency: 20 kHz
- Primary inductance: 520 mH  $\pm$ 10% at 1 kHz – 0.25 V <sup>(a)</sup>
- Peak primary current 4.2 A<sub>PK</sub>
- RMS primary current 1.4 A<sub>RMS</sub>

### 6.3 Electrical diagram

Figure 37. Electrical diagram



a. Measured between pins #5 & #9

## 6.4 Winding characteristics

**Table 2. Winding characteristics**

Pins	Winding	RMS current	Number of turns	Wire type
5 - 9	Primary <sup>(1)</sup>	1.4 A <sub>RMS</sub>	57.5 - FIT	Multi stranded #7 x $\phi$ 0.20 mm
11 - 3	AUX <sup>(2)</sup>	0.05 A <sub>RMS</sub>	5.5 - spaced	$\phi$ 0.28 mm

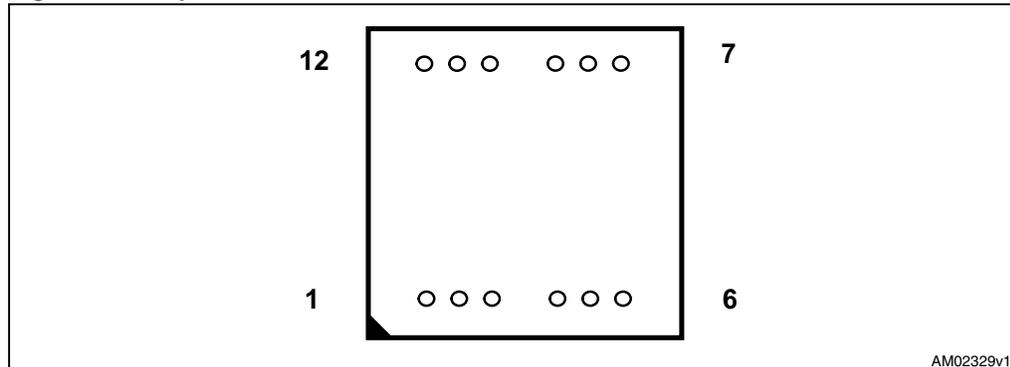
1. Primary winding external insulation: 2 layers of polyester tape

2. Aux. winding is wound on top of primary winding. External insulation with 2 layers of polyester tape

## 6.5 Mechanical aspect and pin numbering

- Maximum height from PCB: 21.5 mm
- Coil former: vertical, 6+6 pins
- TDK P/N: BPQ26/20-1112CP
- Pins #1, 2, 4, 6, 7, 10, 12 are removed. Pin 8 is for polarity key.
  - External copper shield: not insulated, wound around the ferrite core, including the coil former. It must be well adhered to the ferrite. Height is 8 mm. Connected to pin #3 by a soldered, solid wire.

**Figure 38. Top view**



## 6.6 Unit identification

- Manufacturer: TDK
- Manufacturer P/N: SRW2620PQ-X22V102

## 7      **References**

- “10-pin transition-mode PFC controller” L6564 datasheet
- “How to design a TM PFC pre-regulator with the L6564” application note AN3009

## 8 Revision history

Table 3. Document revision history

Date	Revision	Changes
18-Nov-2009	1	Initial release

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