MJB41C (NPN), MJB42C (PNP)

Preferred Devices

Complementary Silicon Plastic Power Transistors

D^2PAK for Surface Mount

Features

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Electrically the Same as TIP41 and T1P42 Series
- Pb−Free Packages are Available

ON Semiconductor®

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COMPLEMENTARY SILICON POWER TRANSISTORS 6 AMPERES, 100 VOLTS, 65 WATTS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	100	Vdc
Collector−Base Voltage	V_{CB}	100	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current − Continuous − Peak	I_C	6.0 10	Adc
Base Current	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 65 0.52	 W W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	 2.0 0.016	 W W/°C
Unclamped Inductive Load Energy (Note 1)	E	62.5	mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

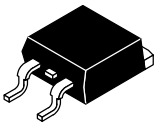
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction−to−Ambient (Note 2)	$R_{\theta JA}$	50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 Seconds	T_L	260	°C

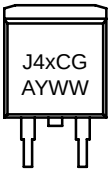
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. I_C = 2.5 A, L = 20 mH, P.R.F. = 10 Hz, V_{CC} = 10 V, R_{BE} = 100 Ω
2. When surface mounted to an FR−4 board using the minimum recommended pad size.

MARKING DIAGRAM



D^2PAK
CASE 418B
STYLE 1



J4xC = Specific Device Code
x = 1 or 2
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
MJB41C	D^2PAK	50 Units/Rail
MJB41CG	D^2PAK (Pb−Free)	50 Units/Rail
MJB41CT4	D^2PAK	800/Tape & Reel
MJB41CT4G	D^2PAK (Pb−Free)	800/Tape & Reel
MJB42C	D^2PAK	50 Units/Rail
MJB42CG	D^2PAK (Pb−Free)	50 Units/Rail
MJB42CT4	D^2PAK	800/Tape & Reel
MJB42CT4G	D^2PAK (Pb−Free)	800/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 3) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	−	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0)	I_{CEO}	−	0.7	mAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, V_{EB} = 0)	I_{CES}	−	100	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	−	50	μAdc
ON CHARACTERISTICS (Note 3)				
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	30 15	− 75	−
Collector−Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 600 mAdc)	$V_{CE(sat)}$	−	1.5	Vdc
Base−Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	−	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain − Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	3.0	−	MHz
Small−Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	20	−	−

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

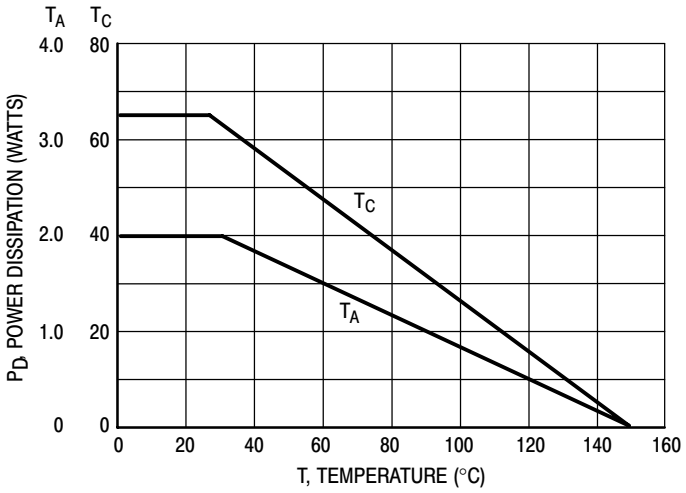
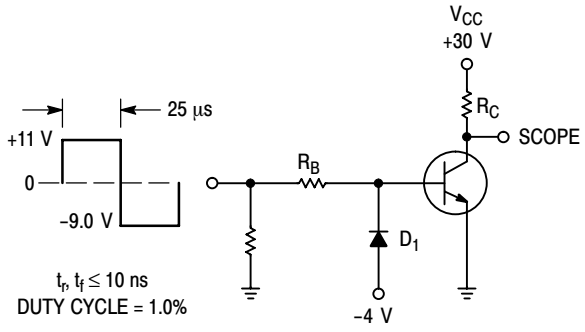


Figure 1. Power Derating



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA

Figure 2. Switching Time Test Circuit

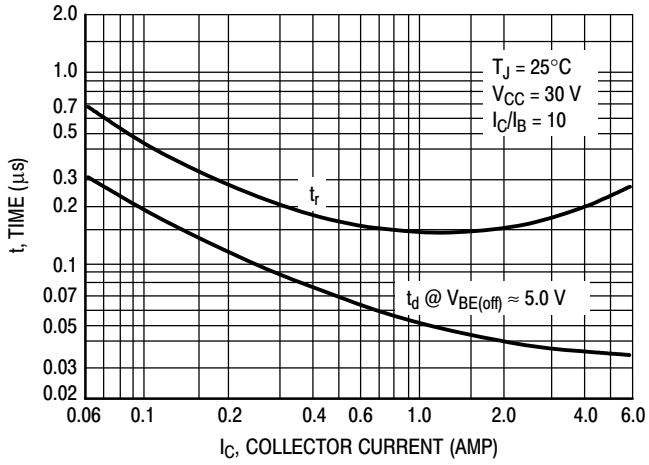


Figure 3. Turn−On Time

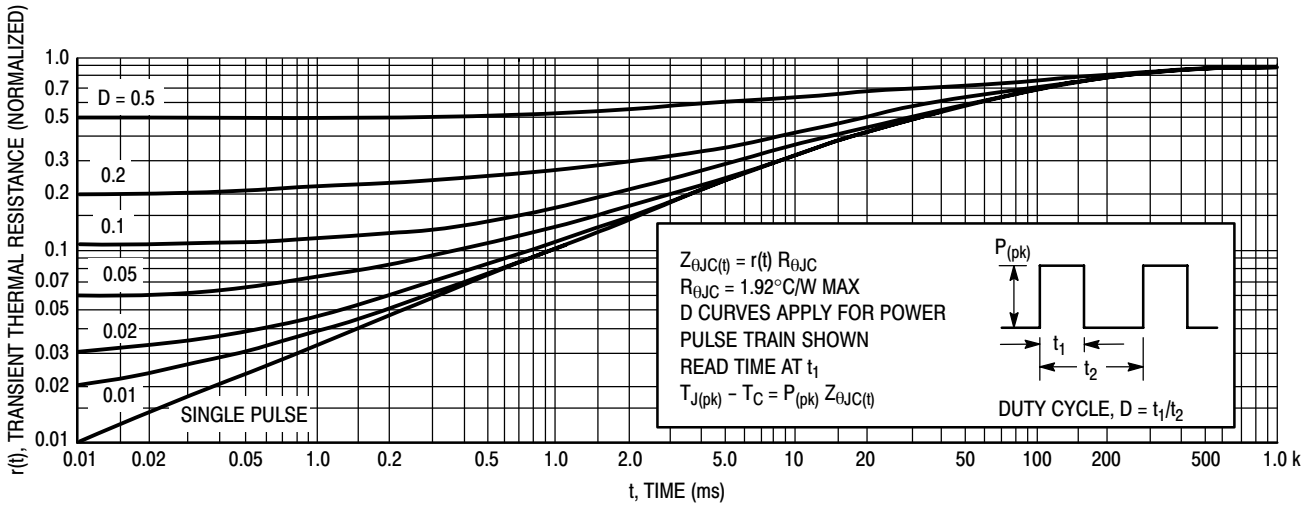


Figure 4. Thermal Response

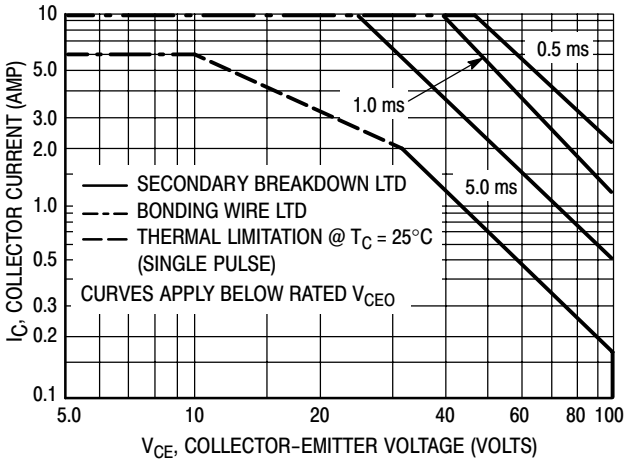


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

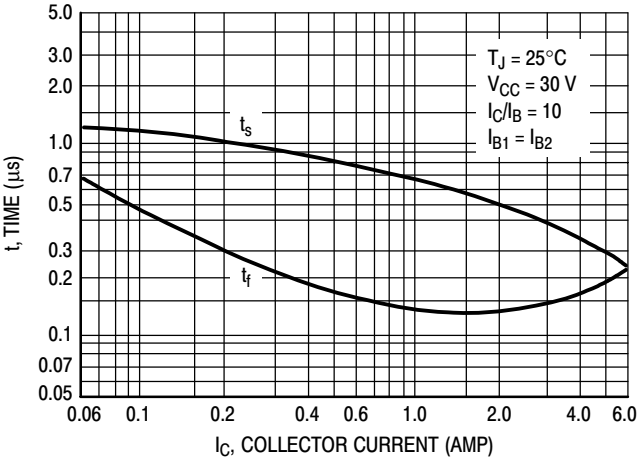


Figure 6. Turn−Off Time

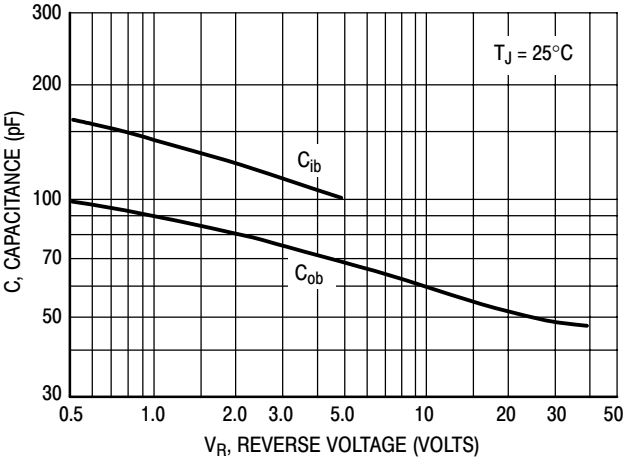


Figure 7. Capacitance

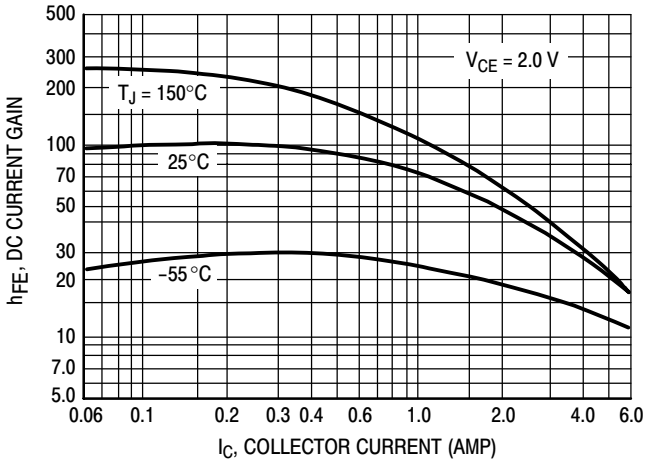


Figure 8. DC Current Gain

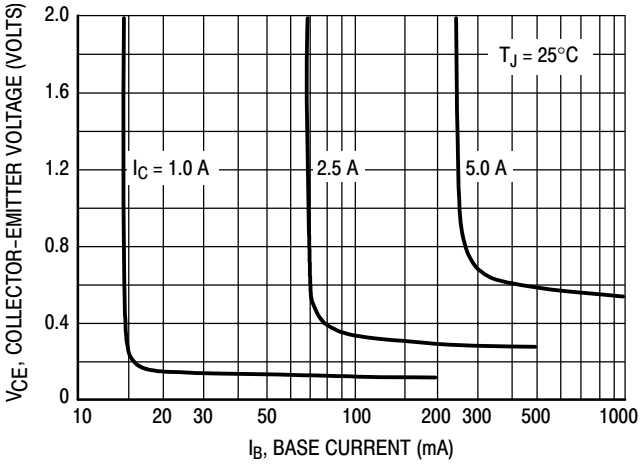


Figure 9. Collector Saturation Region

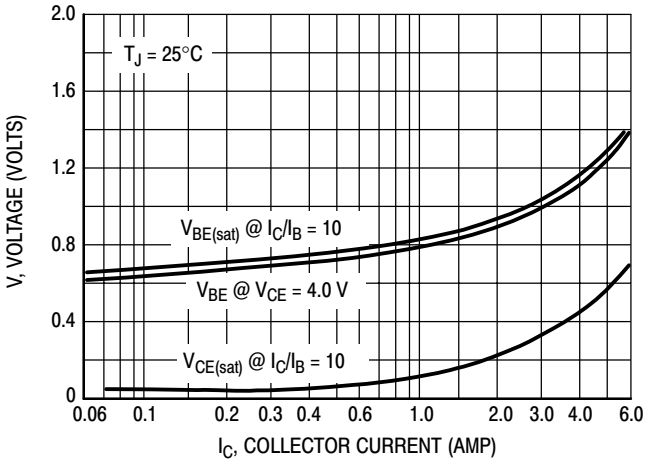


Figure 10. “On” Voltages

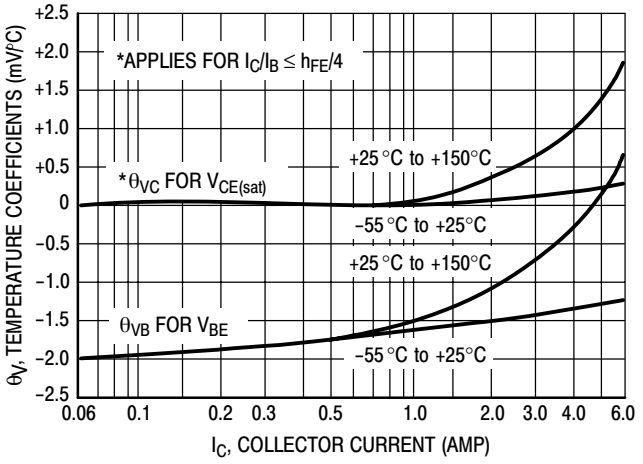


Figure 11. Temperature Coefficients

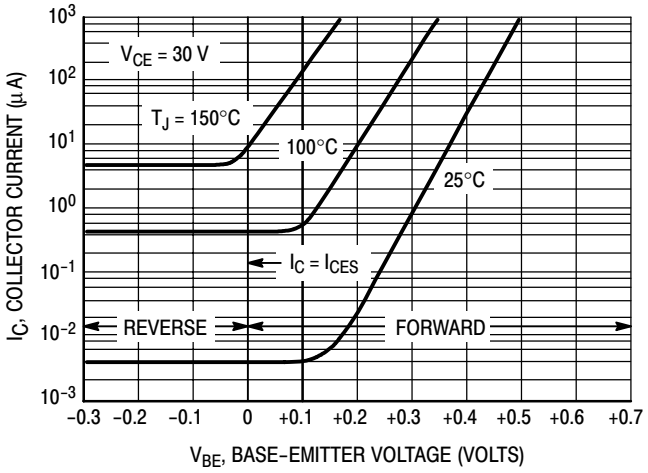


Figure 12. Collector Cut−Off Region

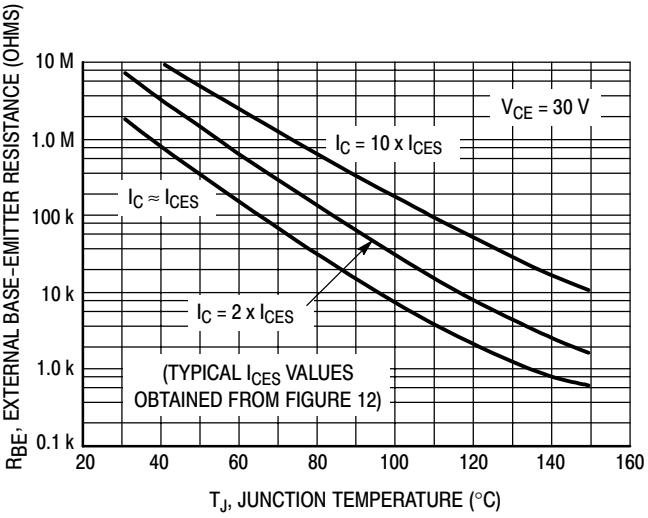
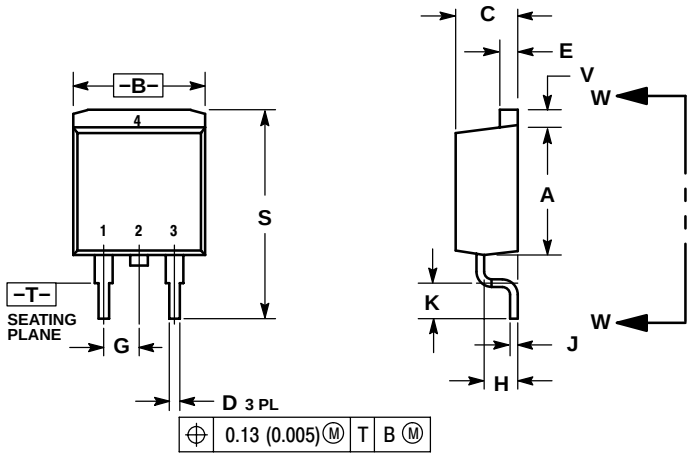


Figure 13. Effects of Base−Emitter Resistance

PACKAGE DIMENSIONS

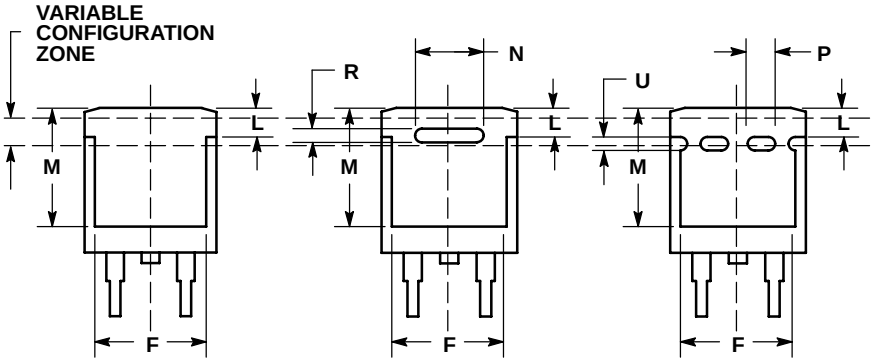
D²PAK 3
CASE 418B−04
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B−01 THRU 418B−03 OBSOLETE, NEW STANDARD 418B−04.

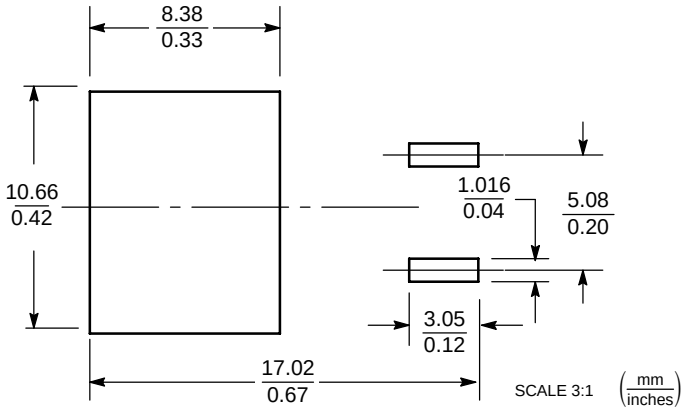
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



VIEW W−W 1 | VIEW W−W 2 | VIEW W−W 3

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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