

### HD1750JL

# Very high voltage NPN power transistor for high definition and slim CRT display

PRELIMINARY DATA

#### **Features**

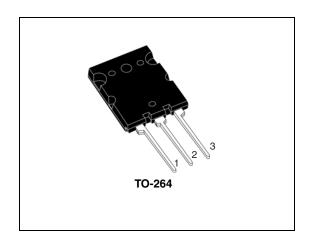
- State-of-the-art technology: diffused collector "enhanced generation" EHVS1
- Wider range of optimum drive conditions
- Less sensitive to operating temperature variation
- In compliance with the 2002/93/EC European directive

#### **Description**

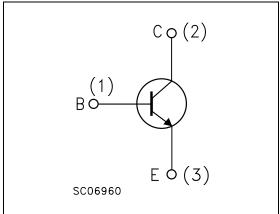
The HD1750JL is manufactured using Diffused Collector in Planar technology adopting new and Enhanced High Voltage Stricture 1 (E.H.V.S.1) developed to fit High-Definition CRT display. The new HD product series show improved silicon efficiency bringing updated performance to the Horizontal Deflection stage.

### **Applications**

■ High-definition and slim CRT TV and monitors



#### Internal schematic diagram



#### Order code

Part number	Marking	Package	Packaging	
HD1750JL	HD1750JL	TO-264	Tube	

February 2007 Rev 3 1/10

Electrical ratings HD1750JL

# 1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>CES</sub>	Collector-emitter voltage (V <sub>BE</sub> = 0)	1700	V
V <sub>CEO</sub>	Collector-emitter voltage (I <sub>B</sub> = 0)	800	٧
V <sub>EBO</sub>	Emitte-base voltage ( $I_C = 0$ )	10	V
I <sub>C</sub>	Collector current	24	Α
I <sub>CM</sub>	Collector peak current (t <sub>P</sub> < 5ms)	36	Α
I <sub>B</sub>	Base current	12	Α
I <sub>BM</sub>	Base peak current (t <sub>P</sub> < 5ms)	18	Α
P <sub>TOT</sub>	Total dissipation at $T_c = 25^{\circ}C$	200	W
T <sub>STG</sub>	Storage temperature	-65 to 150	°C
T <sub>J</sub>	Max. operating junction temperature	150	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJ-C}$	Thermal resistance junction-case max	0.625	°C/W

## 2 Electrical characteristics

(T<sub>CASE</sub>=25°C unless otherwise specified)

Table 3. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I <sub>CES</sub>	Collector cut-off current (V <sub>BE</sub> = 0)	V <sub>CE</sub> = 1700V V <sub>CE</sub> = 1700V; T <sub>C</sub> = 125°C			0.2 2	mA mA
I <sub>EBO</sub>	Emitter cut-off current (I <sub>C</sub> = 0)	V <sub>EB</sub> = 5V			10	μА
V <sub>CEO(sus)</sub> <sup>(1)</sup>	Collector-emitter sustaining voltage (I <sub>B</sub> = 0)	I <sub>C</sub> = 10mA	800			V
V <sub>EBO</sub> <sup>(1)</sup>	Emitter-base saturation voltage (I <sub>C</sub> = 0)	I <sub>E</sub> = 10mA	10			V
V <sub>CE(sat)</sub> <sup>(1)</sup>	Collector-emitter saturation voltage	I <sub>C</sub> = 12A; I <sub>B</sub> = 3A			3	V
V <sub>BE(sat)</sub> <sup>(1)</sup>	Base-emitter saturation voltage	I <sub>C</sub> = 12A; I <sub>B</sub> = 3A		0.95	1.5	V
h <sub>FE</sub>	DC current gain	$I_C = 1A;$ $V_{CE} = 5V$ $I_C = 12A;$ $V_{CE} = 5V$	5.5	30	8.5	
t <sub>s</sub>	Inductive load Storage time Fall time	$\begin{split} I_{C} &= 12A; & I_{B(on)} = 1.8A \\ I_{B(off)} &= -7.25A; \\ V_{CE(fly)} &= 1320V; \\ V_{BE(off)} &= -2.7V; \\ L_{BB(on)} &= 0.8 \mu H; \\ f_{h} &= 31520 Hz \end{split}$		3 300	3.6 450	μs ns
t <sub>s</sub>	Inductive load Storage time Fall time	$\begin{split} I_{C} = 6.5A; & I_{B(on)} = 1.1A \\ I_{B(off)} = -5.25A; \\ V_{CE(fly)} = 1220V; \\ V_{BE(off)} = -2.7V; \\ L_{BB(on)} = 0.25\mu H; \\ f_{h} = 100kHz \end{split}$		1.6 110	2 220	μs ns

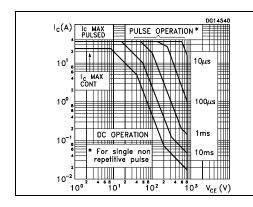
<sup>1.</sup> Pulsed: pulse duration =  $300\mu s$ , duty cycle < 2%

Electrical characteristics HD1750JL

### 2.1 Electrical characteristics (curve)

Figure 1. Safe operating area

Figure 2. Derating curve



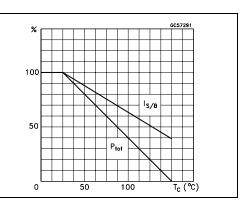
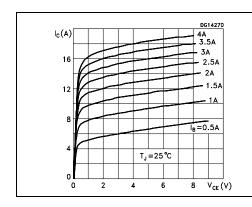


Figure 3. Output characteristics

Figure 4. Reverse biased SOA



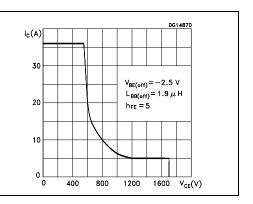
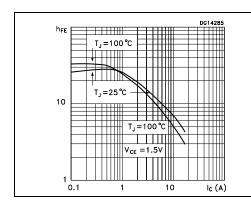


Figure 5. DC current gain

Figure 6. DC current gain



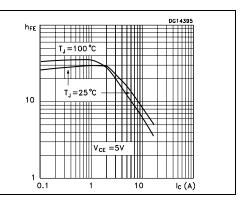


Figure 7. Collector-emitter saturation Figure 8. Base-emitter saturation voltage

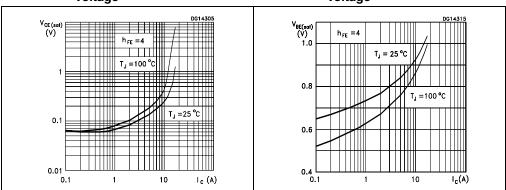


Figure 9. Power losses

Figure 10. Power losses

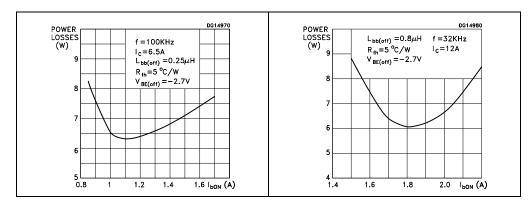
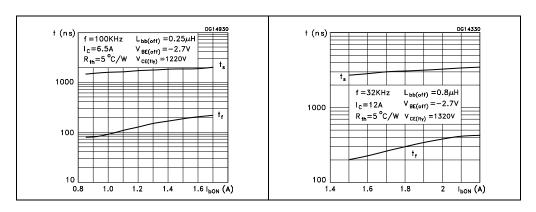


Figure 11. Inductive load switching time Figure 12. Inductive load switching time



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Test circuit HD1750JL

### 3 Test circuit

Figure 13. Power losses and inductive load switching test circuit

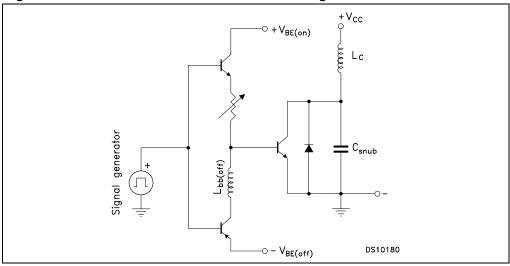
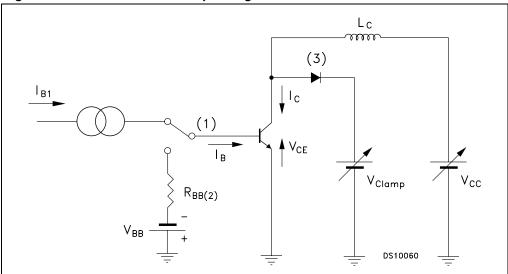


Figure 14. Reverse biased safe operating area test circuit



### 4 Package mechanical data

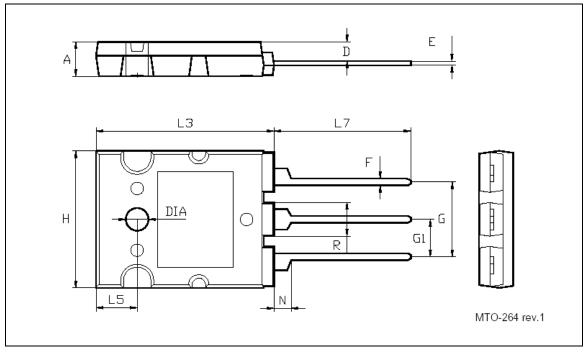
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Table 4. TO-264 Mechanical Data

DIM.	mm.			inch		
DIWI.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
А	4.80		5.20	0.189		0.205
D	2.50		3.10	0.098		0.122
E	0.50	0.60	0.85	0.020	0.24	0.033
F	0.90	1.00	1.25	0.036	0.039	0.049
G	10.30		11.50	0.406		0.453
G1		5.45			0.215	
Н	19.80		20.20	0.780		0.795
L3	25.80		26.20	1.016		1.031
L5	5.80		6.20	0.228		0.244
L7	19.50		20.50	0.768		0.807
N	2.30		2.70	0.091		0.106
R	4.7		5.10	0.185		0.201
DIA	3.10		3.50	0.122		0.138

Figure 15. TO-264 Drawing



HD1750JL Revision history

# 5 Revision history

Table 5. Revision history

Date	Revision	Changes
12-Oct-2006	1	Initial release.
17-Oct-2005	2	Final document
23-Feb-2007	3	The document has been reformatted

Revision history HD1750JL

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