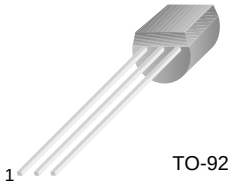
FAIRCHILD SEMICONDUCTOR®

March 2009

# MPSA77
# PNP Darlington Transistor

- This device is designed for applications requiring extremely high current gain at currents to 800mA.
- Sourced from process 61.




TO-92

1. Emitter 2. Base 3. Collector

## Absolute Maximum Ratings * $T_a$=25°C unless otherwise noted

| Symbol | Parameter | | Value | Units |
|---|---|---|---|---|
| $V_{CES}$ | Collector-Emitter Voltage | | -60 | V |
| $V_{CBO}$ | Collector-Base Voltage | | -60 | V |
| $V_{EBO}$ | Emitter-Base Voltage | | -10 | V |
| $I_C$ | Collector Current | - Continuous | -1.2 | A |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | -55 ~ +150 | °C |

* These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

**NOTES:**
1. These ratings are based on a maximum junction temperature of 150 degrees C.
2. These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

## Thermal Characteristics $T_a$=25°C unless otherwise noted

| Symbol | Parameter | Max. | Units |
|---|---|---|---|
| $P_D$ | Total Device Dissipation<br>Derate above 25°C | 625<br>5.0 | mW<br>mW/°C |
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 83.3 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | 200 | °C/W |

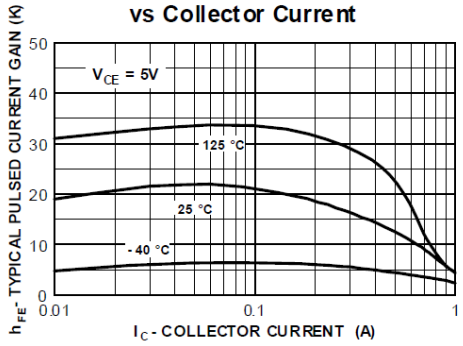
## Electrical Characteristics $T_a$=25°C unless otherwise noted

| Symbol | Parameter | Test Condition | Min. | Max. | Units |
|---|---|---|---|---|---|
| **Off Characteristics** | | | | | |
| $V_{(BR)CES}$ | Collector-Emitter Breakdown Voltage | $I_C$ = -100μA, $I_B$ = 0 | -60 | | V |
| $I_{CBO}$ | Collector Cutoff Current | $V_{CB}$ = -30V, $I_E$ = 0 | | -100 | nA |
| $I_{EBO}$ | Emitter Cutoff Current | $V_{EB}$ = -10V, $I_C$ = 0 | | -100 | nA |
| **On Characteristics *** | | | | | |
| $h_{FE}$ | DC Current Gain | $I_C$ = -10mA, $V_{CE}$ = -5.0V<br>$I_C$ = -100mA, $V_{CE}$ = -5.0V | 10,000<br>10,000 | | |
| $V_{CE}$(sat) | Collector-Emitter Saturation Voltage | $I_C$ = -100mA, $I_B$ = -0.1mA | | -1.5 | V |
| $V_{BE}$(on) | Base-Emitter On Voltage | $I_C$ = -100mA, $V_{CE}$ = -5.0mA | | -2.0 | V |
| **Small Signal Characteristics *** | | | | | |
| $f_T$ | Current Gain Dandwidth Product | $I_C$ = -10mA, $V_{CE}$ = -5.0V<br>f = 100MHz | 100 | | MHz |

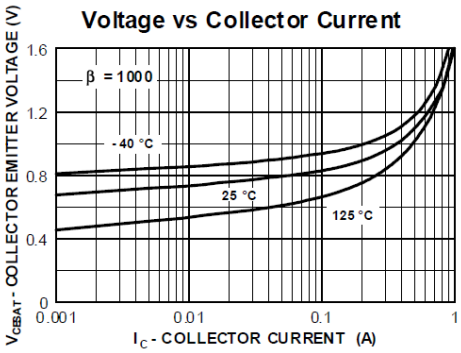
* Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%

## Typical Performance Characteristics

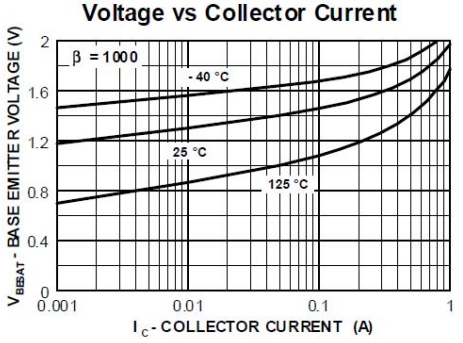
**Typical Pulsed Current Gain vs Collector Current**



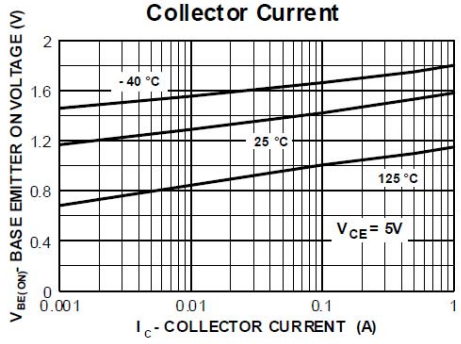

**Collector-Emitter Saturation Voltage vs Collector Current**



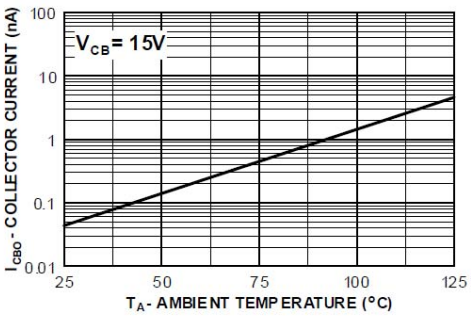

**Base-Emitter Saturation Voltage vs Collector Current**



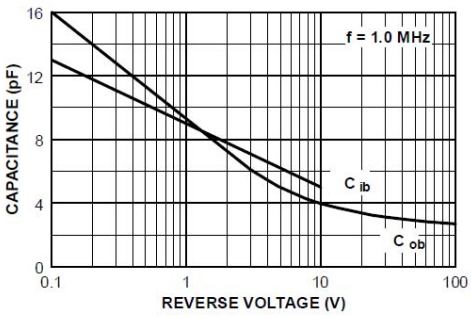

**Base Emitter ON Voltage vs Collector Current**




**Collector-Cutoff Current vs Ambient Temperature**

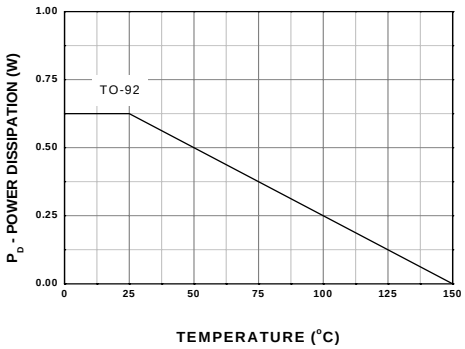



**Input and Output Capacitance vs Reverse Bias Voltage**

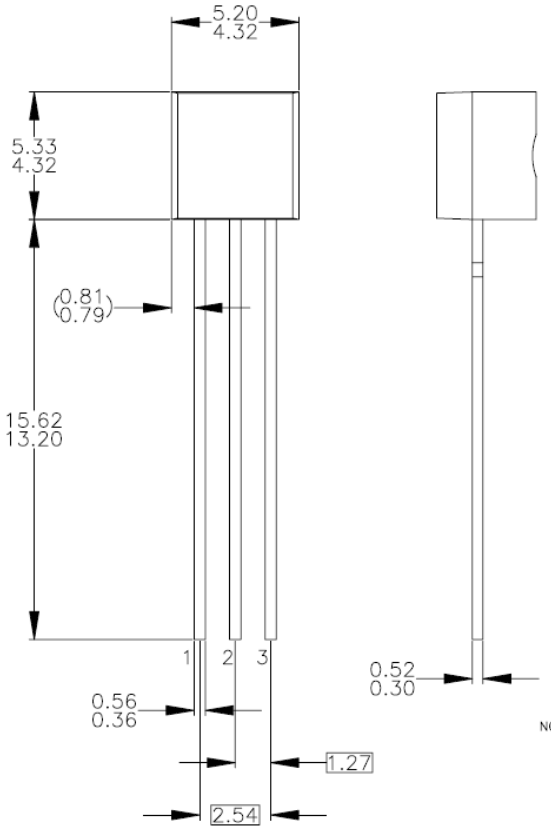


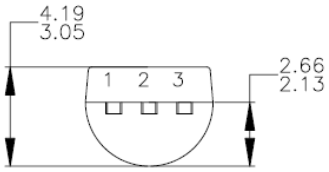
## Typical Performance Characteristics (Continued)

**Power Dissipation vs Ambient Temperature**



## Mechanical Dimensions (TO-92)




NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M-1994.
D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

| PIN | 92 | | | 94 | | | 96 | | | 97 | | | 98 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | P | F | M | P | F | M | B | F | M | P | F | M | P | F | M |
| 1 | E | S | S | E | S | S | B | D | G | C | G | D | C | G | D |
| 2 | B | D | G | C | G | D | E | S | S | B | D | G | E | S | S |
| 3 | C | G | D | B | D | G | C | G | D | E | S | S | B | D | G |

LEGEND:
P – BIPOLAR
F – JFET
M – DMOS
E – EMITTER
B – BASE
C – COLLECTOR
D – DRAIN
S – SOURCE
G – GATE

E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT-ZA03DREV3.

Dimensions in Millimeters

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|---|---|---|
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