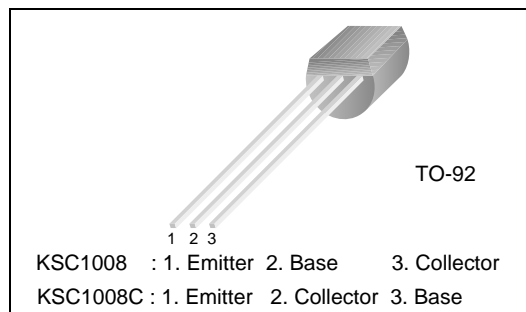


KSC1008

NPN Epitacial Silicon Transistor

Features

- Low frequency amplifier medium speed switching.
- High Collector-Base Voltage : $V_{CBO}=80V$.
- Collector Current : $I_C=700mA$
- Collector Power Dissipation : $P_C=800mW$
- Suffix “-C” means Center Collector (1. Emitter 2. Collector 3. Base)
- Non suffix “-C” means Side Collector (1. Emitter 2. Base 3. Collector)
- Complement to KSA708



Absolute Maximum Ratings * $T_a = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Voltage	80	V
V_{CEO}	Collector-Emitter Voltage	60	V
V_{EBO}	Emitter-Base Voltage	8	V
I_C	Collector current	700	mA
P_C	Collector Power Dissipation	800	mW
T_J	Junction Temperature	+150	$^\circ C$
T_{stg}	Storage Temperature	-55 ~ +150	$^\circ C$

* 1. These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.
2. These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Electrical Characteristics * $T_a = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
BV_{CBO}	Collector-Base Breakdown Voltage	$I_C=100\mu A, I_E=0$	80			V
BV_{CEO}	Collector-Emitter Breakdown Voltage	$I_C=10mA, I_B=0$	60			V
BV_{EBO}	Emitter-Base Breakdown Voltage	$I_E=10\mu A, I_C=0$	8			V
I_{CBO}	Collector Cut-off Current	$V_{CB}=60V, I_E=0$			0.1	μA
I_{EBO}	Emitter Cut-off Current	$V_{EB}=5V, I_C=0$			0.1	μA
h_{FE}	DC Current Gain	$V_{CE}=2V, I_C=50mA$	40		400	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C=500mA, I_B=50mA$		0.2	0.4	V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	$I_C=500mA, I_B=50mA$		0.86	1.1	V
f_T	Current Gain Bandwidth Product	$V_{CE}=10V, I_C=50mA$	30	50		MHz
C_{ob}	Output Capacitance	$V_{CB}=10V, I_E=0, f=1MHz$		8		pF

* DC Item are tested by Pulse Test: Pulse Width \leq 300us, Duty Cycle \leq 2%

h_{FE} Classification

Classification	R	O	Y	G
h_{FE}	40 ~ 80	70 ~ 140	120 ~ 240	200 ~ 400

Package Marking and Ordering Information

Device(note)	Device Marking	Package	Packing Method	Qty(pcs)	Pin Definitions
KSC1008COBU	C1008OC	TO-92	BULK	--	1.Emitter 2.Collector 3.Base
KSC1008COTA	C1008OC	TO-92	TAPE & AMMO	2,000	1.Emitter 2.Collector 3.Base
KSC1008CYBU	C1008YC	TO-92	BULK	--	1.Emitter 2.Collector 3.Base
KSC1008CYTA	C1008YC	TO-92	TAPE & AMMO	2,000	1.Emitter 2.Collector 3.Base
KSC1008GBU	C1008G	TO-92	BULK	--	1.Emitter 2.Base 3.Collector
KSC1008GTA	C1008G	TO-92	TAPE & AMMO	2,000	1.Emitter 2.Base 3.Collector
KSC1008OBU	C1008O	TO-92	BULK	--	1.Emitter 2.Base 3.Collector
KSC1008OTA	C1008O	TO-92	TAPE & AMMO	2,000	1.Emitter 2.Base 3.Collector
KSC1008RBU	C1008R	TO-92	BULK	--	1.Emitter 2.Base 3.Collector
KSC1008RTA	C1008R	TO-92	TAPE & AMMO	2,000	1.Emitter 2.Base 3.Collector
KSC1008YBU	C1008Y	TO-92	BULK	--	1.Emitter 2.Base 3.Collector
KSC1008YTA	C1008Y	TO-92	TAPE & AMMO	2,000	1.Emitter 2.Base 3.Collector
KSC1008YTF	C1008Y	TO-92	TAPE & REEL	2,000	1.Emitter 2.Base 3.Collector

Note : Affix "-C-" - center collector pin.

Affix "-R-, -O-, -Y-, -G-" - h_{FE} classification

Suffix "-BU" - Bulk packing, straight lead form. (see package dimensions)

Suffix "-TF" - Tape & Reel packing, 0.200 In-Line Spacing lead form. (see package dimensions)

Suffix "-TA" - Tape & AMMO packing, 0.200 In-Line Spacing lead form. (see package dimensions)

Typical Characteristics

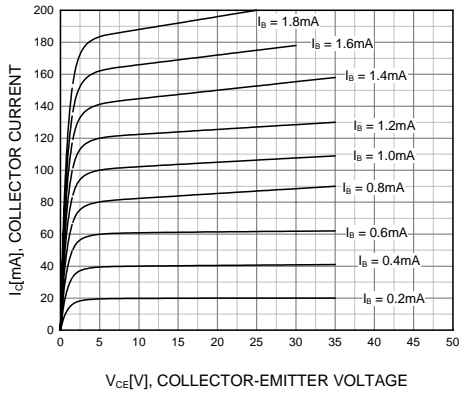


Figure 1. Static Characteristic

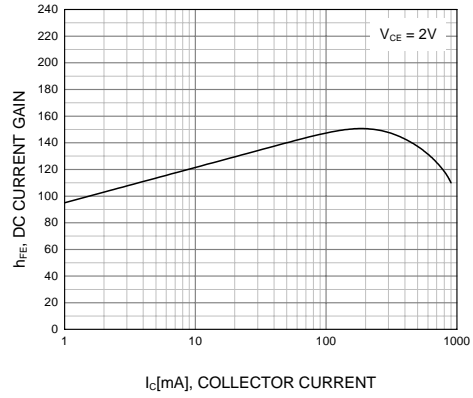


Figure 2. DC current Gain

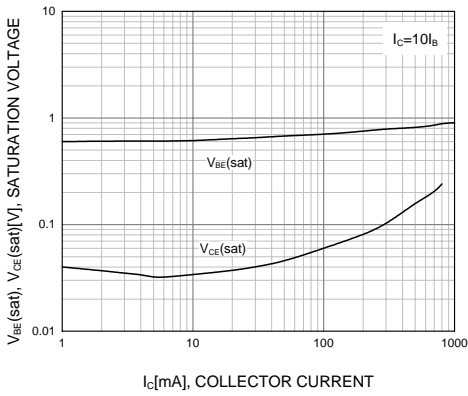


Figure 3. Base-Emitter Saturation Voltage
Collector-Emitter Saturation Voltage

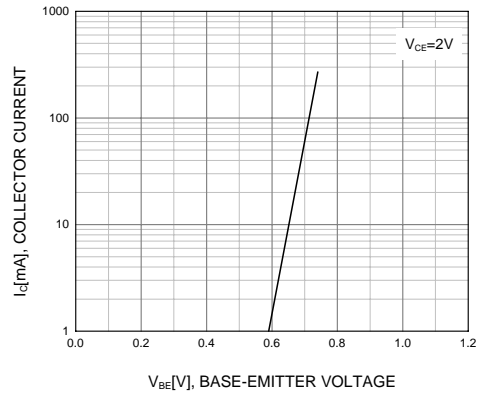


Figure 4. Base-Emitter On Voltage

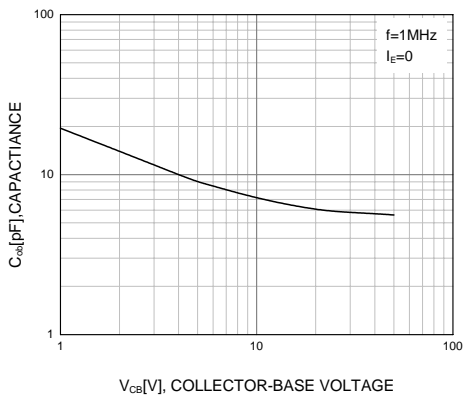
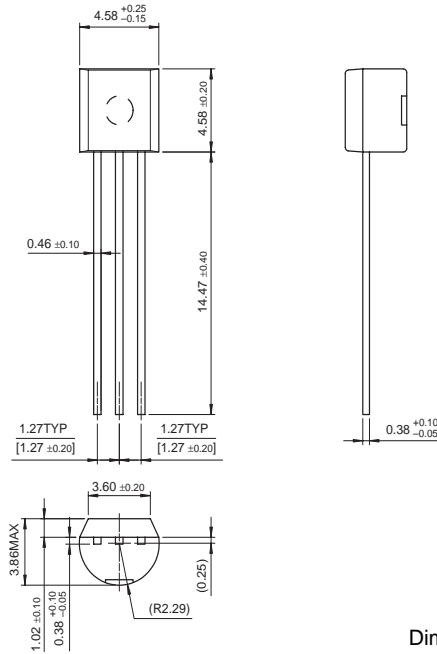


Figure 5. Collector Output Capacitance

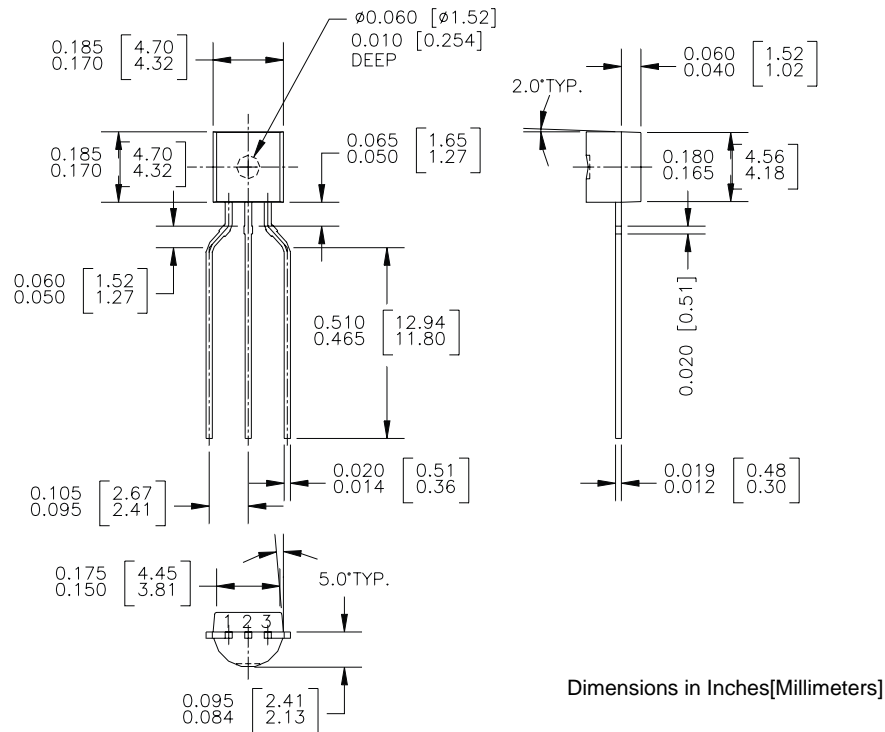
Package Dimensions

TO-92 Straight Lead Form



Dimensions in Millimeters

TO-92 0.200 In-Line Spacing Lead Form



Dimensions in Inches [Millimeters]

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Programmable Active Droop™				

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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