

# MJF6388 (NPN), MJF6668 (PNP)

Preferred Device

## Complementary Power Darlington For Isolated Package Applications

Designed for general-purpose amplifiers and switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

### Features

- Isolated Overmold Package, TO-220 Type
- Electrically Similar to the Popular 2N6388, 2N6668, TIP102, and TIP107
- 100  $V_{CEO(sus)}$
- 10 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- High DC Current Gain – 1000 (Min) @  $I_C = 5.0 \text{ Adc}$
- High Isolation Voltage (up to 4500 VRMS)
- Case 221D is UL Recognized at 3500 VRMS: File #E69369
- Pb-Free Packages are Available\*

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	100	Vdc
Collector-Base Voltage	$V_{CB}$	100	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0	Vdc
RMS Isolation Voltage (Note 1) ( $t = 0.3 \text{ sec}$ , R.H. $\leq 30\%$ , $T_A = 25^\circ\text{C}$ ) Per Figure 14	$V_{ISOL}$	4500	V
Collector Current – Continuous – Peak (Note 2)	$I_C$	10 15	Adc
Base Current – Continuous	$I_B$	1.0	Adc
Total Power Dissipation (Note 3) @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	40 0.31	W W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2.0 0.016	W W/ $^\circ\text{C}$
Operating and Storage Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case (Note 3)	$R_{\theta JC}$	4.0	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$
Lead Temperature for Soldering Purposes	$T_L$	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

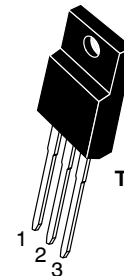
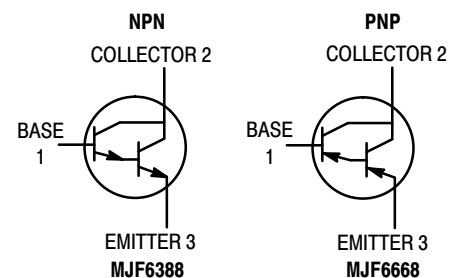
1. Proper strike and creepage distance must be provided.
2. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle  $\leq 10\%$ .
3. Measurement made with thermocouple contacting the bottom insulated surface (in a location beneath the die), the devices mounted on a heatsink with thermal grease and a mounting torque of  $\geq 6 \text{ in. lbs}$ .



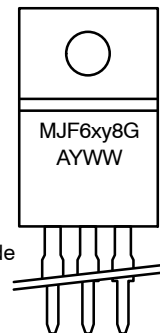
ON Semiconductor®

<http://onsemi.com>

## COMPLEMENTARY SILICON POWER DARLINGTONS 10 AMPERES 100 VOLTS, 40 WATTS



### MARKING DIAGRAM



TO-220 FULLPACK  
CASE 221D  
STYLE 2  
UL RECOGNIZED

- MJF6xy8 = Specific Device Code  
 $x = 3 \text{ or } 6$   
 $y = 6 \text{ or } 8$   
 G = Pb-Free Package  
 A = Assembly Location  
 Y = Year  
 WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MJF6388	TO-220 FULLPACK	50 Units/Rail
MJF6388G	TO-220 FULLPACK (Pb-Free)	50 Units/Rail
MJF6668	TO-220 FULLPACK	50 Units/Rail
MJF6668G	TO-220 FULLPACK (Pb-Free)	50 Units/Rail

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (Note 4) ( $I_C = 30\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	100	–	Vdc
Collector Cutoff Current ( $V_{CE} = 80\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	–	10	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CE} = 100\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 100\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 125^\circ\text{C}$ )	$I_{CEX}$	–	10 3.0	$\mu\text{Adc}$ mAdc
Collector Cutoff Current ( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	–	10	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	2.0	mAdc
<b>ON CHARACTERISTICS (Note 4)</b>				
DC Current Gain ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 5.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ ) ( $I_C = 8.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 10\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )	$h_{FE}$	3000 1000 200 100	15000 – – –	–
Collector–Emitter Saturation Voltage ( $I_C = 3.0\text{ Adc}$ , $I_B = 6.0\text{ mAdc}$ ) ( $I_C = 5.0\text{ Adc}$ , $I_B = 0.01\text{ Adc}$ ) ( $I_C = 8.0\text{ Adc}$ , $I_B = 80\text{ mAdc}$ ) ( $I_C = 10\text{ Adc}$ , $I_B = 0.1\text{ Adc}$ )	$V_{CE(sat)}$	– – – –	2.0 2.0 2.5 3.0	Vdc
Base–Emitter Saturation Voltage ( $I_C = 5.0\text{ Adc}$ , $I_B = 0.01\text{ Adc}$ ) ( $I_C = 10\text{ Adc}$ , $I_B = 0.1\text{ Adc}$ )	$V_{BE(sat)}$	– –	2.8 4.5	Vdc
Base–Emitter On Voltage ( $I_C = 8.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	–	2.5	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Small–Signal Current Gain ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 5.0\text{ Vdc}$ , $f_{test} = 1.0\text{ MHz}$ )	$ h_{fe} $	20	–	–
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1.0\text{ MHz}$ )	MJF6388 MJF6668 $C_{ob}$	–	200 300	pF
Insulation Capacitance (Collector–to–External Heatsink)	$C_{c-hs}$	–	3.0 Typ	pF
Small–Signal Current Gain ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 5.0\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	1000	–	–

4. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

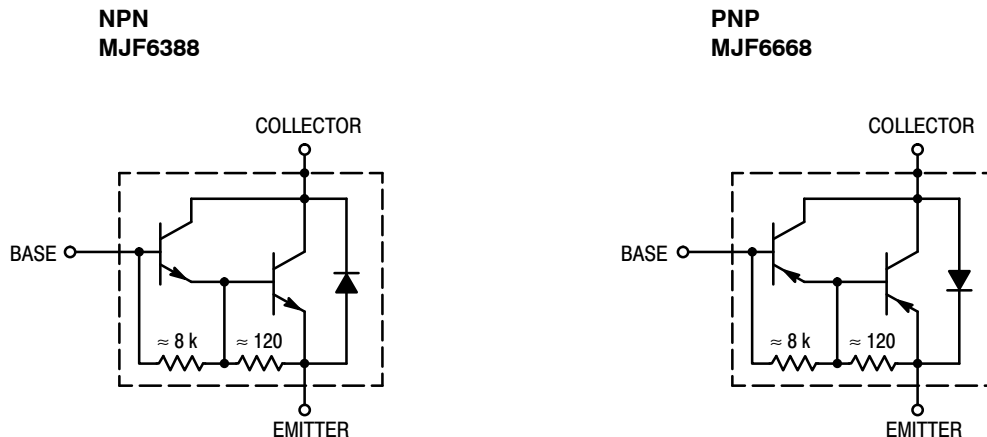
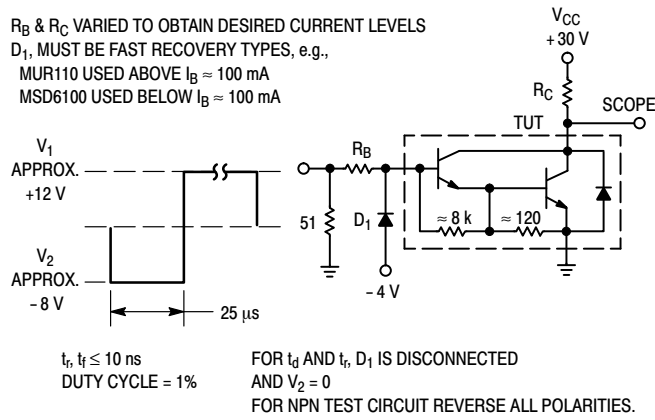


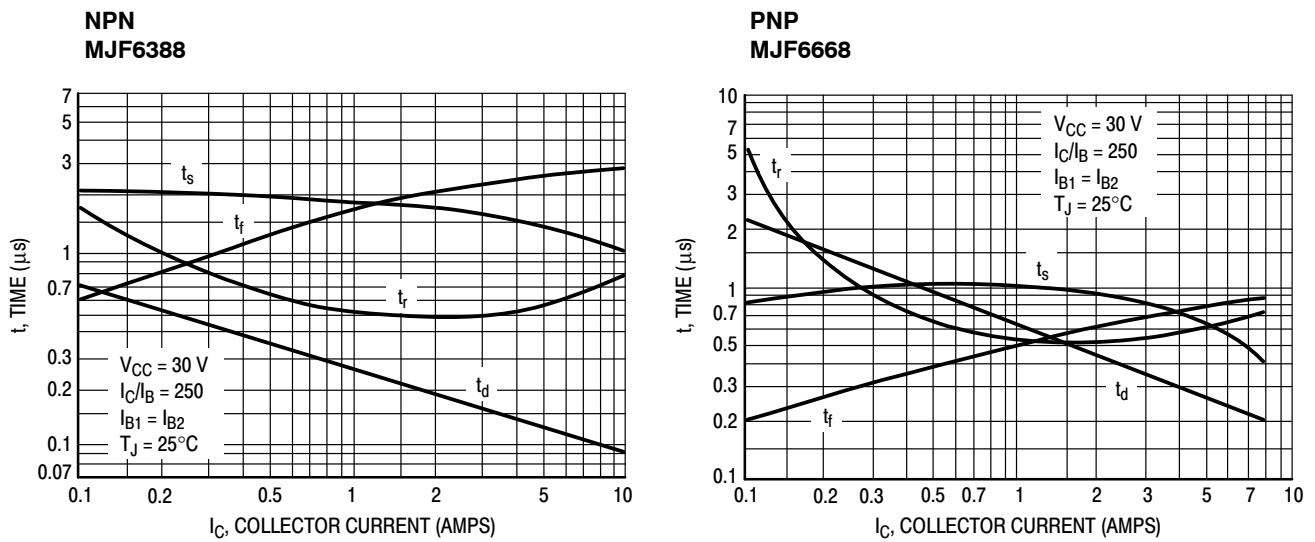
Figure 1. Darlington Schematic

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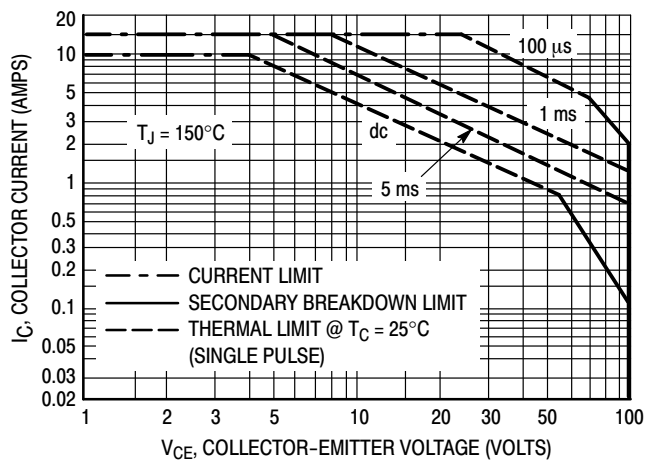
$R_B$  &  $R_C$  VARIED TO OBTAIN DESIRED CURRENT LEVELS  
 $D_1$ , MUST BE FAST RECOVERY TYPES, e.g.,  
 MUR110 USED ABOVE  $I_B \approx 100$  mA  
 MSD6100 USED BELOW  $I_B \approx 100$  mA



**Figure 2. Switching Times Test Circuit**



**Figure 3. Typical Switching Times**



**Figure 4. Maximum Forward Bias Safe Operating Area**

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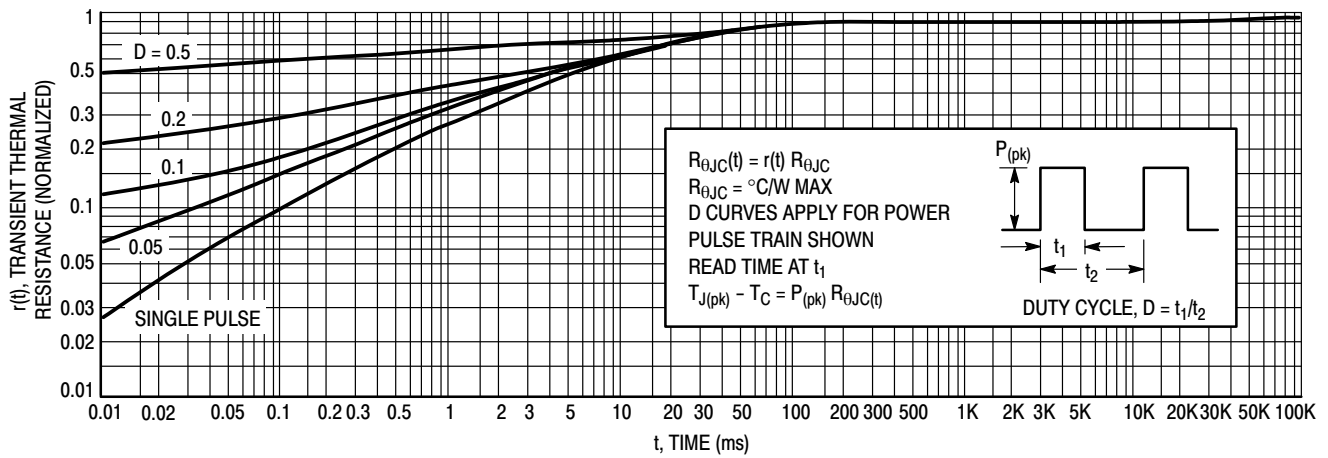


Figure 5. Thermal Response

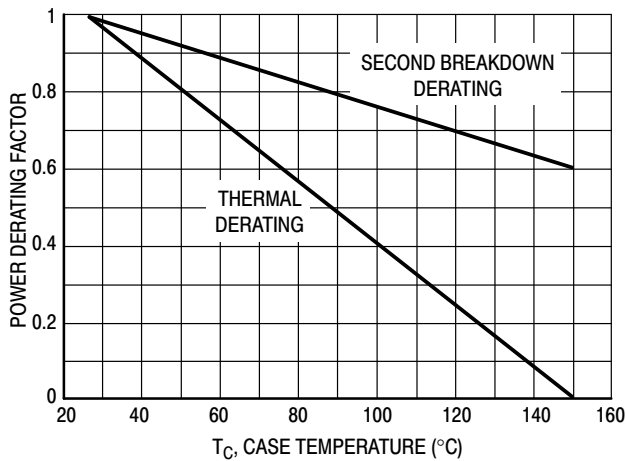


Figure 6. Maximum Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

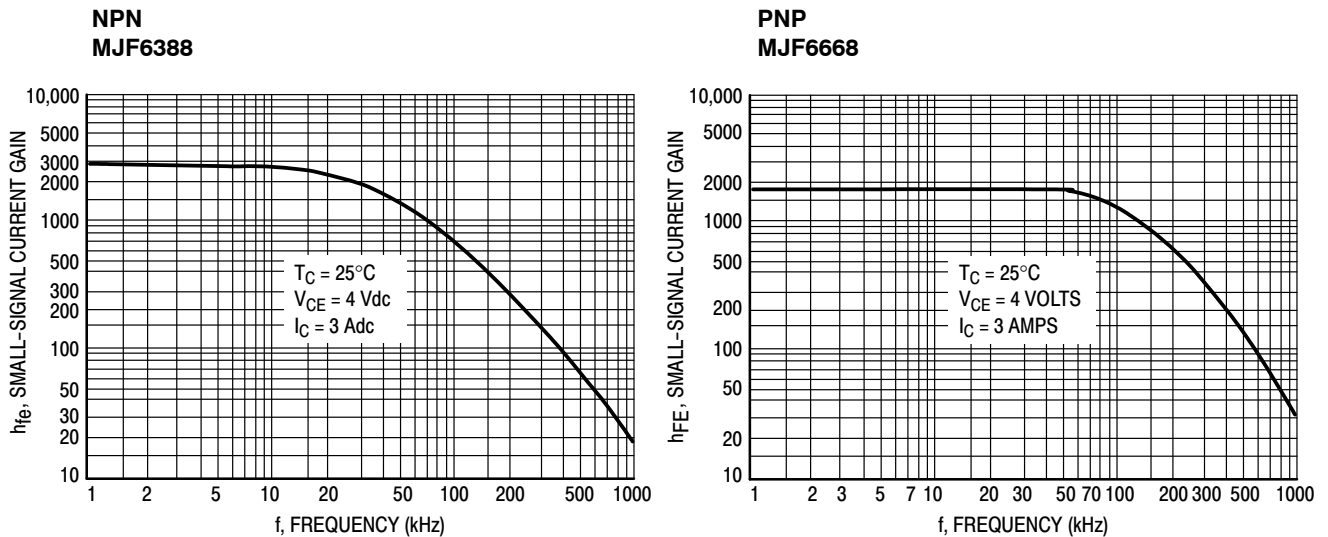


Figure 7. Typical Small-Signal Current Gain

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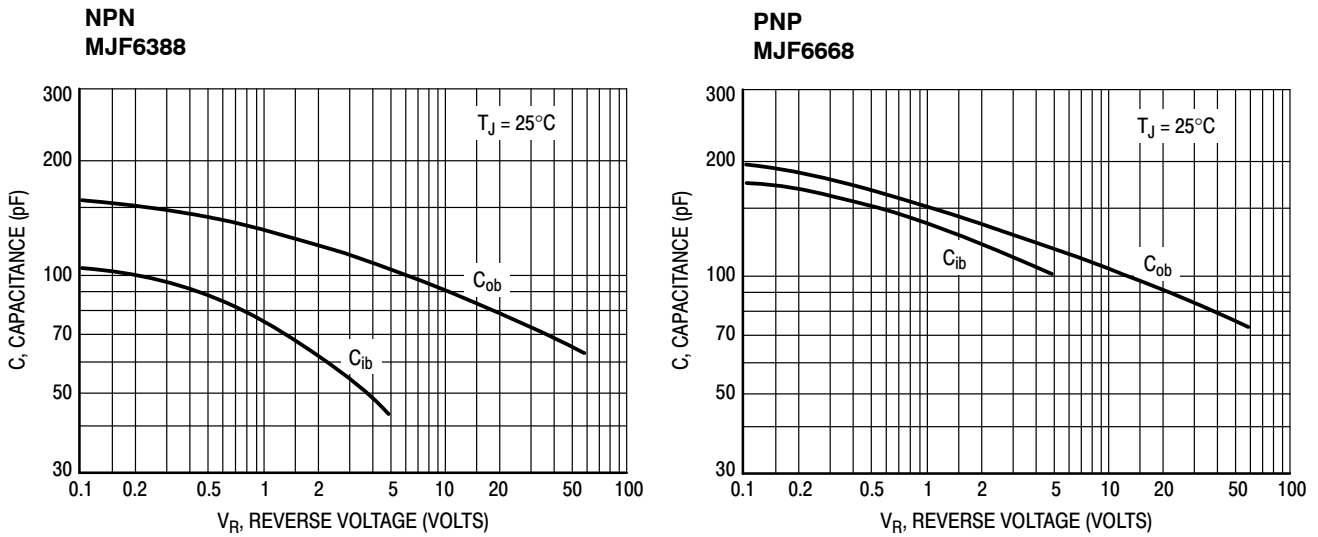


Figure 8. Typical Capacitance

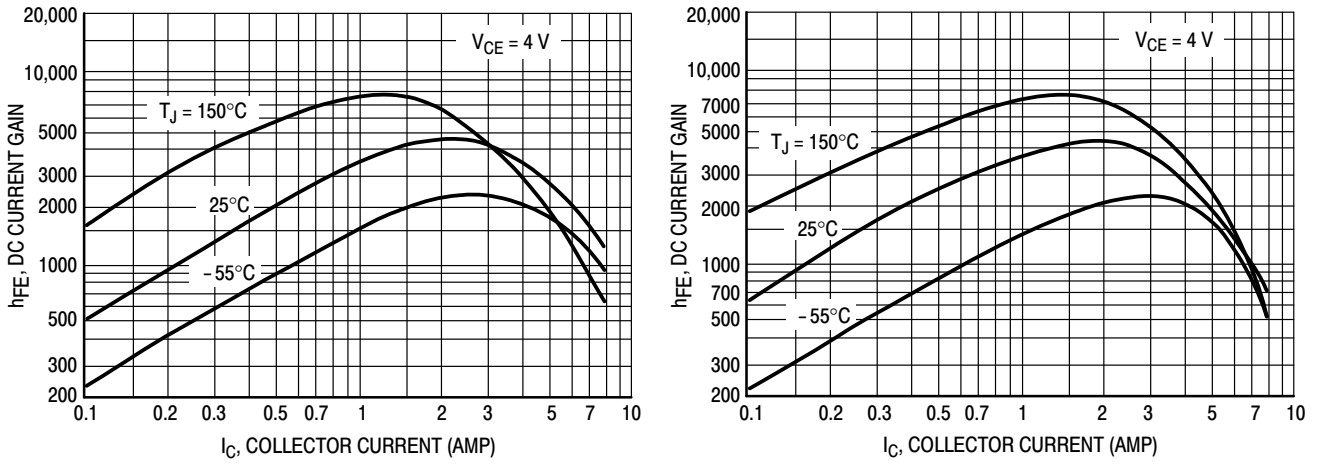


Figure 9. Typical DC Current Gain

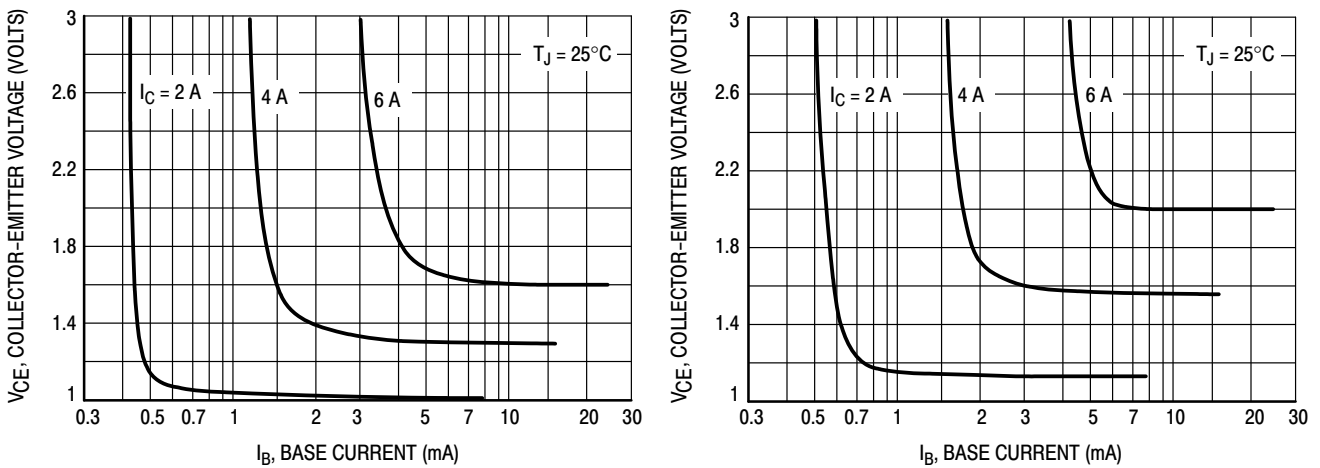


Figure 10. Typical Collector Saturation Region

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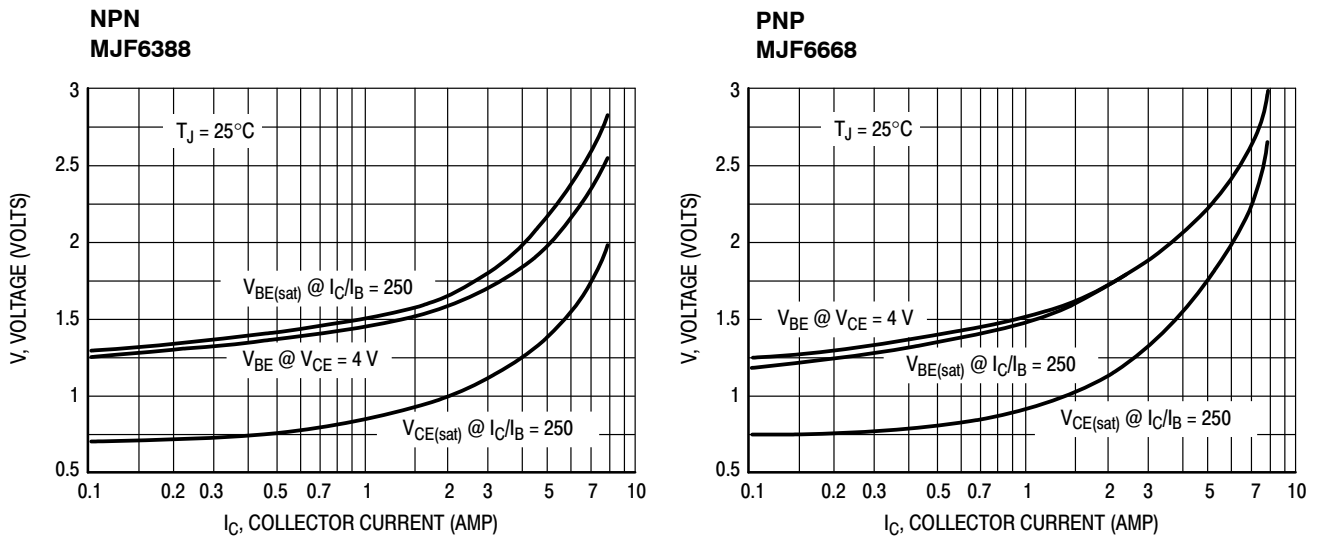


Figure 11. Typical "On" Voltages

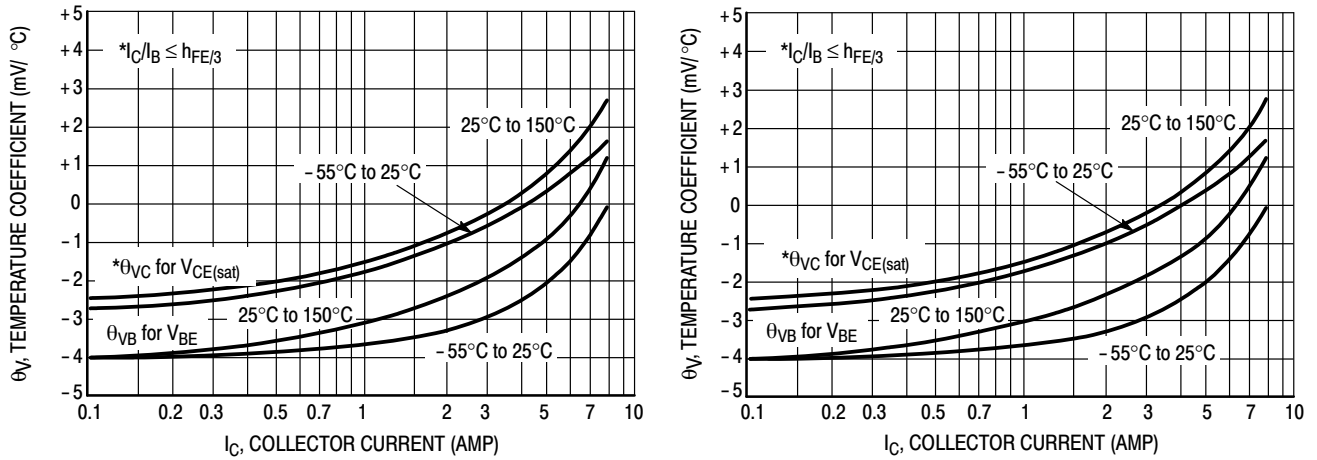


Figure 12. Typical Temperature Coefficients

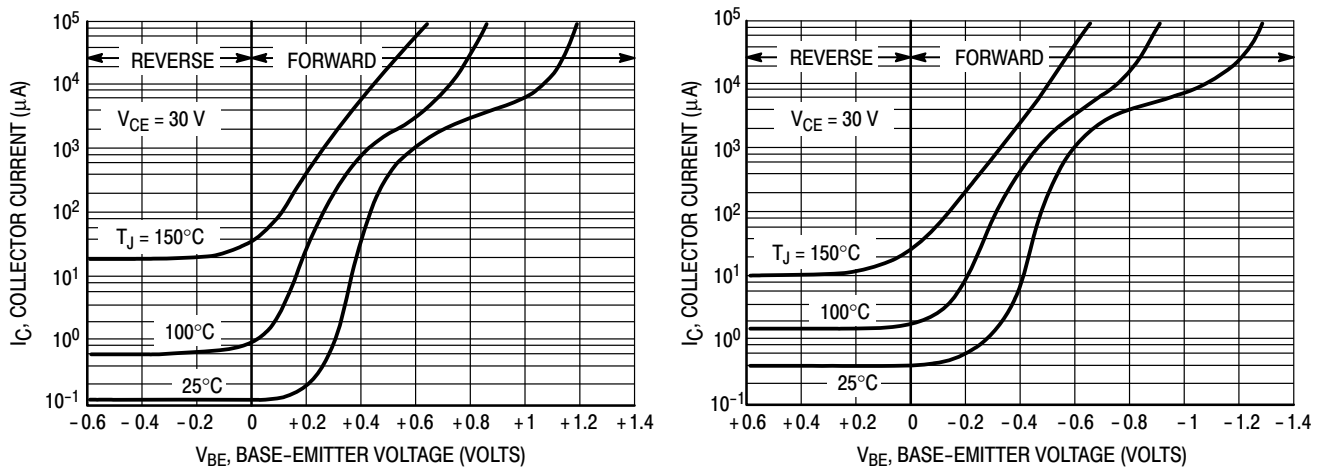


Figure 13. Typical Collector Cut-Off Region

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### TEST CONDITION FOR ISOLATION TEST\*

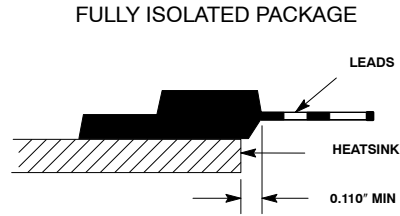


Figure 14. Mounting Position

\*Measurement made between leads and heatsink with all leads shorted together.

### MOUNTING INFORMATION

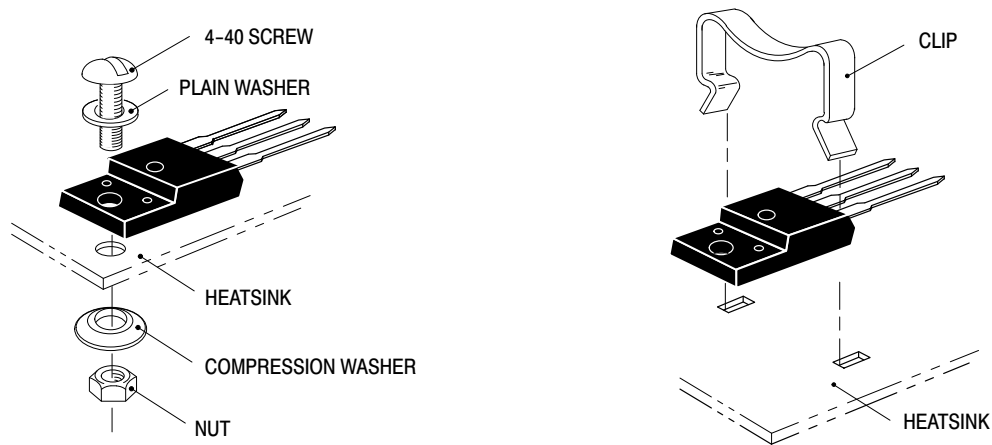


Figure 15. Typical Mounting Techniques\*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4-40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

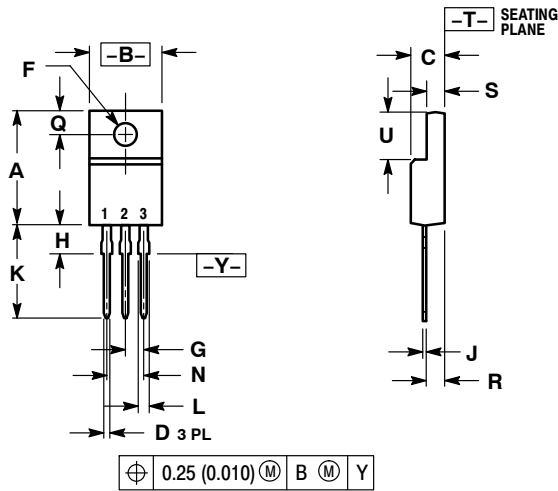
Additional tests on slotted 4-40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

\*\* For more information about mounting power semiconductors see Application Note AN1040.

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## PACKAGE DIMENSIONS

TO-220 FULLPAK  
CASE 221D-03  
ISSUE J



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

**STYLE 2:**

1. BASE
2. COLLECTOR
3. EMITTER

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