

MJ15003 (NPN), MJ15004 (PNP)

Preferred Device

Complementary Silicon Power Transistors

The MJ15003 and MJ15004 are PowerBase™ power transistors designed for high power audio, disk head positioners and other linear applications.

Features

- High Safe Operating Area (100% Tested) – 5.0 A @ 50 V
- For Low Distortion Complementary Designs
- High DC Current Gain – $h_{FE} = 25$ (Min) @ $I_C = 5$ Adc
- Pb-Free Packages are Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	140	Vdc
Collector-Base Voltage	V_{CBO}	140	Vdc
Emitter-Base Voltage	V_{EBO}	5	Vdc
Collector Current – Continuous	I_C	20	Adc
Base Current – Continuous	I_B	5	Adc
Emitter Current – Continuous	I_E	25	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	250 1.43	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.70	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes 1/16" from Case for ≤ 10 secs	T_L	265	$^\circ\text{C}$

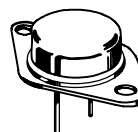
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.



ON Semiconductor®

<http://onsemi.com>

**20 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
140 VOLTS, 250 WATTS**



TO-204AA (TO-3)
CASE 1-07
STYLE 1

MARKING DIAGRAM



MJ1500x = Device Code
x = 3 or 4
G = Pb-Free Package
A = Location Code
YY = Year
WW = Work Week
MEX = Country of Origin

ORDERING INFORMATION

Device	Package	Shipping
MJ15003	TO-204AA	100 Units/Tray
MJ15003G	TO-204AA (Pb-Free)	100 Units/Tray
MJ15004	TO-204AA	100 Units/Tray
MJ15004G	TO-204AA (Pb-Free)	100 Units/Tray

Preferred devices are recommended choices for future use and best overall value.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MJ15003 (NPN), MJ15004 (PNP)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector Emitter Sustaining Voltage (Note 1) ($I_C = 200\text{ mAdc}$, $I_B = 0$)	$V_{CE(sus)}$	140	–	Vdc
Collector Cutoff Current ($V_{CE} = 140\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CE} = 140\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEX}	–	100 2	μAdc mAdc
Collector Cutoff Current ($V_{CE} = 140\text{ Vdc}$, $I_B = 0$)	I_{CEO}	–	250	μAdc
Emitter Cutoff Current ($V_{EB} = 5\text{ Vdc}$, $I_C = 0$)	I_{EBO}	–	100	μAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased ($V_{CE} = 50\text{ Vdc}$, $t = 1\text{ s}$ (non repetitive)) ($V_{CE} = 100\text{ Vdc}$, $t = 1\text{ s}$ (non repetitive))	$I_{S/b}$	5.0 1.0	– –	Adc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 5\text{ Adc}$, $V_{CE} = 2\text{ Vdc}$)	h_{FE}	25	150	–
Collector Emitter Saturation Voltage ($I_C = 5\text{ Adc}$, $I_B = 0.5\text{ Adc}$)	$V_{CE(sat)}$	–	1.0	Vdc
Base Emitter On Voltage ($I_C = 5\text{ Adc}$, $V_{CE} = 2\text{ Vdc}$)	$V_{BE(on)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product ($I_C = 0.5\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$, $f_{test} = 0.5\text{ MHz}$)	f_T	2.0	–	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1\text{ MHz}$)	C_{ob}	–	1000	pF

1. Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2\%$.

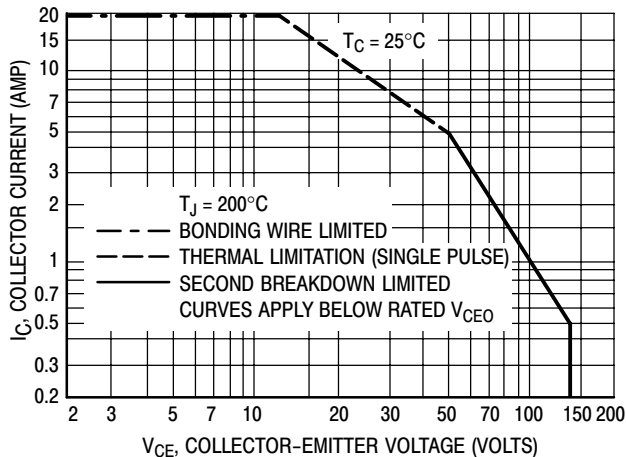


Figure 1. Active-Region Safe Operating Area

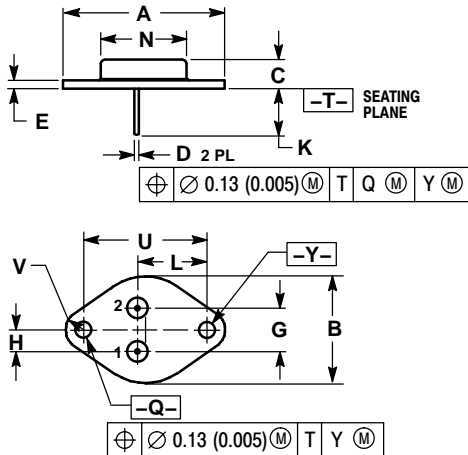
There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MJ15003 (NPN), MJ15004 (PNP)

PACKAGE DIMENSIONS

TO-204 (TO-3)
CASE 1-07
ISSUE Z



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:

- PIN 1. BASE
 - EMITTER
- CASE: COLLECTOR

PowerBase is a trademark of Semiconductor Components Industries, LLC.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.

MJ15003/D