2N6109 and 2N6292 are Preferred Devices

# **Complementary Silicon Plastic Power Transistors**

These devices are designed for use in general-purpose amplifier and switching applications.

#### **Features**

• DC Current Gain Specified to 7.0 Amperes

• Collector-Emitter Sustaining Voltage -

• High Current Gain - Bandwidth Product

$$f_T$$
 = 4.0 MHz (Min) @  $I_C$  = 500 mAdc - 2N6288, 90, 92 = 10 MHz (Min) @  $I_C$  = 500 mAdc - 2N6107, 09, 11

- TO-220AB Compact Package
- Pb-Free Packages are Available\*

### MAXIMUM RATINGS (Note 1)

Rating		Symbol	Value	Unit
Collector-Emitter Voltage	2N6111, 2N6288 2N6109 2N6107, 2N6292	V <sub>CEO</sub>	30 50 70	Vdc
Collector-Base Voltage	2N6111, 2N6288 2N6109 2N6107, 2N6292	V <sub>CB</sub>	40 60 80	Vdc
Emitter-Base Voltage		V <sub>EB</sub>	5.0	Vdc
Collector Current - Contin - Peak	nuous	I <sub>C</sub>	7.0 10	Adc
Base Current		Ι <sub>Β</sub>	3.0	Adc
Total Power Dissipation @ Derate above 25°C	© T <sub>C</sub> = 25°C	P <sub>D</sub>	40 0.32	W W/°C
Operating and Storage Ju Temperature Range	ınction	T <sub>J</sub> , T <sub>stg</sub>	-65 to +150	°C

### THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.125	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Indicates JEDEC Registered Data.

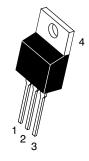


## ON Semiconductor®

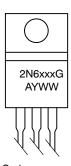
http://onsemi.com

# **7 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON** 30 - 50 - 70 VOLTS, 40 WATTS

### **MARKING DIAGRAM**



TO-220AB CASE 221A STYLE 1



2N6xxx = Specific Device Code = See Table on Page 4 XXX G = Pb-Free Package Α = Assembly Location = Year

= Work Week

### ORDERING INFORMATION

See detailed ordering, marking, and shipping information in the package dimensions section on page 4 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

<sup>\*</sup>For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

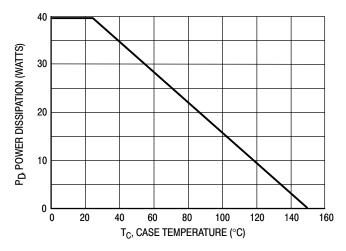


Figure 1. Power Derating

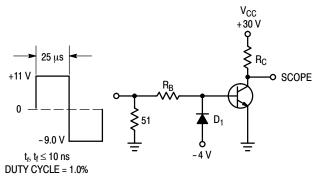
# **ELECTRICAL CHARACTERISTICS** ( $T_C = 25^{\circ}C$ unless otherwise noted) (Note 2)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Note 3) $(I_C = 100 \text{ mAdc}, I_B = 0)$	2N6111, 2N6288 2N6109 2N6107, 2N6292	$V_{CEO(sus)}$	30 50 70	- - -	Vdc
Collector Cutoff Current $(V_{CE} = 20 \text{ Vdc}, I_B = 0)$ $(V_{CE} = 40 \text{ Vdc}, I_B = 0)$ $(V_{CE} = 60 \text{ Vdc}, I_B = 0)$	2N6111, 2N6288 2N6109 2N6107, 2N6292	I <sub>CEO</sub>	- - -	1.0 1.0 1.0	mAdc
	2N6111, 2N6288 2N6109 2N6107, 2N6292 2N6111, 2N6288 2N6109 2N6107, 2N6292	I <sub>CEX</sub>	- - - -	100 100 100 2.0 2.0 2.0	μAdc mAdc
Emitter Cutoff Current (V <sub>BE</sub> = 5.0 Vdc, I <sub>C</sub> = 0)		I <sub>EBO</sub>	-	1.0	mAdc
ON CHARACTERISTICS (Note 3)					
DC Current Gain $ \begin{array}{l} (I_C = 2.0 \; \text{Adc}, \; V_{CE} = 4.0 \; \text{Vdc}) \\ (I_C = 2.5 \; \text{Adc}, \; V_{CE} = 4.0 \; \text{Vdc}) \\ (I_C = 3.0 \; \text{Adc}, \; V_{CE} = 4.0 \; \text{Vdc}) \\ (I_C = 7.0 \; \text{Adc}, \; V_{CE} = 4.0 \; \text{Vdc}) \end{array} $	2N6107, 2N6292 2N6109 2N6111, 2N6288 All Devices	h <sub>FE</sub>	30 30 30 2.3	150 150 150 -	-
Collector-Emitter Saturation Voltage (I <sub>C</sub> = 7.0 Adc, I <sub>B</sub> = 3.0 Adc)		V <sub>CE(sat)</sub>	-	3.5	Vdc
Base-Emitter On Voltage (I <sub>C</sub> = 7.0 Adc, V <sub>CE</sub> = 4.0 Vdc)		V <sub>BE(on)</sub>	-	3.0	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (Note 4) $(I_C = 500 \text{ mAdc}, V_{CE} = 4.0 \text{ Vdc}, f_{test} = 1.0 \text{ MHz})$	2N6288, 92 2N6107, 09, 11	f <sub>T</sub>	4.0 10	- -	MHz
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 1.0 MHz)		C <sub>ob</sub>	-	250	pF
Small-Signal Current Gain ( $I_C$ = 0.5 Adc, $V_{CE}$ = 4.0 Vdc, f = 50 kHz	<u></u>	h <sub>fe</sub>	20	_	-

<sup>2.</sup> Indicates JEDEC Registered Data.

<sup>3.</sup> Pulse Test: Pulse Width  $\leq$  300  $\mu$ s, Duty Cycle  $\leq$  2.0%.

<sup>4.</sup>  $f_T = |h_{fe}| \bullet f_{test}$ 



 $\ensuremath{\mathsf{R}}_B$  and  $\ensuremath{\mathsf{R}}_C$  are varied to obtain desired current levels

D1 MUST BE FAST RECOVERY TYPE, eg: 1N5825 USED ABOVE I  $_{B} \approx 100$  mA MSD6100 USED BELOW I  $_{B} \approx 100$  mA

Figure 2. Switching Time Test Circuit

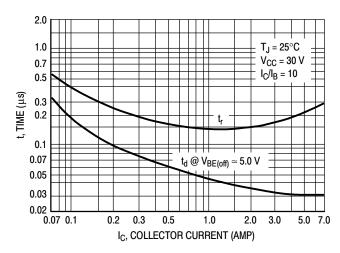


Figure 3. Turn-On Time

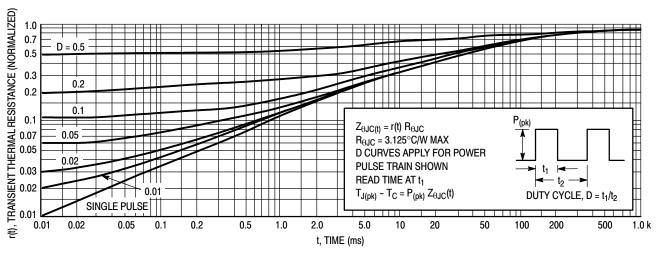


Figure 4. Thermal Response

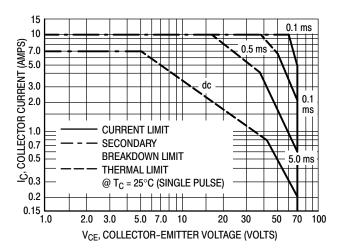


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C$  –  $V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^{\circ} C$ ;  $T_{C}$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^{\circ} C$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

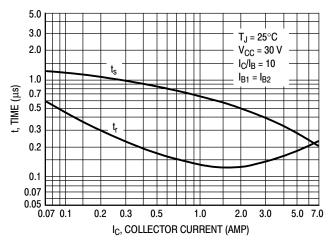


Figure 6. Turn-Off Time

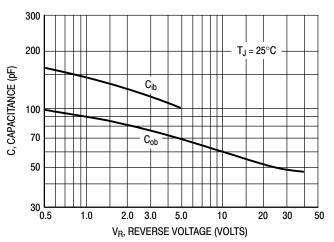


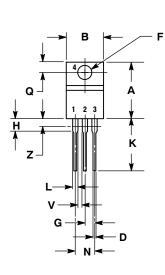
Figure 7. Capacitance

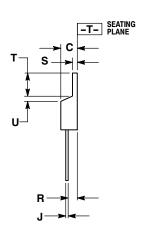
## **ORDERING INFORMATION**

Device	Device Marking	Package	Shipping
2N6107		TO-220AB	
2N6107G	2N6107	TO-220AB (Pb-Free)	50 Units / Rail
2N6109		TO-220AB	
2N6109G	2N6109	TO-220AB (Pb-Free)	50 Units / Rail
2N6111		TO-220AB	
2N6111G	2N6111	TO-220AB (Pb-Free)	50 Units / Rail
2N6288		TO-220AB	
2N6288G	2N6288	TO-220AB (Pb-Free)	50 Units / Rail
2N6292		TO-220AB	
2N6292G	2N6292	TO-220AB (Pb-Free)	50 Units / Rail

### PACKAGE DIMENSIONS

TO-220 CASE 221A-09 ISSUE AE





#### NOTES

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.570	0.620	14.48	15.75
В	0.380	0.405	9.66	10.28
С	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
Н	0.110	0.155	2.80	3.93
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
٧	0.045		1.15	
Z		0.080		2.04

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