

BSP19AT1G

NPN Silicon Epitaxial Transistor

This family of NPN Silicon Epitaxial transistors is designed for use as a general purpose amplifier and in switching applications. The device is housed in the SOT-223 package which is designed for medium power surface mount applications.

Features

- High Voltage: $V_{(BR)CEO}$ of 250 and 350 V
- The SOT-223 Package Can Be Soldered Using Wave or Reflow
- SOT-223 Package Ensures Level Mounting, Resulting in Improved Thermal Conduction, and Allows Visual Inspection of Soldered Joints
- The Formed Leads Absorb Thermal Stress During Soldering, Eliminating the Possibility of Damage to the Die
- PNP Complement is BSP16T1
- Moisture Sensitivity Level (MSL): 1
- ESD: Human Body Model (HBM) = 4 KV
Machine Model (MM) = 400 V
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage (Open Base)	V_{CEO}	350	Vdc
Collector-Base Voltage (Open Emitter)	V_{CBO}	400	Vdc
Emitter-Base Voltage (Open Collector)	V_{EBO}	5.0	Vdc
Collector Current (DC)	I_C	100	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1) Derate above 25°C	P_D	0.8 6.4	W mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	156	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

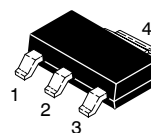
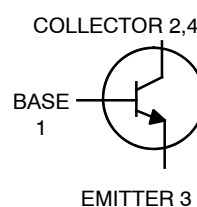
1. Device mounted on a FR-4 glass epoxy printed circuit board using minimum recommended footprint.



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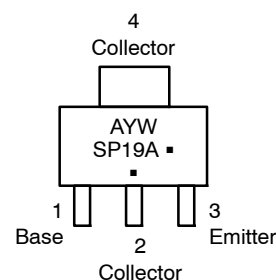
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SOT-223 PACKAGE NPN SILICON HIGH VOLTAGE TRANSISTOR SURFACE MOUNT



CASE 318E
TO-261AA
STYLE 1

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
SP19A = Specific Device Code
■ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
BSP19AT1G	SOT-223 (Pb-Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage ($I_C = 1.0\text{ mAdc}$, $I_B = 0$)	$V_{(BR)CEO}$	350	-	Vdc
Collector-Base Cutoff Current ($V_{CB} = 400\text{ Vdc}$, $I_E = 0$)	I_{CBO}	-	20	nAdc
Emitter-Base Cutoff Current ($V_{EB} = 5.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	-	10	μAdc
ON CHARACTERISTICS (Note 2)				
DC Current Gain ($I_C = 20\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$)	h_{FE}	40	-	-
Current-Gain — Bandwidth Product ($I_C = 10\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $f = 5.0\text{ MHz}$)	f_T	70	-	MHz
Collector-Emitter Saturation Voltage ($I_C = 50\text{ mAdc}$, $I_B = 4.0\text{ mAdc}$)	$V_{CE(sat)}$	-	0.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 50\text{ mAdc}$, $I_B = 4.0\text{ mAdc}$)	$V_{BE(sat)}$	-	1.3	Vdc

2. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle = 2.0%

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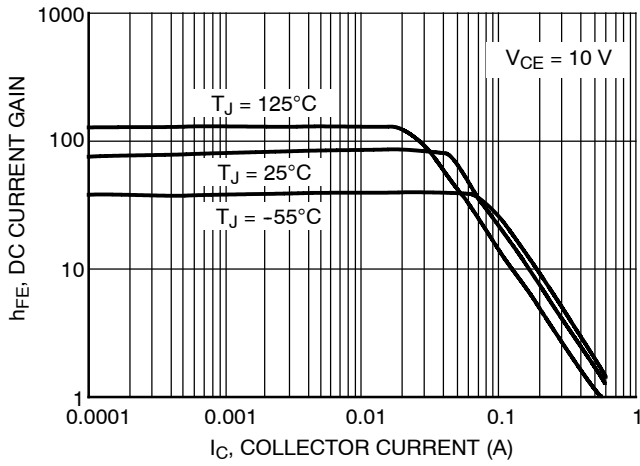


Figure 1. DC Current Gain

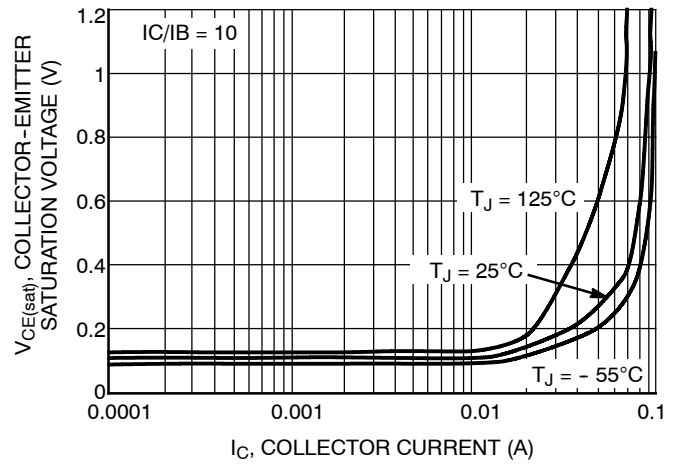


Figure 2. Collector Saturation Voltage

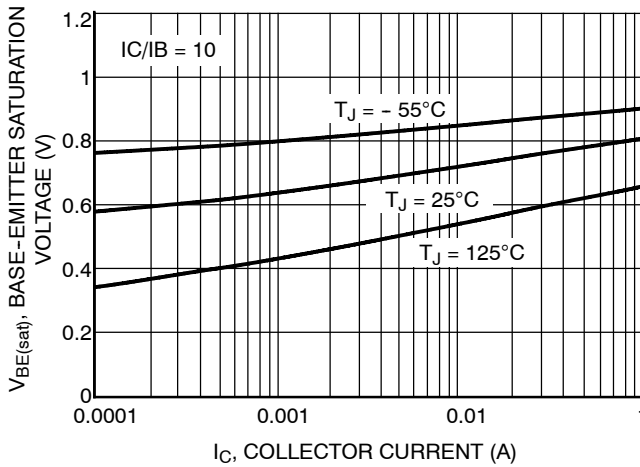


Figure 3. Base Saturation Voltage

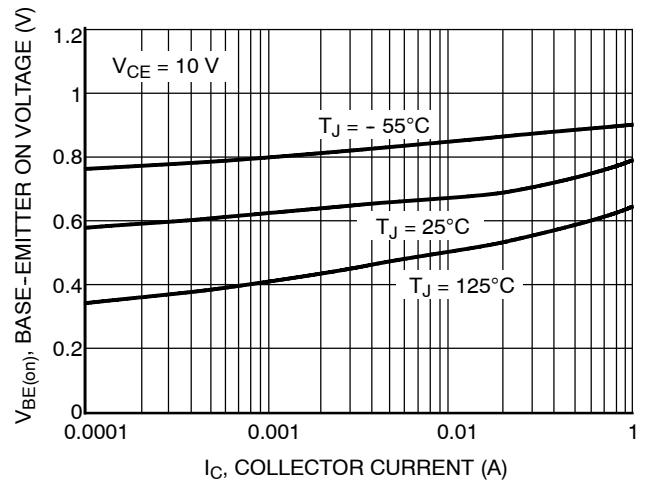


Figure 4. Base ON Voltage

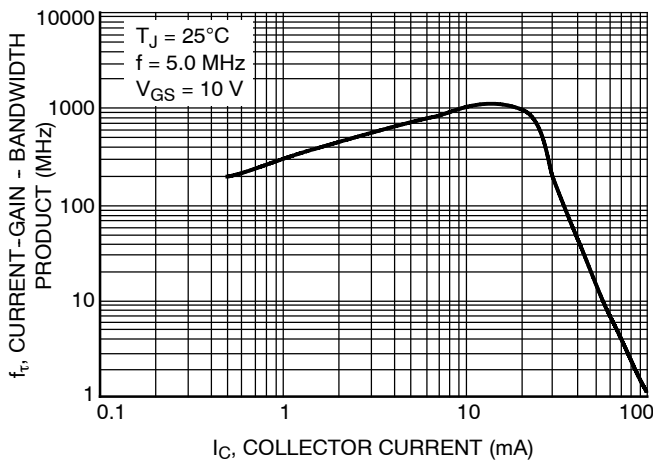


Figure 5. Current Gain - Bandwidth Product

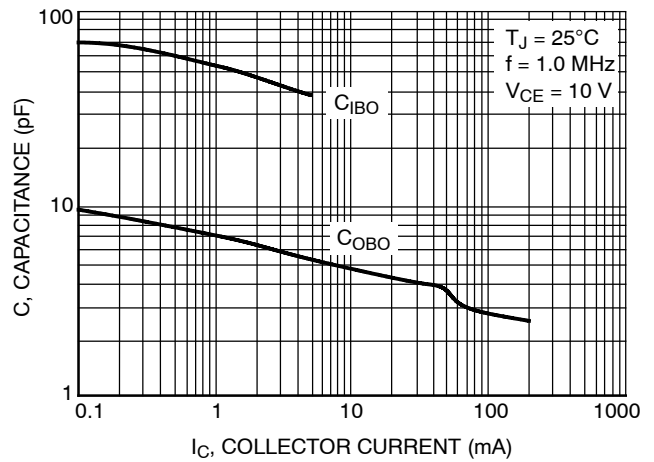
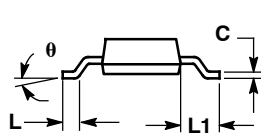
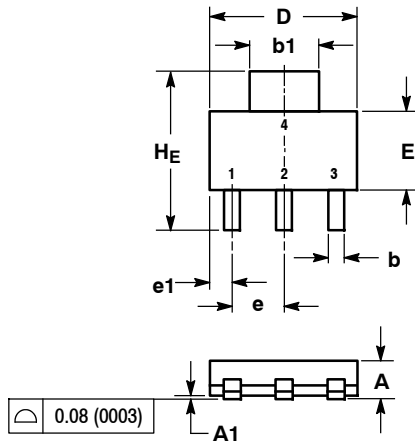


Figure 6. Capacitance

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PACKAGE DIMENSIONS

SOT-223 (TO-261)
CASE 318E-04
ISSUE N

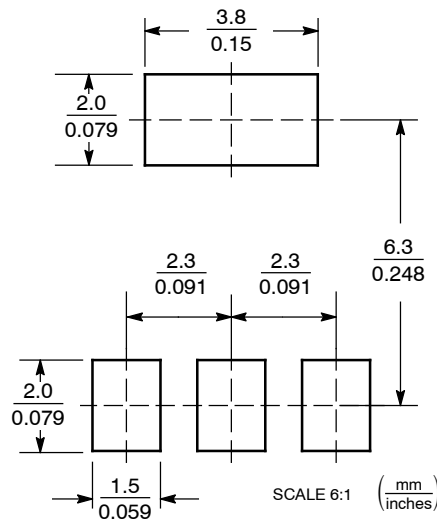


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L	0.20	---	---	0.008	---	---
L1	1.50	1.75	2.00	0.060	0.069	0.078
HE	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	-	10°	0°	-	10°

- STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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