Darlington Transistor

NPN Silicon

Features

• These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector - Emitter Voltage	V _{CEO}	40	Vdc
Collector - Base Voltage	V _{CBO}	40	Vdc
Emitter - Base Voltage	V _{EBO}	12	Vdc
Collector Current - Continuous	I _C	500	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board, (Note 1) T _A = 25°C Derate above 25°C	P _D	225 1.8	mW mW/°C
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate, (Note 2) T _A = 25°C Derate above 25°C	P _D	300 2.4	mW mW/°C
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T _J , T _{stg}	-55 to +150	°C

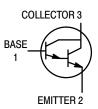
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. $FR-5 = 1.0 \times 0.75 \times 0.062$ in.
- 2. Alumina = 0.4 x 0.3 x 0.024 in. 99.5% alumina.



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SOT-23 (TO-236) CASE 318 STYLE 6

MARKING DIAGRAM



1V = Device Code M = Date Code* ■ = Pb-Free Package

(Note: Microdot may be in either location)
*Date Code orientation and/or overbar may
vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping [†]
MMBT6427LT1G	SOT-23 (Pb-Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector – Emitter Breakdown Voltage (I _C = 10 mAdc, V _{BE} = 0)	V _{(BR)CEO}	40	-	Vdc
Collector – Base Breakdown Voltage (I_C = 100 μ Adc, I_E = 0)	V _{(BR)CBO}	40	-	Vdc
Emitter – Base Breakdown Voltage ($I_C = 10 \mu Adc, I_C = 0$)	V _{(BR)EBO}	12	-	Vdc
Collector Cutoff Current ($V_{CE} = 25 \text{ Vdc}, I_B = 0$)	I _{CES}	-	1.0	μAdc
Collector Cutoff Current $(V_{CB} = 30 \text{ Vdc}, I_E = 0)$	Ісво	-	50	nAdc
Emitter Cutoff Current $(V_{EB} = 10 \text{ Vdc}, I_C = 0)$	I _{EBO}	-	50	nAdc
ON CHARACTERISTICS	<u>.</u>			
DC Current Gain	h _{FE}	10,000 20,000 14,000	100,000 200,000 140,000	-
Collector – Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 0.5 mAdc) (I_C = 500 mAdc, I_B = 0.5 mAdc)	V _{CE(sat)} ⁽³⁾	- -	1.2 1.5	Vdc
Base – Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 0.5 mAdc)	V _{BE(sat)}	-	2.0	Vdc
Base – Emitter On Voltage ($I_C = 50 \text{ mAdc}, V_{CE} = 5.0 \text{ Vdc}$)	V _{BE(on)}	-	1.75	Vdc
SMALL-SIGNAL CHARACTERISTICS				
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 1.0 MHz)	C _{obo}	_	7.0	pF
Input Capacitance (V _{EB} = 0.5 Vdc, I _C = 0, f = 1.0 MHz)	C _{ibo}	-	15	pF
Current Gain - High Frequency (I _C = 10 mAdc, V _{CE} = 5.0 Vdc, f = 100 MHz)	h _{fe}	1.3	-	Vdc
Noise Figure (I _C = 1.0 mAdc, V_{CE} = 5.0 Vdc, R_{S} = 100 k Ω , f = 1.0 kHz)	NF	-	10	dB

^{3.} Pulse Test: Pulse Width = 300 μ s, Duty Cycle = 2.0%.

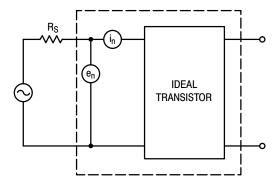


Figure 1. Transistor Noise Model

NOISE CHARACTERISTICS

 $(V_{CE} = 5.0 \text{ Vdc}, T_A = 25^{\circ}C)$

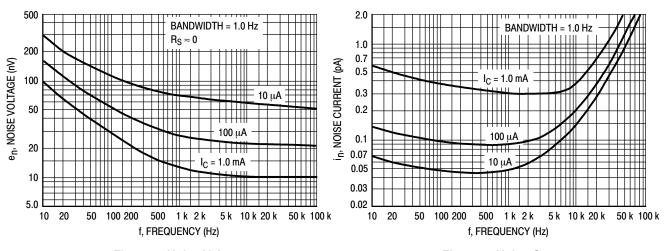


Figure 2. Noise Voltage

Figure 3. Noise Current

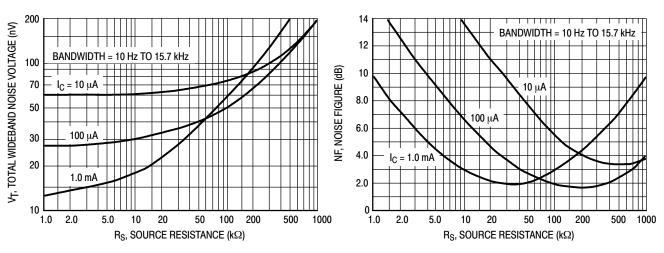
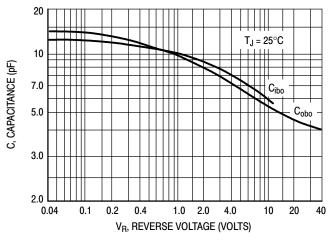


Figure 4. Total Wideband Noise Voltage

Figure 5. Wideband Noise Figure

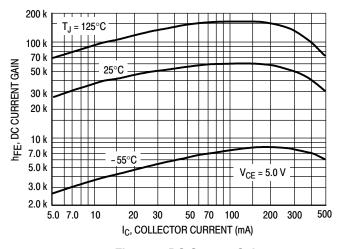
SMALL-SIGNAL CHARACTERISTICS



V_{CE} = 5.0 V Ihfel, SMALL-SIGNAL CURRENT GAIN f = 100 MHz $T_J = 25^{\circ}C$ 2.0 1.0 8.0 0.6 0.4 0.2 2.0 20 100 200 500 1.0 0.5 10 50 0.5 IC, COLLECTOR CURRENT (mA)

Figure 6. Capacitance

Figure 7. High Frequency Current Gain



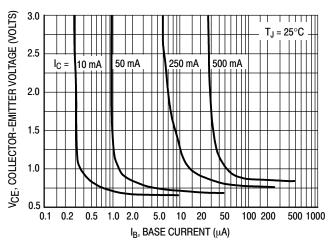
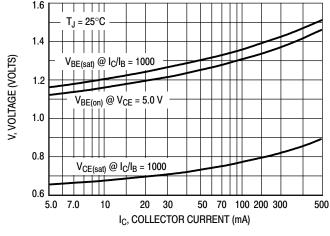


Figure 8. DC Current Gain

Figure 9. Collector Saturation Region



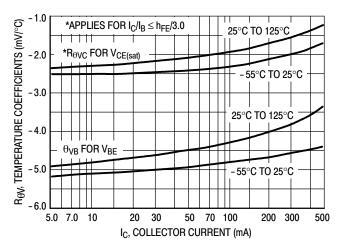


Figure 10. "On" Voltages

Figure 11. Temperature Coefficients

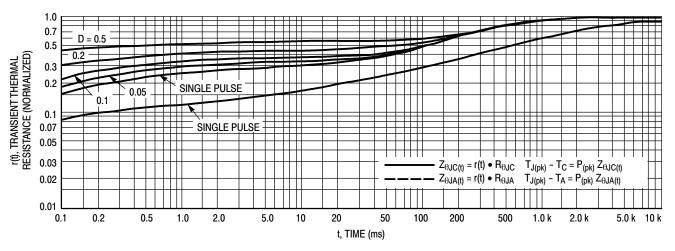
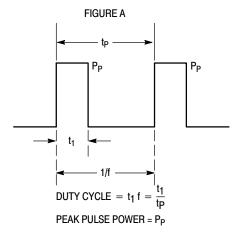


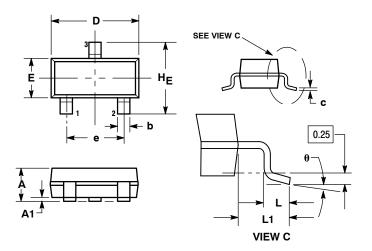
Figure 12. Thermal Response



Design Note: Use of Transient Thermal Resistance Data

PACKAGE DIMENSIONS

SOT-23 (TO-236) CASE 318-08 ISSUE AN



NOTES:

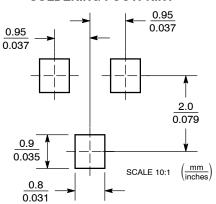
- DIMENSIONING AND TOLERANCING PER ANSI
 V14 5M 1982
- Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH.
- 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
- 318-01 THRU -07 AND -09 OBSOLETE, NEW STANDARD 318-08.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	MOM	MAX
Α	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
С	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
е	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.40	2.64	0.083	0.094	0.104

STYLE 6: PIN 1. BASE

2. EMITTER 3. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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