PBSS5350D

50 V, 3 A PNP low VCEsat (BISS) transistor

Rev. 5 — 23 March 2011 Product data sheet

1. Product profile

1.1 General description

PNP low V_{CEsat} Breakthrough In Small Signal (BISS) transistor in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package.

NPN complement: PBSS4350D

1.2 Features and benefits

- Low collector-emitter saturation voltage V_{CEsat}
- High current capability
- High efficiency due to less heat generation
- AEC-Q101 qualified
- Smaller Printed-Circuit Board (PCB) area than for conventional transistors

1.3 Applications

- Supply line switching circuits
- Battery management applications
- DC-to-DC conversion

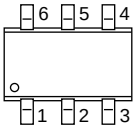
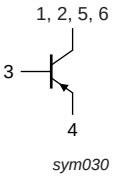
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CEO}	collector-emitter voltage	open base	-	-	-50	V
I_C	collector current		-	-	-3	A
I_{CM}	peak collector current		-	-	-5	A
R_{CEsat}	collector-emitter saturation resistance	I_C = -2 A; I_B = -200 mA; pulsed; $t_p \leq 300$ µs; $\delta \leq 0.02$; T_{amb} = 25 °C	-	120	150	mΩ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	C	collector		
2	C	collector		
3	B	base		
4	E	emitter		
5	C	collector	SOT457 (TSOP6)	sym030
6	C	collector		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBSS5350D	TSOP6	plastic surface-mounted package (TSOP6); 6 leads	SOT457

4. Marking

Table 4. Marking codes

Type number	Marking code[1]
PBSS5350D	53

[1] % = placeholder for manufacturing site code

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter		-	-60	V
V_{CEO}	collector-emitter voltage	open base		-	-50	V
V_{EBO}	emitter-base voltage	open collector		-	-6	V
I_C	collector current			-	-3	A
I_{CM}	peak collector current			-	-5	A
I_{BM}	peak base current			-	-1	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	600	mW
			[2]	-	750	mW
		$T_{amb} \leq 25$ °C; pulsed; $t_p \leq 50$ ms; $\delta \leq 0.5$	[2]	-	1200	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-65	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for collector 1 cm^2.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm^2.

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	208	K/W
			[2]	-	-	160	K/W
		in free air; pulsed; $t_p \leq 50$ ms; $\delta \leq 0.5$	[2]	-	-	100	K/W

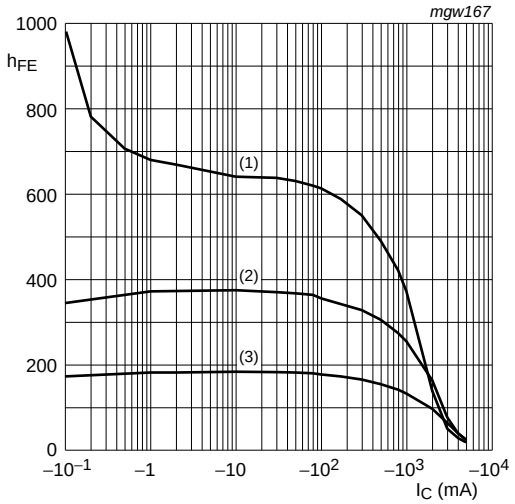
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm^2.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm^2.

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CBO}	collector-base cut-off current	V_{CB} = -50 V; I_E = 0 A; T_{amb} = 25 °C	-	-	-100	nA
		V_{CB} = -50 V; I_E = 0 A; T_j = 150 °C	-	-	-50	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = -5 V; I_C = 0 A; T_{amb} = 25 °C	-	-	-100	nA
h_{FE}	DC current gain	V_{CE} = -2 V; I_C = -500 mA; T_{amb} = 25 °C	200	-	-	
		V_{CE} = -2 V; I_C = -1 A; pulsed; $t_p \leq 300$ µs; $\delta \leq 0.02$; T_{amb} = 25 °C	200	-	-	
		V_{CE} = -2 V; I_C = -2 A; pulsed; $t_p \leq 300$ µs; $\delta \leq 0.02$; T_{amb} = 25 °C	100	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = -500 mA; I_B = -50 mA; T_{amb} = 25 °C	-	-	-100	mV
		I_C = -1 A; I_B = -50 mA; T_{amb} = 25 °C	-	-	-180	mV
		I_C = -2 A; I_B = -200 mA; pulsed; $t_p \leq 300$ µs; $\delta \leq 0.02$; T_{amb} = 25 °C	-	-	-300	mV
R_{CEsat}	collector-emitter saturation resistance		-	120	150	mΩ
V_{BEsat}	base-emitter saturation voltage		-	-	-1.2	V
V_{BEon}	base-emitter turn-on voltage	V_{CE} = -2 V; I_C = -1 A; pulsed; $t_p \leq 300$ µs; $\delta \leq 0.02$; T_{amb} = 25 °C	-	-	-1.1	V
f_T	transition frequency	V_{CE} = -5 V; I_C = -100 mA; f = 100 MHz; T_{amb} = 25 °C	100	-	-	MHz
C_c	collector capacitance	V_{CB} = -10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C	-	-	40	pF



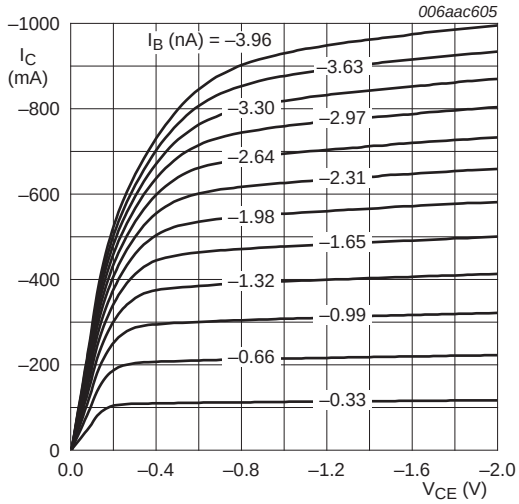
V_{CE} = -2 V

(1) T_{amb} = 150 °C

(2) T_{amb} = 25 °C

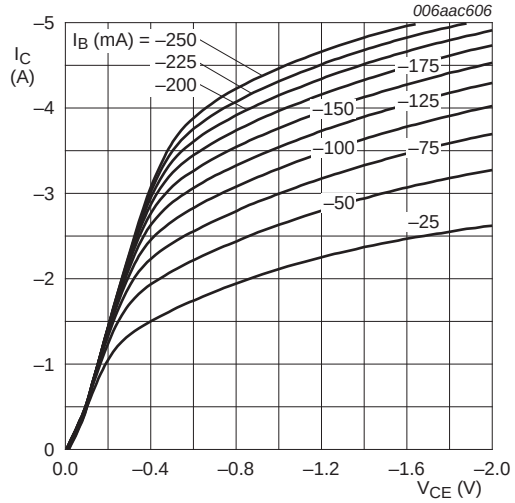
(3) T_{amb} = -55 °C

Fig 1. DC current gain as a function of collector current; typical values



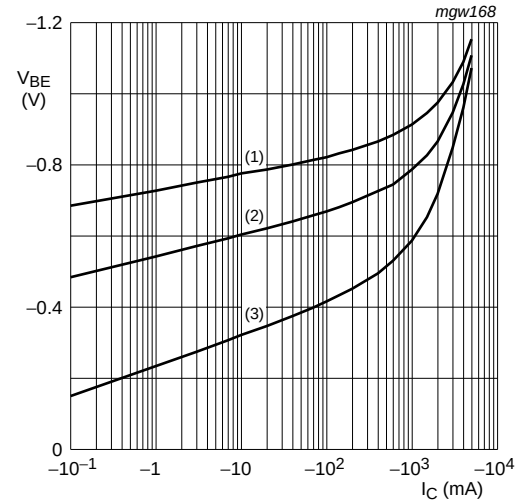
T_{amb} = 25 °C

Fig 2. Collector current as a function of collector-emitter voltage; typical values



T_{amb} = 25 °C

Fig 3. Collector current as a function of collector-emitter voltage; typical values



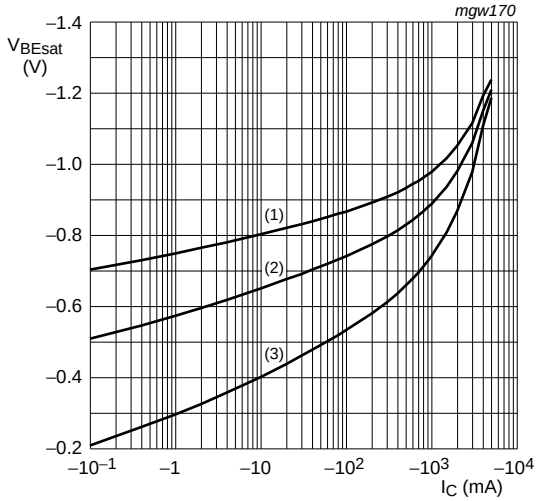
V_{CE} = -2 V

(1) T_{amb} = -55 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 150 °C

Fig 4. Base-emitter voltage as a function of collector current; typical values



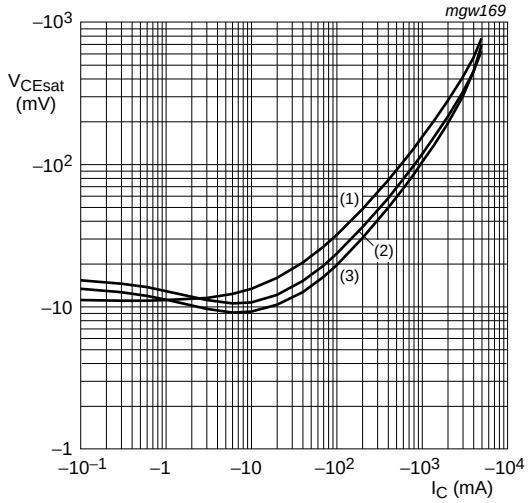
I_C/I_B = 10

(1) T_{amb} = -55 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 150 °C

Fig 5. Base-emitter saturation voltage as a function of collector current; typical values



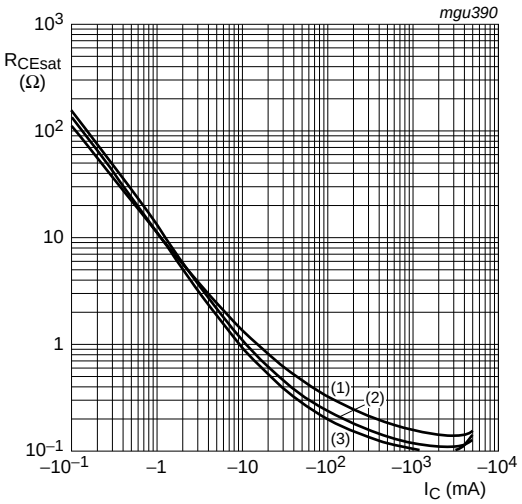
I_C/I_B = 10

(1) T_{amb} = 150 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = -55 °C

Fig 6. Collector-emitter saturation voltage as a function of collector current; typical values



I_C/I_B = 20

(1) T_{amb} = 150 °C

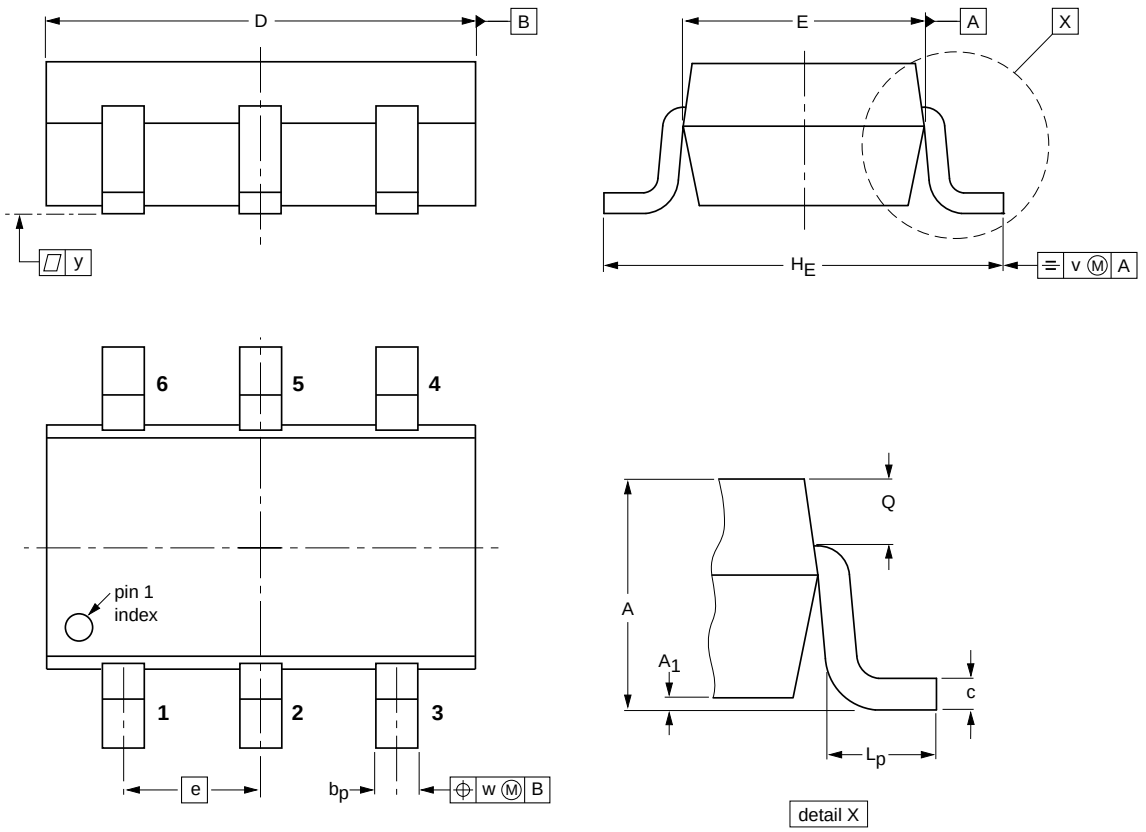
(2) T_{amb} = 25 °C

(3) T_{amb} = -55 °C

Fig 7. Collector-emitter saturation resistance as a function of collector current; typical values

8. Package outline

Plastic surface-mounted package (TSOP6); 6 leads **SOT457**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT457			SC-74			~~05-11-07~~ 06-03-16

Fig 8. Package outline SOT457 (TSOP6)

9. Soldering

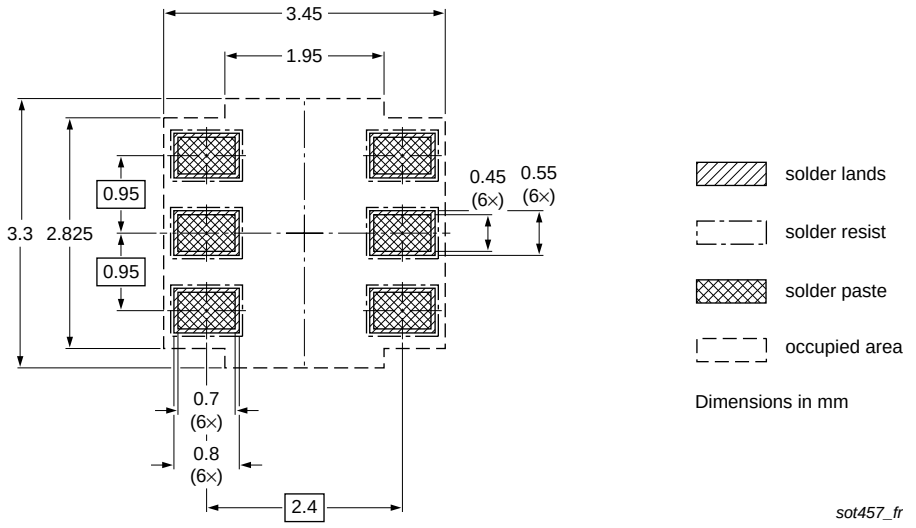


Fig 9. Reflow soldering footprint for SOT457 (TSOP6)

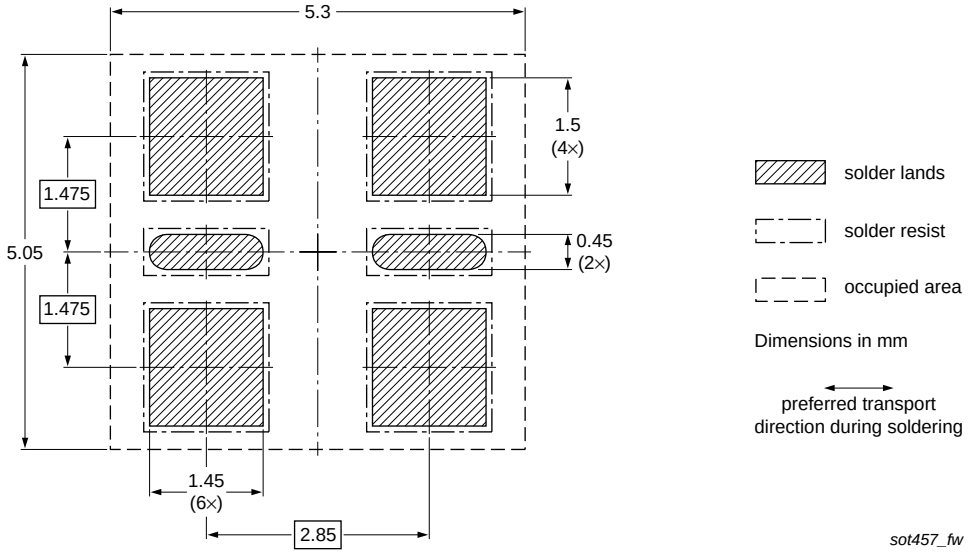


Fig 10. Wave soldering footprint for SOT457 (TSOP6)

10. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PBSS5350D v.5	20110323	Product data sheet	-	PBSS5350D v.4
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • 1 “Product profile”: updated. • Figures 2 and 3: updated. • 5 “Limiting values”: P_{tot} updated. • 6 “Thermal characteristics”: updated. • 8 “Package outline”: updated. • 9 “Soldering”: added. • 11 “Legal information”: updated.			
PBSS5350D v.4	20011113	Product specification	-	PBSS5350D v.3
PBSS5350D v.3	20010713	Product specification	-	PBSS5350D v.2
PBSS5350D v.2	20010126	Product specification	-	PBSS5350D v.1
PBSS5350D v.1	20000308	Product specification	-	-

11. Legal information

11.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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13. Contents

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Date of release: 23 March 2011
Document identifier: PBSS5350D