

EMC2DXV5T1G, EMC3DXV5T1G, EMC4DXV5T1G, EMC5DXV5T1G

Dual Common Base-Collector Bias Resistor Transistors

NPN and PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the EMC2DXV5T1 series, two complementary BRT devices are housed in the SOT-553 package which is ideal for low power surface mount applications where board space is at a premium.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- These are Pb-Free Devices

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted, common for Q_1 and Q_2 , - minus sign for Q_1 (PNP) omitted)

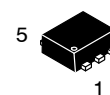
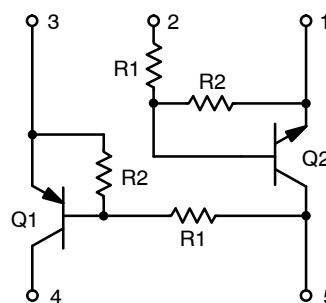
Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



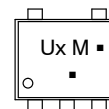
ON Semiconductor®

<http://onsemi.com>



SOT-553
CASE 463B

MARKING DIAGRAM



Ux = Specific Device Code
x = C, 3, E, or 5

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

EMC2DXV5T1G, EMC3DXV5T1G, EMC4DXV5T1G, EMC5DXV5T1G

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
ONE JUNCTION HEATED			
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	357 (Note 1) 2.9 (Note 1)	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	350 (Note 1)	$^\circ\text{C}/\text{W}$
BOTH JUNCTIONS HEATED			
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	500 (Note 1) 4.0 (Note 1)	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	250 (Note 1)	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

1. FR-4 @ Minimum Pad

DEVICE ORDERING INFORMATION, MARKING AND RESISTOR VALUES

Device	Marking	Transistor 1 - PNP		Transistor 2 - NPN		Package	Shipping [†]
		R1 (K)	R2 (K)	R1 (K)	R2 (K)		
EMC2DXV5T1G	UC	22	22	22	22	SOT-553*	4000 / Tape & Reel
EMC3DXV5T1G	U3	10	10	10	10	SOT-553*	4000 / Tape & Reel
EMC3DXV5T5G						SOT-553*	8000 / Tape & Reel
EMC4DXV5T1G	UE	10	47	47	47	SOT-553*	4000 / Tape & Reel
EMC5DXV5T1G	U5	4.7	10	47	47	SOT-553*	4000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

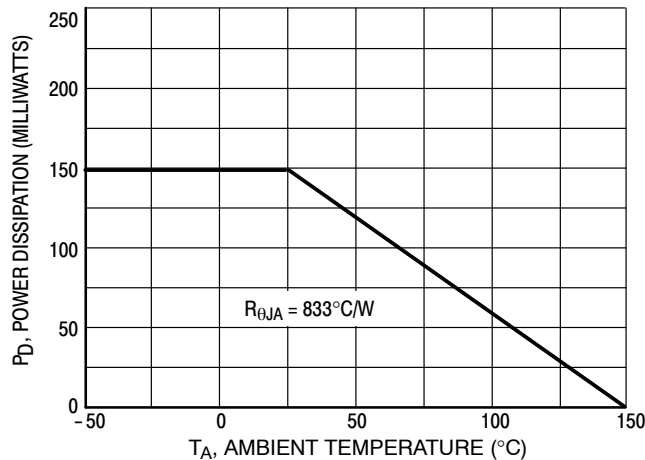


Figure 1. Derating Curve

EMC2DXV5T1G, EMC3DXV5T1G, EMC4DXV5T1G, EMC5DXV5T1G

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Q1 TRANSISTOR: PNP OFF CHARACTERISTICS					
Collector-Base Cutoff Current (V _{CB} = 50 V, I _E = 0)	I _{CBO}	-	-	100	nAdc
Collector-Emitter Cutoff Current (V _{CB} = 50 V, I _B = 0)	I _{CEO}	-	-	500	nAdc
Emitter-Base Cutoff Current (V _{EB} = 6.0 V, I _C = 0)	I _{EBO}	-	-	0.2	mAdc
	EMC2DXV5T1	-	-	0.5	
	EMC3DXV5T1	-	-	0.2	
	EMC4DXV5T1	-	-	1.0	
	EMC5DXV5T1	-	-		

ON CHARACTERISTICS

Collector-Base Breakdown Voltage (I _C = 10 μA, I _E = 0)	V _{(BR)CBO}	50	-	-	Vdc
Collector-Emitter Breakdown Voltage (I _C = 2.0 mA, I _B = 0)	V _{(BR)CEO}	50	-	-	Vdc
DC Current Gain (V _{CE} = 10 V, I _C = 5.0 mA)	h _{FE}	60	100	-	
	EMC2DXV5T1	35	60	-	
	EMC3DXV5T1	80	140	-	
	EMC4DXV5T1	20	35	-	
	EMC5DXV5T1				
Collector-Emitter Saturation Voltage (I _C = 10 mA, I _B = 0.3 mA)	V _{CE(SAT)}	-	-	0.25	Vdc
Output Voltage (on) (V _{CC} = 5.0 V, V _B = 2.5 V, R _L = 1.0 kΩ)	V _{OL}	-	-	0.2	Vdc
Output Voltage (off) (V _{CC} = 5.0 V, V _B = 0.5 V, R _L = 1.0 kΩ)	V _{OH}	4.9	-	-	Vdc
Input Resistor	R1	15.4	22	28.6	kΩ
	EMC2DXV5T1	7.0	10	13	
	EMC3DXV5T1, EMC4DXV5T1	3.3	4.7	6.1	
	EMC5DXV5T1				
Resistor Ratio	R1/R2	0.8	1.0	1.2	
	EMC2DXV5T1	0.8	1.0	1.2	
	EMC3DXV5T1	0.17	0.21	0.25	
	EMC4DXV5T1	0.38	0.47	0.56	
	EMC5DXV5T1				

Q2 TRANSISTOR: NPN OFF CHARACTERISTICS

Collector-Base Cutoff Current (V _{CB} = 50 V, I _E = 0)	I _{CBO}	-	-	100	nAdc
Collector-Emitter Cutoff Current (V _{CB} = 50 V, I _B = 0)	I _{CEO}	-	-	500	nAdc
Emitter-Base Cutoff Current (V _{EB} = 6.0 V, I _C = 0)	I _{EBO}	-	-	0.2	mAdc
	EMC2DXV5T1	-	-	0.5	
	EMC3DXV5T1	-	-	0.1	
	EMC4DXV5T1, EMC5DXV5T1	-	-		

ON CHARACTERISTICS

Collector-Base Breakdown Voltage (I _C = 10 μA, I _E = 0)	V _{(BR)CBO}	50	-	-	Vdc
Collector-Emitter Breakdown Voltage (I _C = 2.0 mA, I _B = 0)	V _{(BR)CEO}	50	-	-	Vdc
DC Current Gain (V _{CE} = 10 V, I _C = 5.0 mA)	h _{FE}	60	100	-	
	EMC2DXV5T1	35	60	-	
	EMC3DXV5T1	80	140	-	
	EMC4DXV5T1, EMC5DXV5T1				
Collector-Emitter Saturation Voltage (I _C = 10 mA, I _B = 0.3 mA)	V _{CE(SAT)}	-	-	0.25	Vdc
Output Voltage (on) (V _{CC} = 5.0 V, V _B = 2.5 V, R _L = 1.0 kΩ)	V _{OL}	-	-	0.2	Vdc
Output Voltage (off) (V _{CC} = 5.0 V, V _B = 0.5 V, R _L = 1.0 kΩ)	V _{OH}	4.9	-	-	Vdc
Input Resistor	R1	15.4	22	28.6	kΩ
	EMC2DXV5T1	7.0	10	13	
	EMC3DXV5T1	33	47	61	
	EMC4DXV5T1, EMC5DXV5T1				
Resistor Ratio	R1/R2	0.8	1.0	1.2	
	EMC2DXV5T1	0.8	1.0	1.2	
	EMC3DXV5T1	0.8	1.0	1.2	
	EMC4DXV5T1, EMC5DXV5T1	0.8	1.0	1.2	

EMC2DXV5T1G, EMC3DXV5T1G, EMC4DXV5T1G, EMC5DXV5T1G

TYPICAL ELECTRICAL CHARACTERISTICS – EMC2DXV5T1 PNP TRANSISTOR

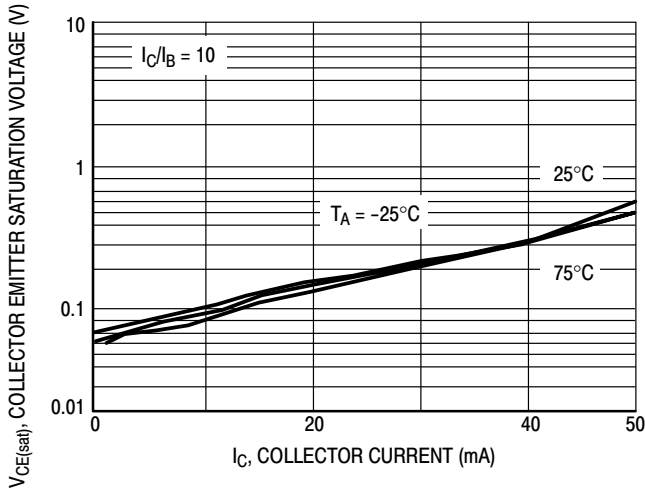


Figure 2. $V_{CE(sat)}$ versus I_C

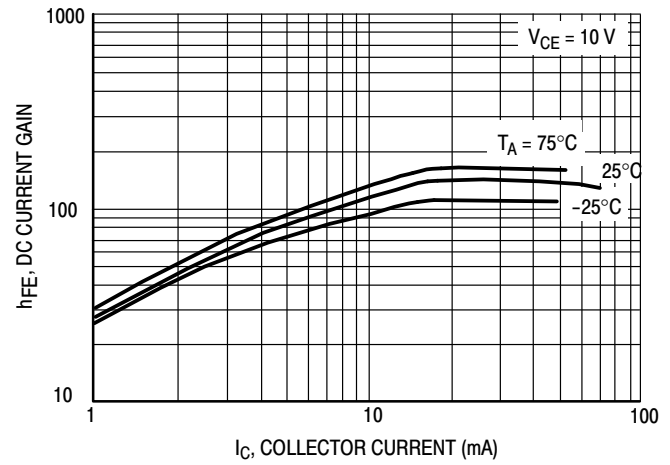


Figure 3. DC Current Gain

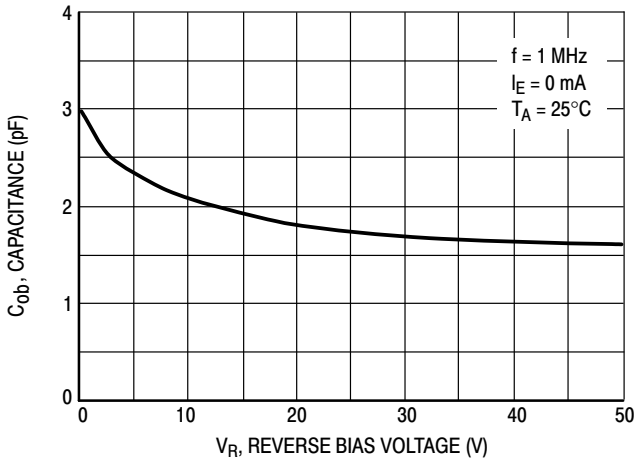


Figure 4. Output Capacitance

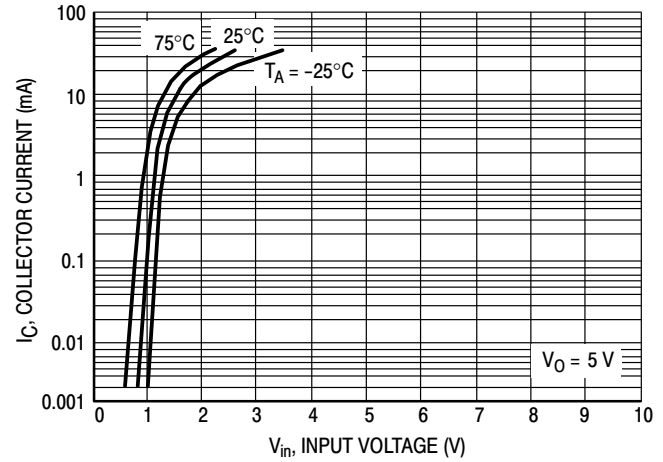


Figure 5. Output Current versus Input Voltage

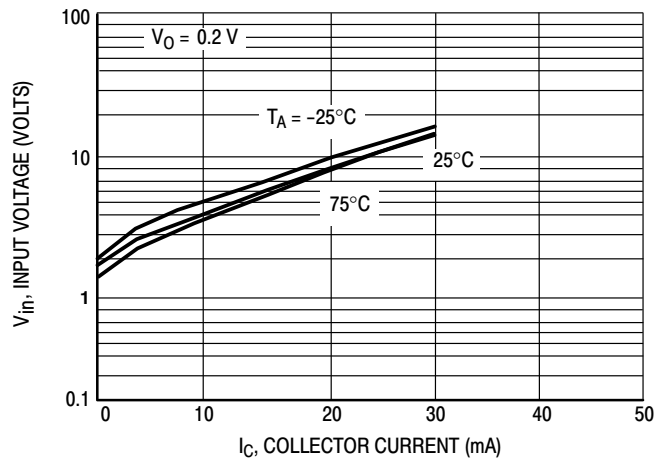


Figure 6. Input Voltage versus Output Current

EMC2DXV5T1G, EMC3DXV5T1G, EMC4DXV5T1G, EMC5DXV5T1G

TYPICAL ELECTRICAL CHARACTERISTICS – EMC2DXV5T1 NPN TRANSISTOR

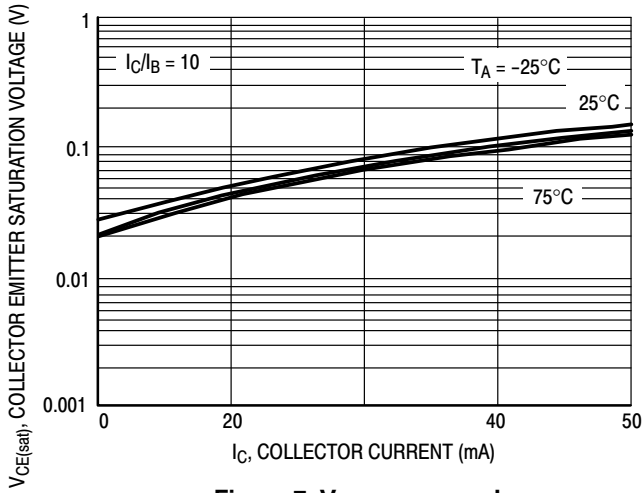


Figure 7. $V_{CE(sat)}$ versus I_C

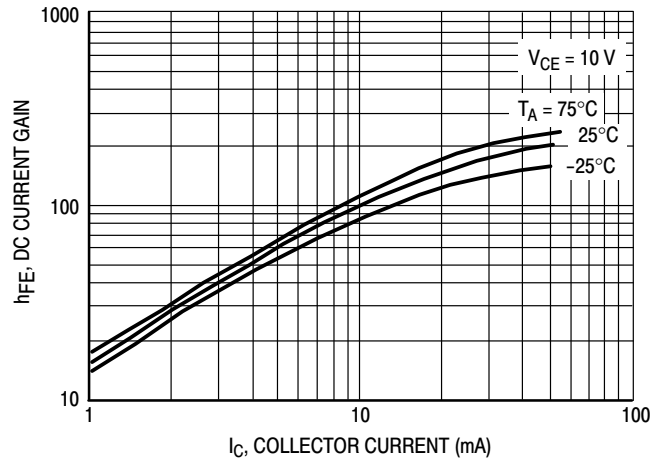


Figure 8. DC Current Gain

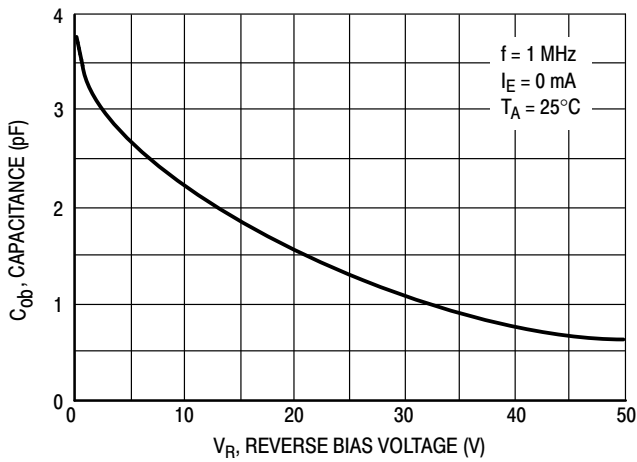


Figure 9. Output Capacitance

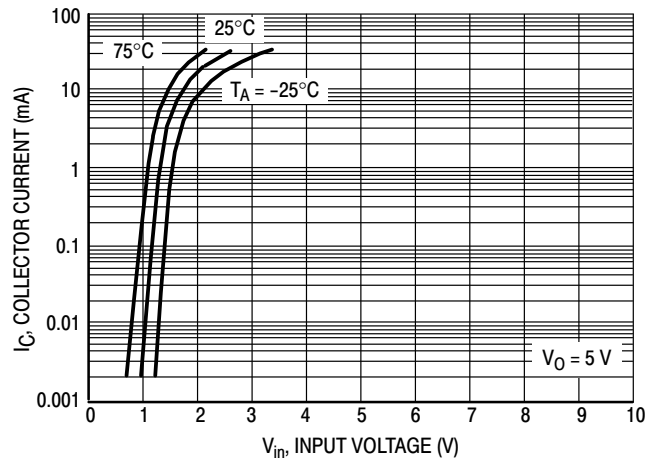


Figure 10. Output Current versus Input Voltage

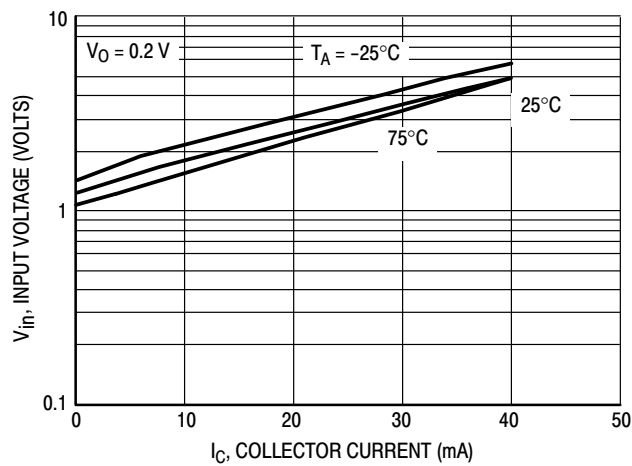


Figure 11. Input Voltage versus Output Current

EMC2DXV5T1G, EMC3DXV5T1G, EMC4DXV5T1G, EMC5DXV5T1G

TYPICAL ELECTRICAL CHARACTERISTICS – EMC3DXV5T1 PNP TRANSISTOR

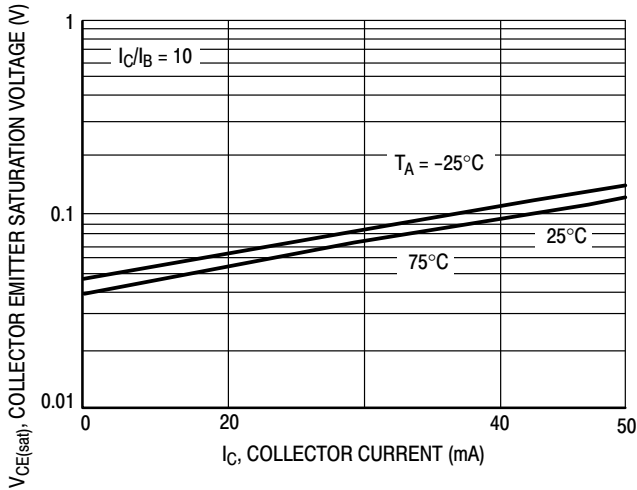


Figure 12. $V_{CE(sat)}$ versus I_C

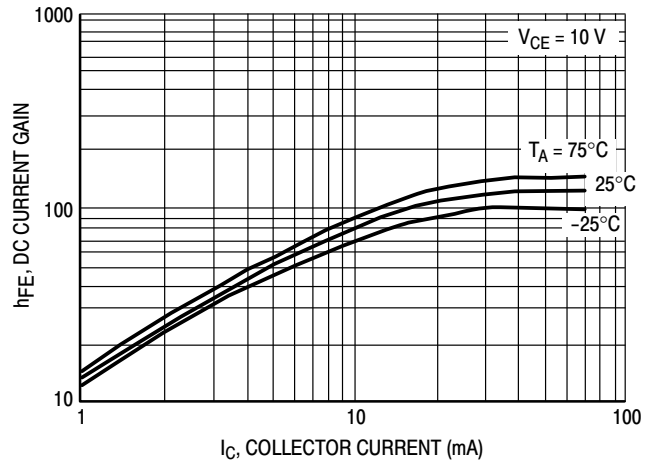


Figure 13. DC Current Gain

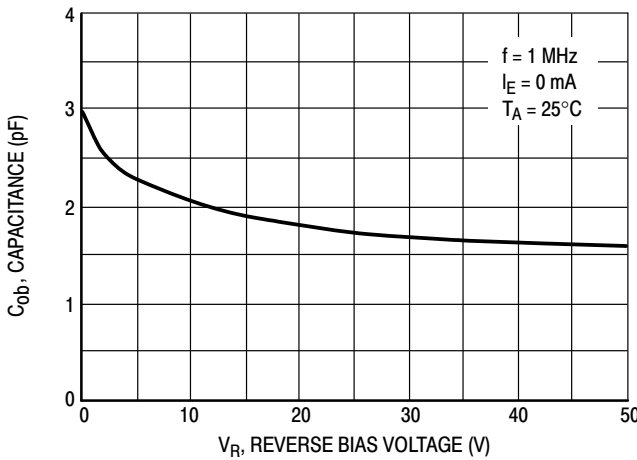


Figure 14. Output Capacitance

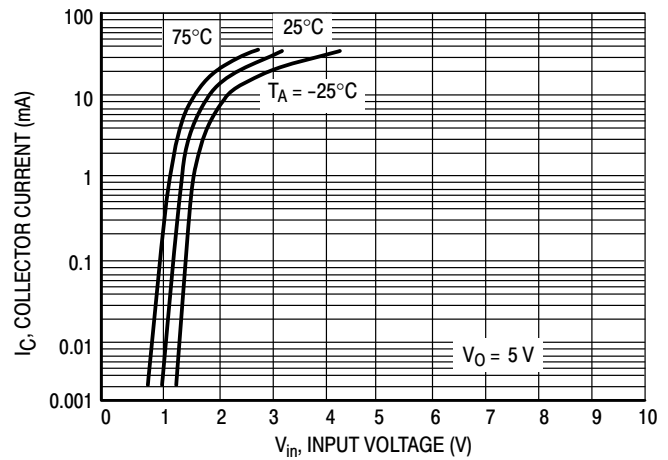


Figure 15. Output Current versus Input Voltage

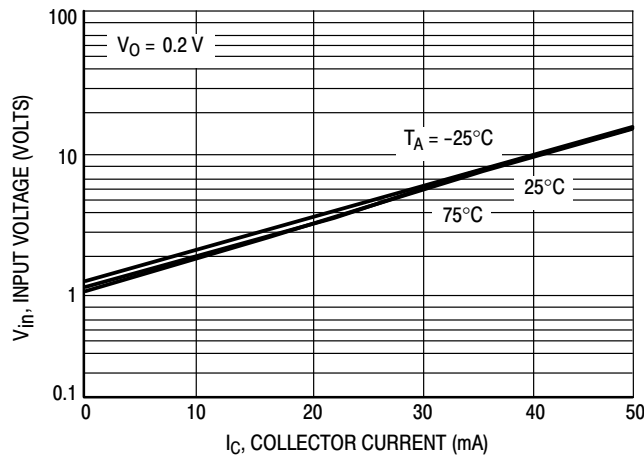


Figure 16. Input Voltage versus Output Current

EMC2DXV5T1G, EMC3DXV5T1G, EMC4DXV5T1G, EMC5DXV5T1G

TYPICAL ELECTRICAL CHARACTERISTICS – EMC3DXV5T1 NPN TRANSISTOR

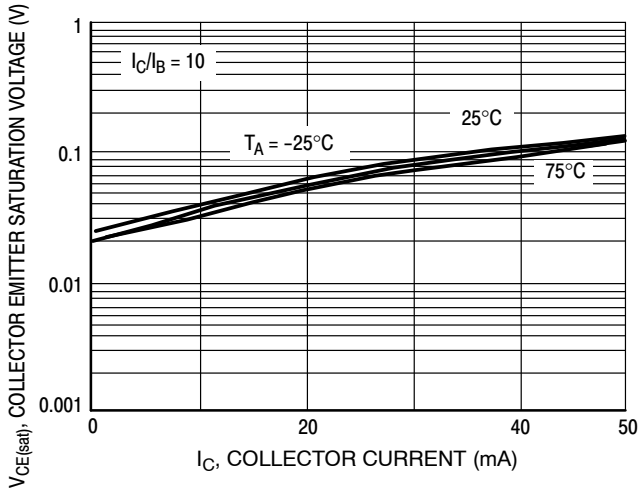


Figure 17. $V_{CE(sat)}$ versus I_C

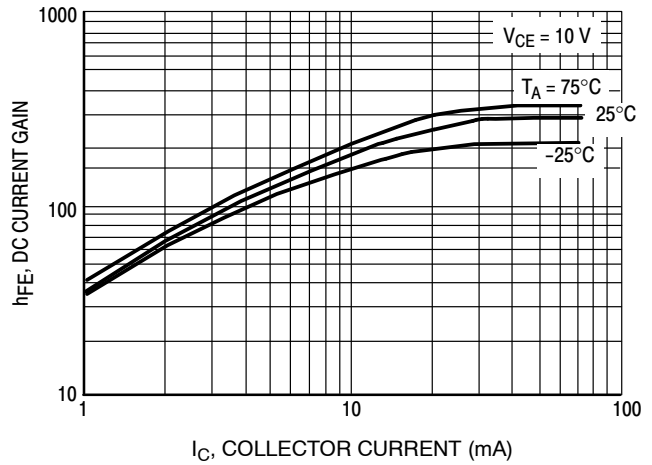


Figure 18. DC Current Gain

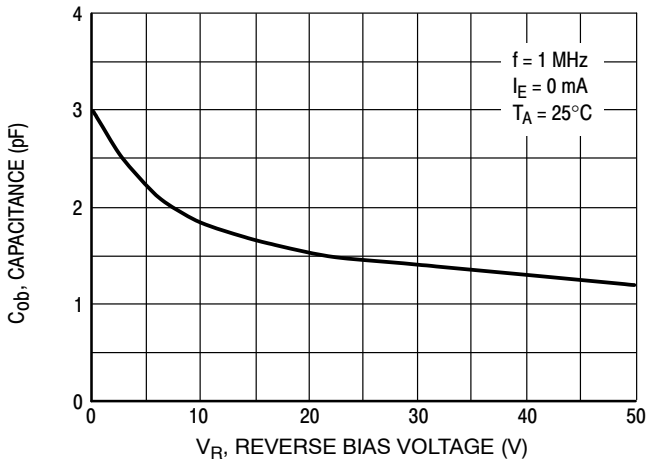


Figure 19. Output Capacitance

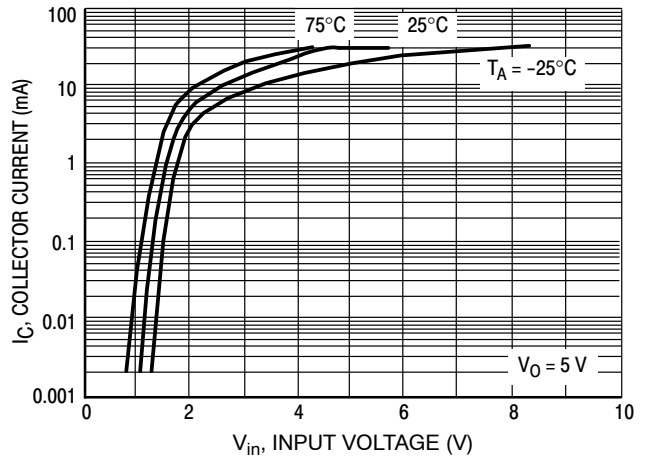


Figure 20. Output Current versus Input Voltage

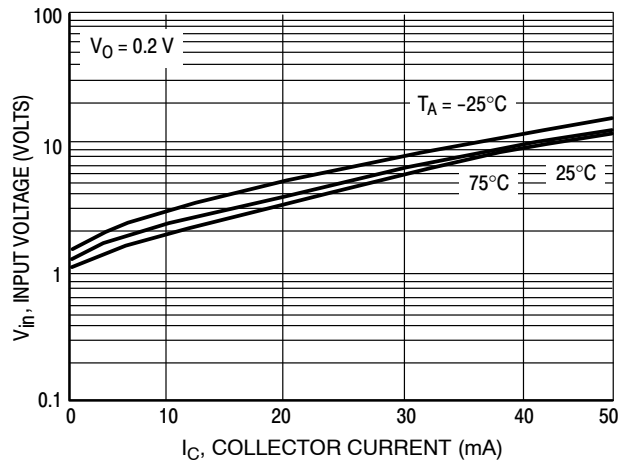


Figure 21. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS – EMC4DXV5T1 PNP TRANSISTOR

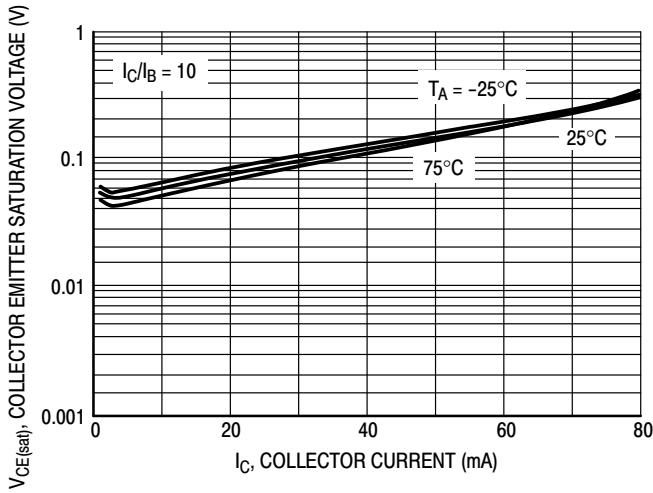


Figure 22. $V_{CE(sat)}$ versus I_C

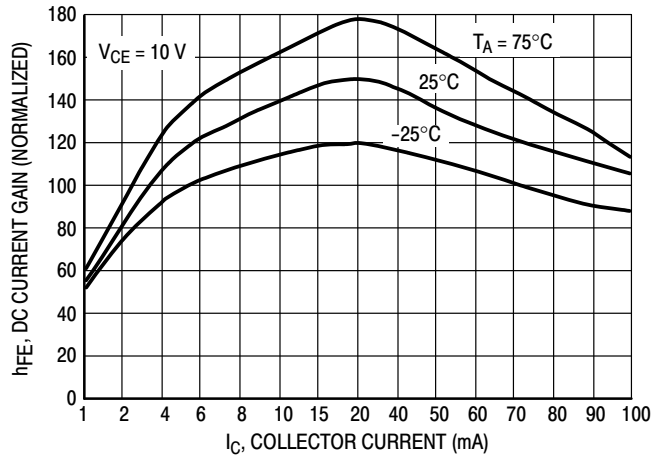


Figure 23. DC Current Gain

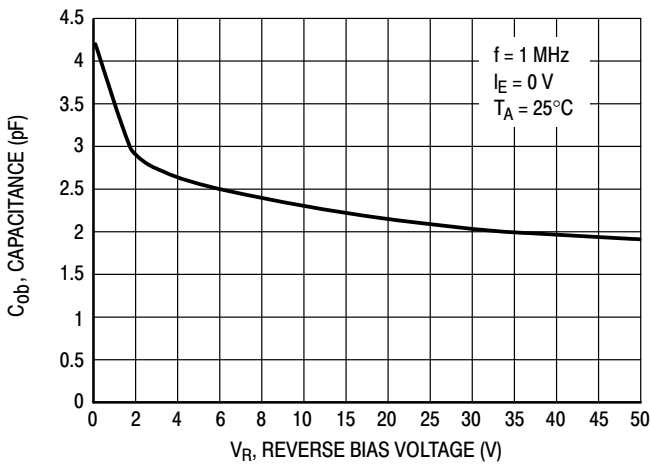


Figure 24. Output Capacitance

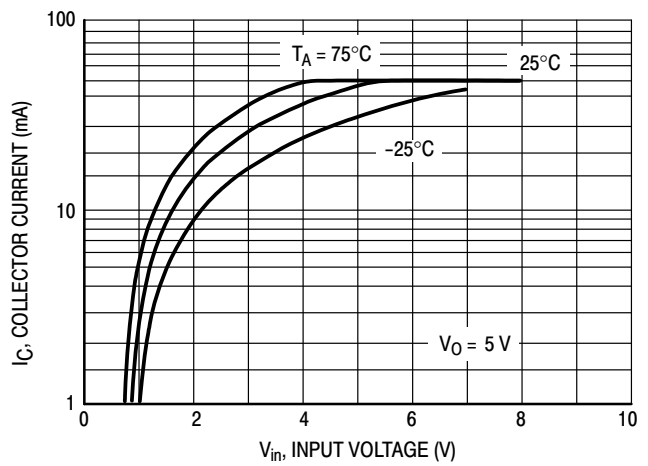


Figure 25. Output Current versus Input Voltage

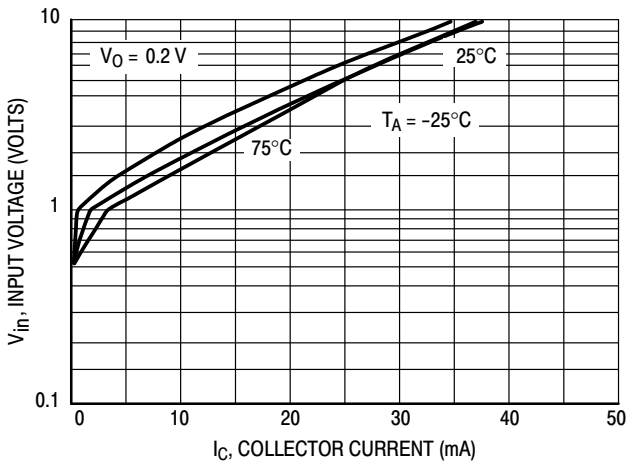


Figure 26. Input Voltage versus Output Current

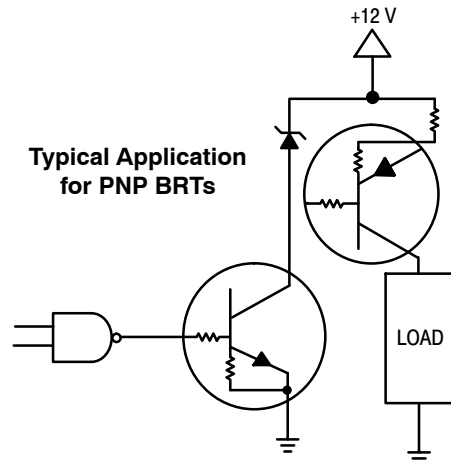


Figure 27. Inexpensive, Unregulated Current Source

EMC2DXV5T1G, EMC3DXV5T1G, EMC4DXV5T1G, EMC5DXV5T1G

TYPICAL ELECTRICAL CHARACTERISTICS – EMC5DXV5T1 PNP TRANSISTOR

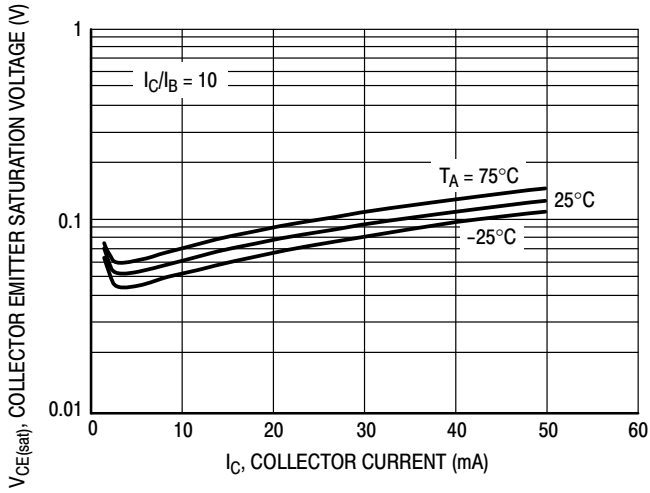


Figure 28. $V_{CE(sat)}$ versus I_C

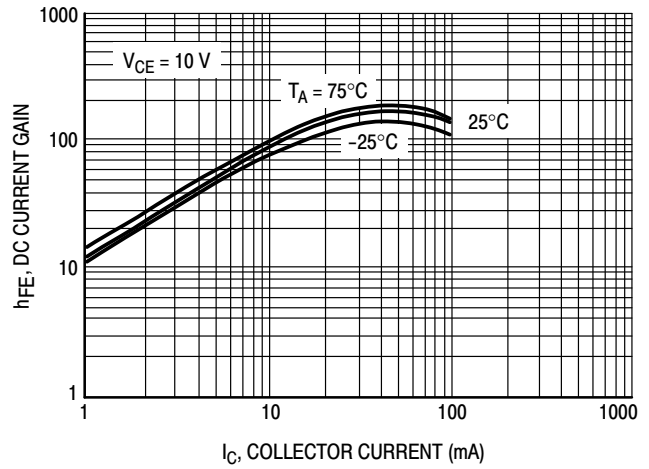


Figure 29. DC Current Gain

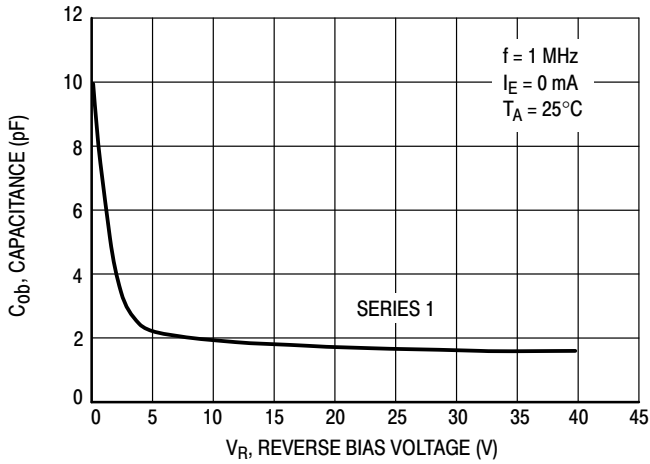


Figure 30. Output Capacitance

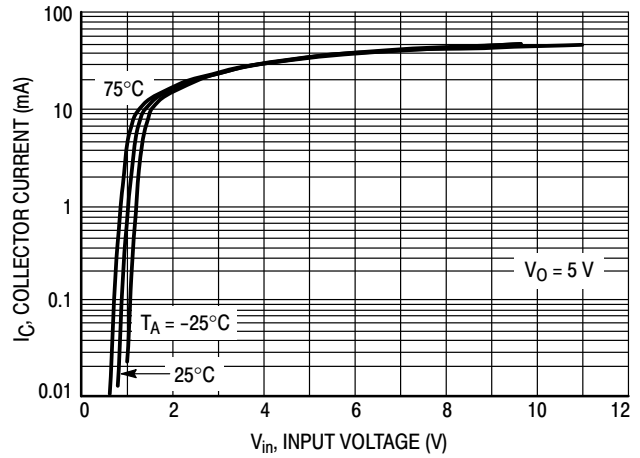


Figure 31. Output Current versus Input Voltage

EMC2DXV5T1G, EMC3DXV5T1G, EMC4DXV5T1G, EMC5DXV5T1G

TYPICAL ELECTRICAL CHARACTERISTICS – EMC4DXV5T1, EMC5DXV5T1 NPN TRANSISTOR

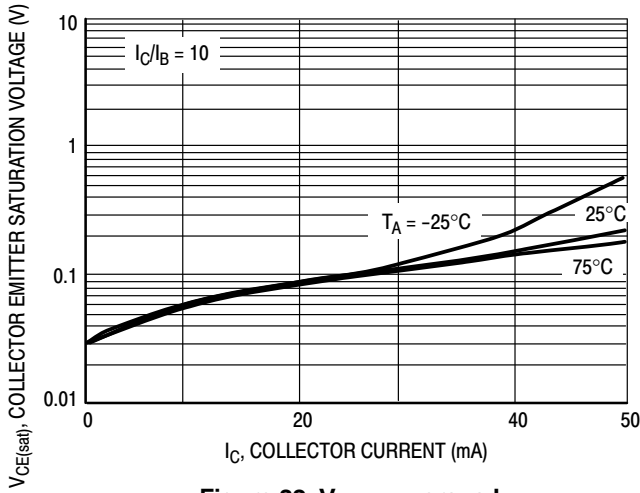


Figure 32. $V_{CE(sat)}$ versus I_C

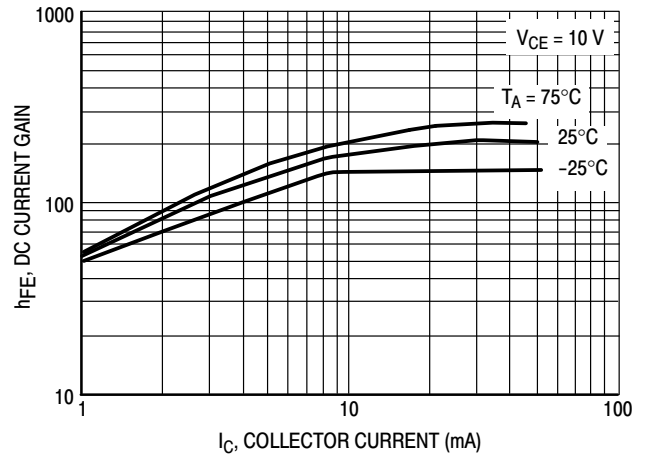


Figure 33. DC Current Gain

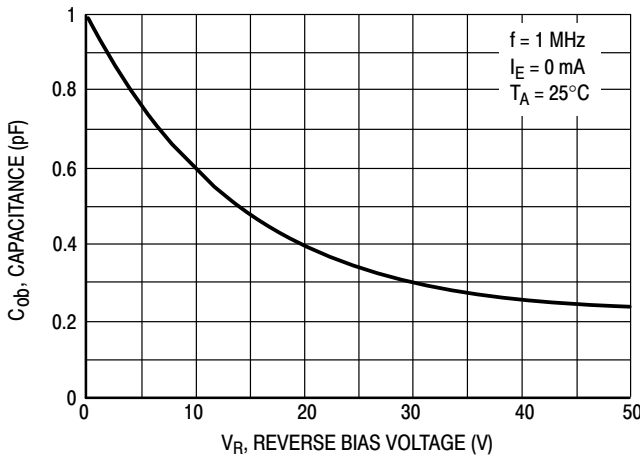


Figure 34. Output Capacitance

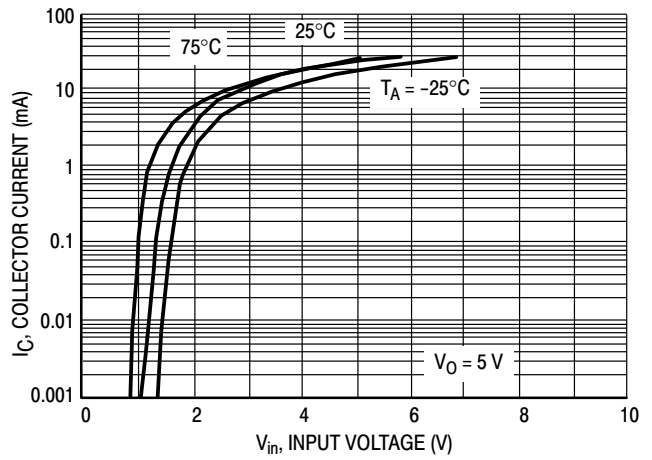


Figure 35. Output Current versus Input Voltage

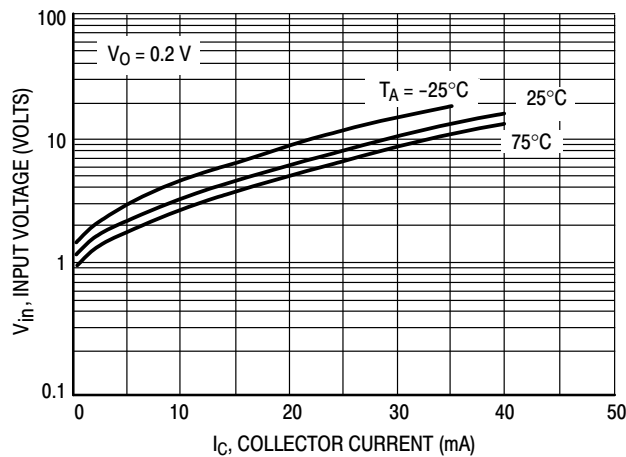
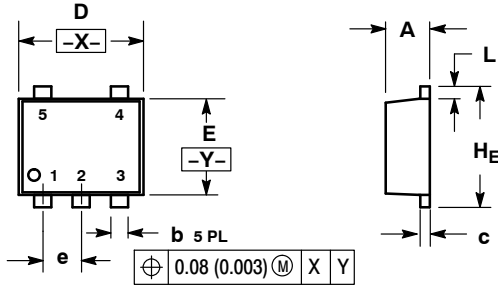


Figure 36. Input Voltage versus Output Current

EMC2DXV5T1G, EMC3DXV5T1G, EMC4DXV5T1G, EMC5DXV5T1G

PACKAGE DIMENSIONS

SOT-553
XV5 SUFFIX
CASE 463B-01
ISSUE B

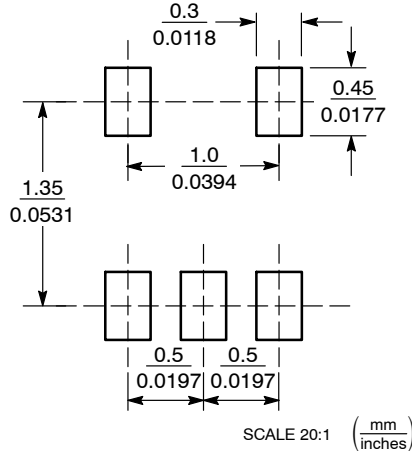


NOTES:


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.08	0.13	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.063	0.067
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.50 BSC			0.020 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
HE	1.50	1.60	1.70	0.059	0.063	0.067

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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