



RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for broadband commercial and industrial applications with frequencies up to 1000 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common-source amplifier applications in 28 volt base station equipment.

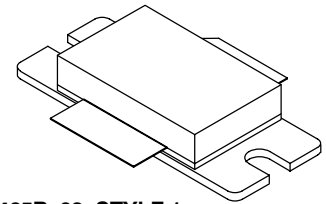
- Typical Single-Carrier W-CDMA Performance: $V_{DD} = 28$ Volts, $I_{DQ} = 1400$ mA, $P_{out} = 58$ Watts Avg., Full Frequency Band, 3GPP Test Model 1, 64 DPCH with 50% Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.
Power Gain — 21.2 dB
Drain Efficiency — 34%
Device Output Signal PAR — 6.3 dB @ 0.01% Probability on CCDF
ACPR @ 5 MHz Offset — -39.1 dBc in 3.84 MHz Channel Bandwidth
- Capable of Handling 10:1 VSWR, @ 32 Vdc, 880 MHz, $P_{out} = 260$ W CW (3 dB Input Overdrive from Rated P_{out}), Designed for Enhanced Ruggedness

Features

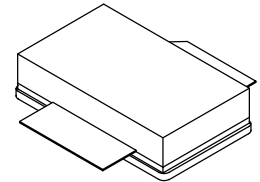
- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Qualified Up to a Maximum of 32 V_{DD} Operation
- Integrated ESD Protection
- Optimized for Doherty Applications
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

MRFE6S9205HR3
MRFE6S9205HSR3

880 MHz, 58 W AVG., 28 V
SINGLE W-CDMA
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465B-03, STYLE 1
NI-880
MRFE6S9205HR3



CASE 465C-02, STYLE 1
NI-880S
MRFE6S9205HSR3

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +66	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +12	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 202 W CW Case Temperature 77°C, 58 W CW	$R_{\theta JC}$	0.27 0.33	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Tools (Software & Tools)/Calculators to access the MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	Class 1C (Minimum)
Machine Model (per EIA/JESD22-A115)	Class B (Minimum)
Charge Device Model (per JESD22-C101)	Class IV (Minimum)

Table 4. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 66\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	10	μAdc

On Characteristics

Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 600\ \mu\text{Adc}$)	$V_{GS(th)}$	1.4	2.1	2.9	Vdc
Gate Quiescent Voltage ($V_{DD} = 28\text{ Vdc}$, $I_D = 1400\ \text{mAdc}$, Measured in Functional Test)	$V_{GS(Q)}$	2.2	2.9	3.7	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 4.2\ \text{Adc}$)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

Dynamic Characteristics ⁽¹⁾

Reverse Transfer Capacitance ($V_{DS} = 28\text{ Vdc} \pm 30\ \text{mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{rss}	—	1.63	—	pF
Output Capacitance ($V_{DS} = 28\text{ Vdc} \pm 30\ \text{mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{oss}	—	590	—	pF
Input Capacitance ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc} \pm 30\ \text{mV(rms)ac}$ @ 1 MHz)	C_{iss}	—	491	—	pF

Functional Tests (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 1400\ \text{mA}$, $P_{out} = 58\ \text{W Avg. W-CDMA}$, $f = 880\ \text{MHz}$, Single-Carrier W-CDMA, 3.84 MHz Channel Bandwidth Carrier. ACPR measured in 3.84 MHz Channel Bandwidth @ 5 MHz Offset. PAR = 7.5 dB @ 0.01% Probability on CCDF.

Power Gain	G_{ps}	20	21.2	23	dB
Drain Efficiency	η_D	32	34	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6	6.3	—	dB
Adjacent Channel Power Ratio	ACPR	—	-39.1	-37.5	dBc
Input Return Loss	IRL	—	-12.5	-8.5	dB

1. Part is internally matched on input.

(continued)

Table 4. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 1400 \text{ mA}$, 865-900 MHz Bandwidth					
Video Bandwidth @ 220 W PEP P_{out} where $IM3 = -30 \text{ dBc}$ (Tone Spacing from 100 kHz to VBW) $\Delta IMD3 = IMD3 @ \text{VBW}$ frequency - $IMD3 @ 100 \text{ kHz} < 1 \text{ dBc}$ (both sidebands)	VBW	—	10	—	MHz
Gain Flatness in 35 MHz Bandwidth @ $P_{out} = 58 \text{ W Avg.}$	G_F	—	0.315	—	dB
Average Deviation from Linear Phase in 35 MHz Bandwidth @ $P_{out} = 200 \text{ W CW}$	Φ	—	0.59	—	°
Average Group Delay @ $P_{out} = 200 \text{ W CW}$, $f = 880 \text{ MHz}$	Delay	—	4.27	—	ns
Part-to-Part Insertion Phase Variation @ $P_{out} = 200 \text{ W CW}$, $f = 880 \text{ MHz}$, Six Sigma Window	$\Delta\Phi$	—	26.3	—	°
Gain Variation over Temperature (-30°C to $+85^\circ\text{C}$)	ΔG	—	0.016	—	dB/°C
Output Power Variation over Temperature (-30°C to $+85^\circ\text{C}$)	ΔP_{1dB}	—	0.006	—	dBm/°C

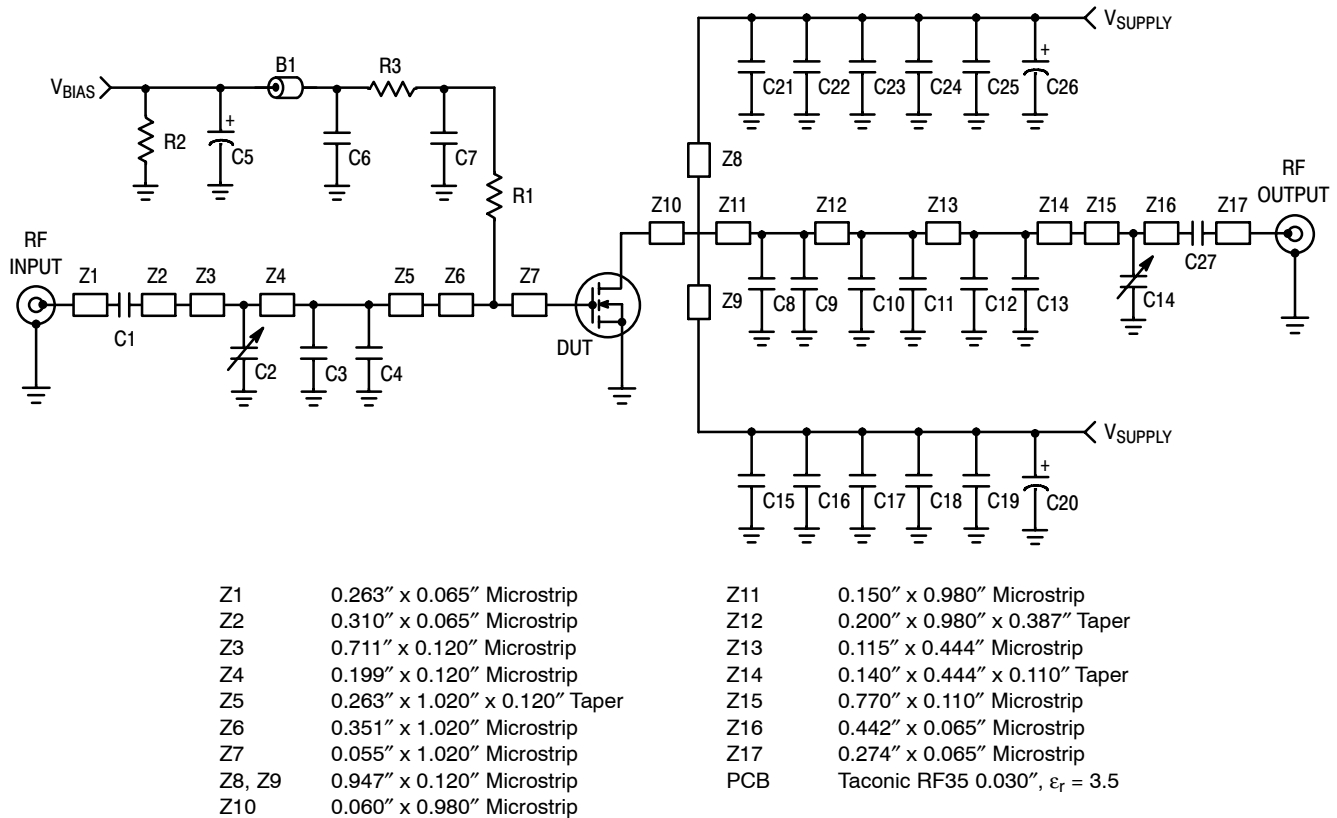


Figure 1. MRFE6S9205HR3(HSR3) Test Circuit Schematic

Table 5. MRFE6S9205HR3(HSR3) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1	Short RF Bead	2743019447	Fair-Rite
C1, C7, C15, C16, C21, C22, C27	39 pF Chip Capacitors	ATC100B390JT500XT	ATC
C2, C14	0.8-8.0 pF Variable Capacitors, Gigatrim	27291SL	Johanson
C3, C4	5.1 pF Chip Capacitors	ATC100B5R1JT500XT	ATC
C5	33 μ F, 25 V Electrolytic Capacitor	EMVY350ADA330MF55G	Nippon Chemi-Con
C6, C17, C18, C19, C23, C24, C25	10 μ F, 50 V Chip Capacitors	GRM55DR61H106KA88B	Murata
C8, C9, C10, C11, C12, C13	6.8 pF Chip Capacitors	ATC100B6R8JT500XT	ATC
C20, C26	470 μ F, 63 V Electrolytic Capacitors	EKME630ELL471MK255	United Chemi-Con
R1, R3	3.3 Ω , 1/3 W Chip Resistors	CRCW12103R30FKEA	Vishay
R2	2.2 k Ω , 1/4 W Chip Resistor	CRCW12062K20FKEA	Vishay

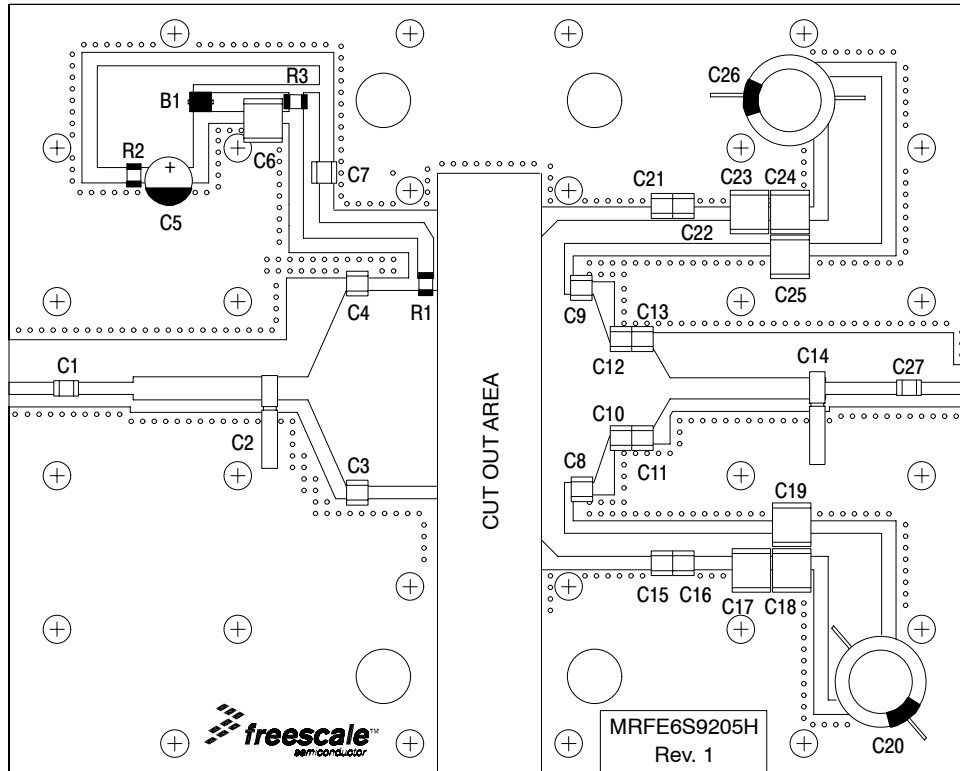


Figure 2. MRFE6S9205HR3(HSR3) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

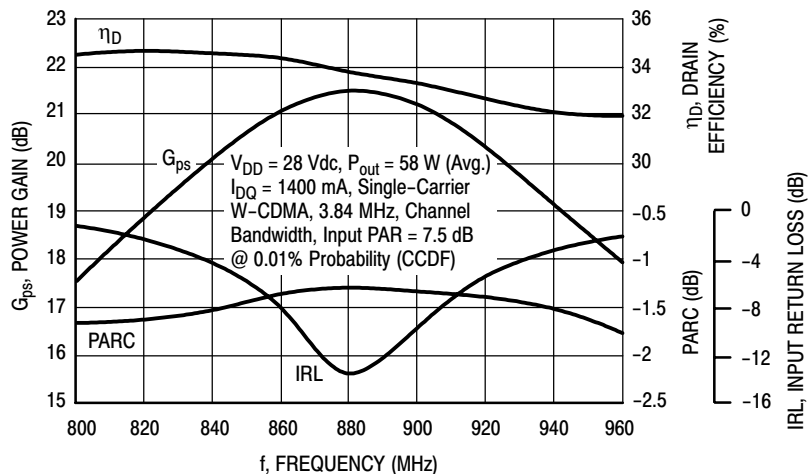


Figure 3. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 58$ Watts Avg.

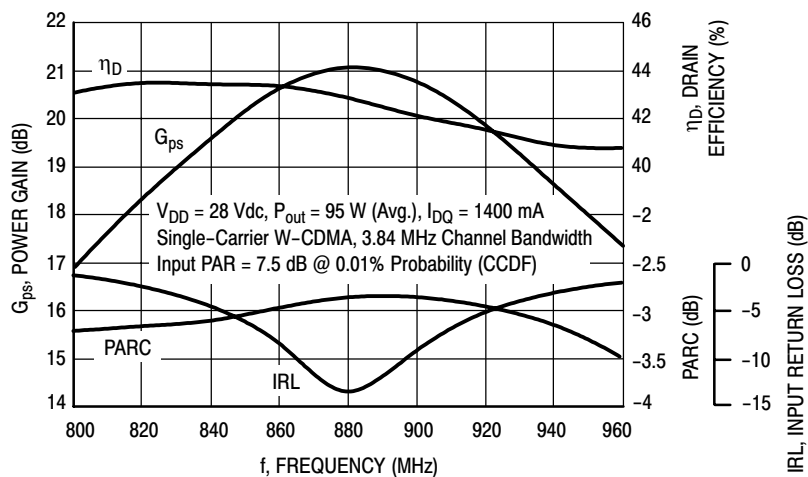


Figure 4. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 95$ Watts Avg.

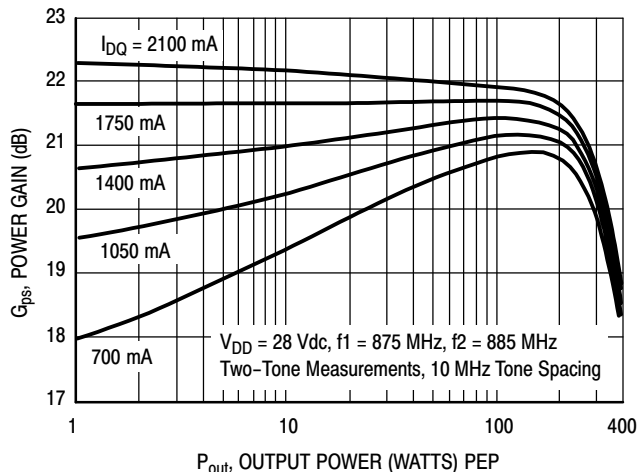


Figure 5. Two-Tone Power Gain versus Output Power

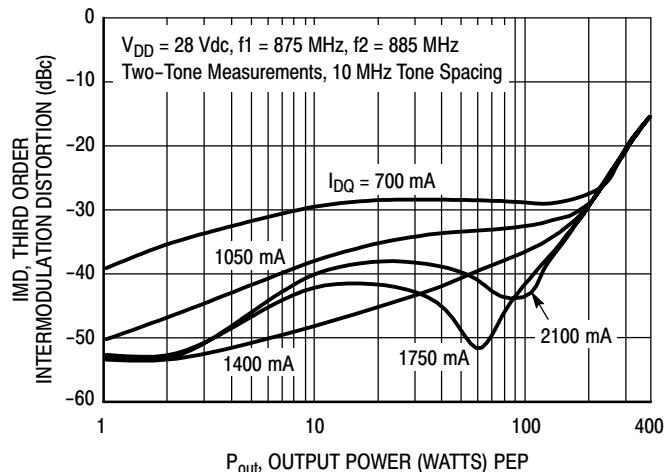


Figure 6. Third Order Intermodulation Distortion versus Output Power

TYPICAL CHARACTERISTICS

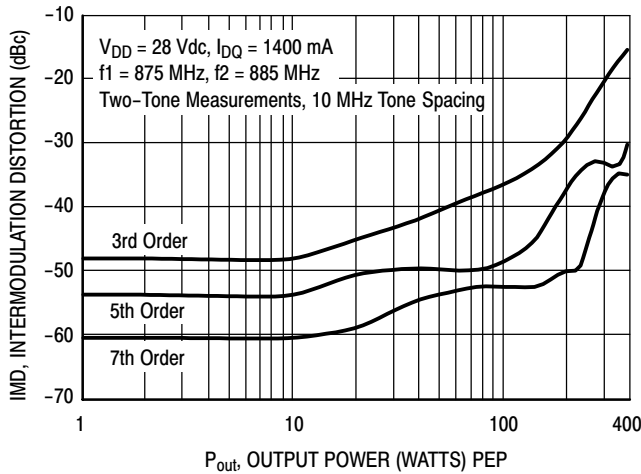


Figure 7. Intermodulation Distortion Products versus Output Power

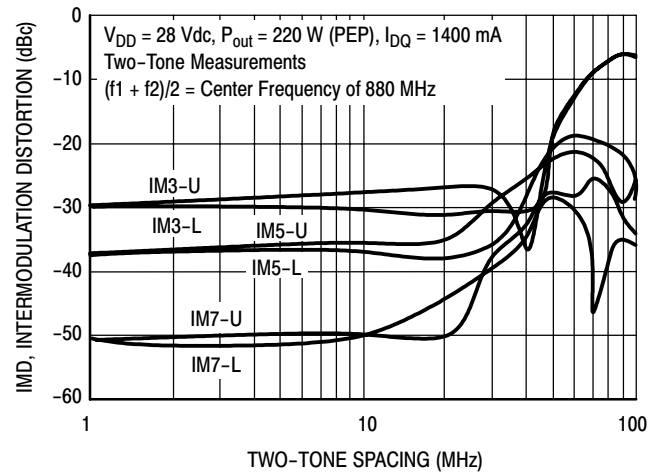


Figure 8. Intermodulation Distortion Products versus Output Power

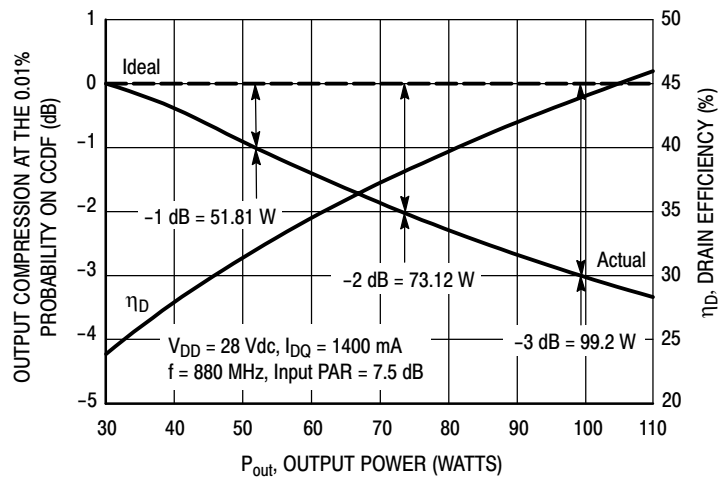


Figure 9. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

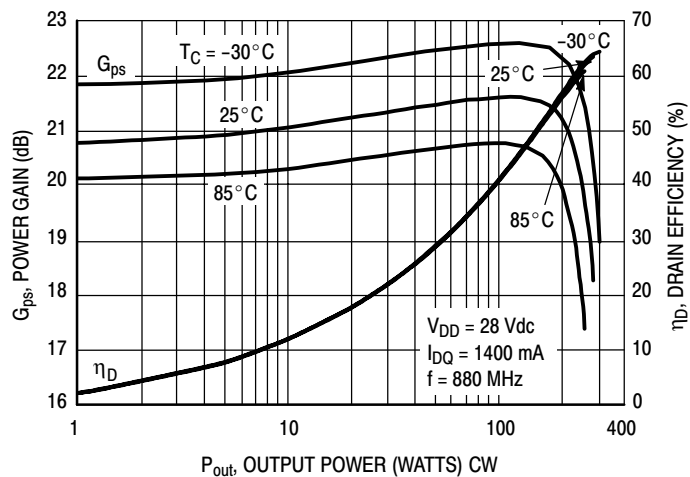


Figure 10. Power Gain and Drain Efficiency versus CW Output Power

MRFE6S9205HR3 MRFE6S9205HSR3

TYPICAL CHARACTERISTICS

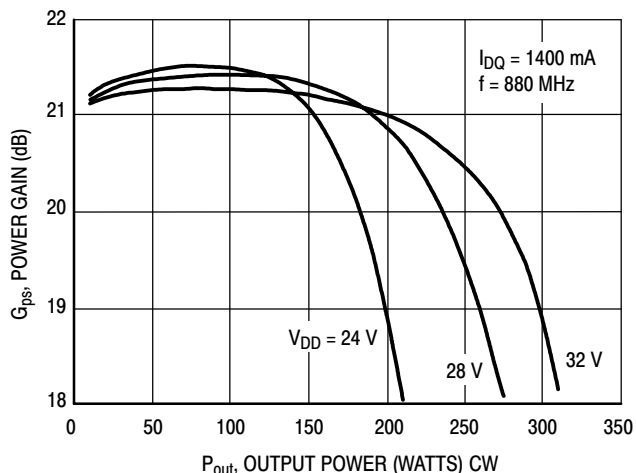
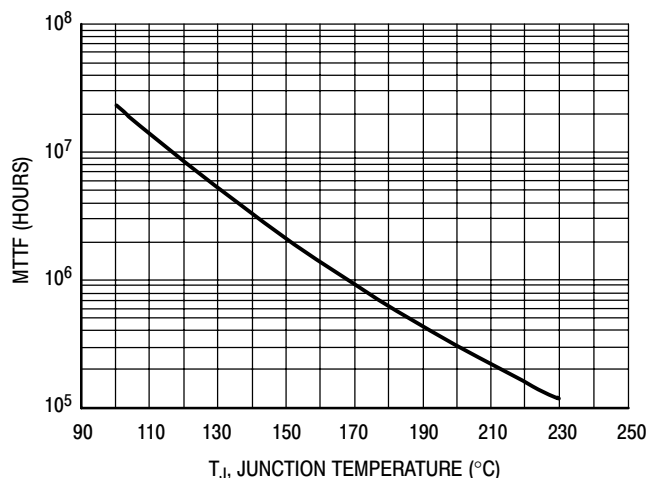


Figure 11. Power Gain versus Output Power



This above graph displays calculated MTTF in hours when the device is operated at $V_{DD} = 28$ Vdc, $P_{out} = 58$ W Avg., and $\eta_D = 34\%$.

MTTF calculator available at <http://www.freescale.com/rf>. Select Tools (Software & Tools)/Calculators to access MTTF calculators by product.

Figure 12. MTTF versus Junction Temperature

W-CDMA TEST SIGNAL

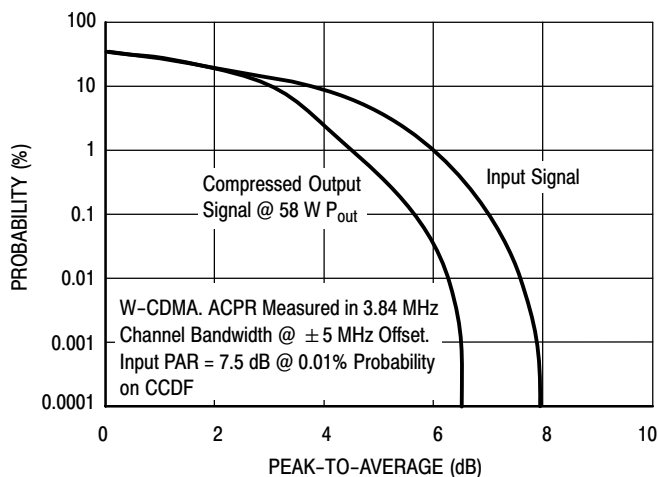


Figure 13. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 50% Clipping, Single-Carrier Test Signal

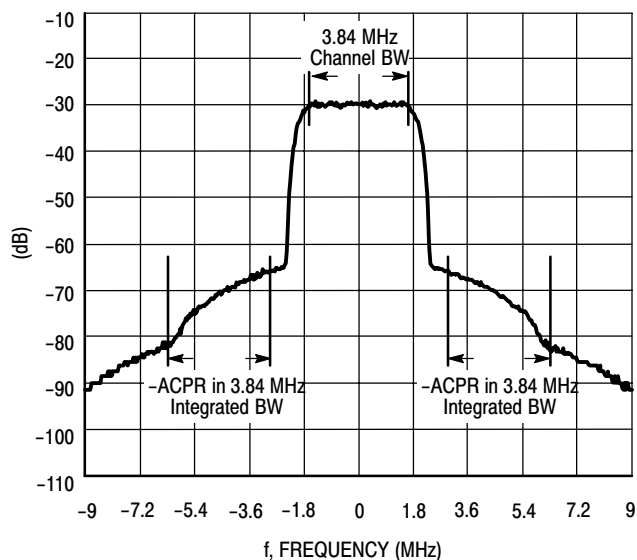
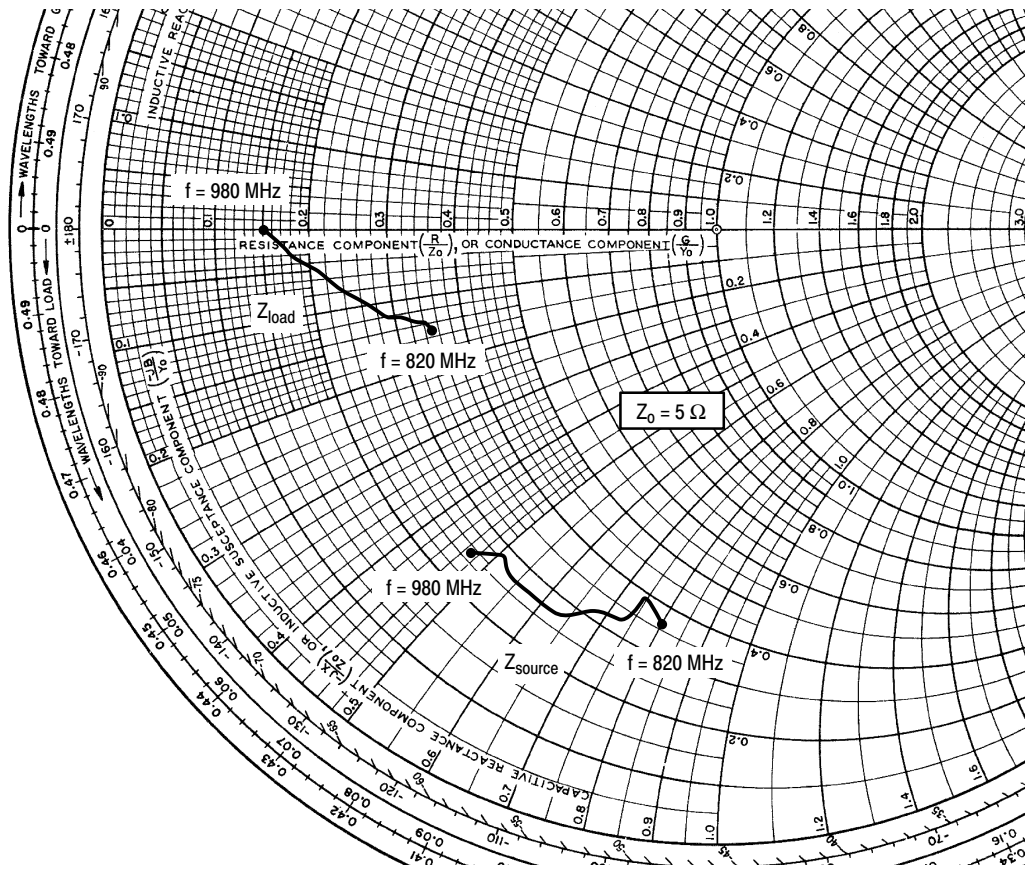


Figure 14. Single-Carrier W-CDMA Spectrum



$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 1400 \text{ mA}$, $P_{out} = 58 \text{ W Avg.}$

f MHz	Z_{source} Ω	Z_{load} Ω
820	$1.80 - j4.00$	$1.75 - j0.73$
840	$1.88 - j3.76$	$1.68 - j0.69$
860	$1.64 - j3.65$	$1.57 - j0.64$
880	$1.54 - j3.41$	$1.44 - j0.58$
900	$1.35 - j3.13$	$1.33 - j0.51$
920	$1.37 - j2.89$	$1.21 - j0.40$
940	$1.37 - j2.66$	$1.07 - j0.27$
960	$1.39 - j2.53$	$0.92 - j0.13$
980	$1.25 - j2.33$	$0.74 + j0.01$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

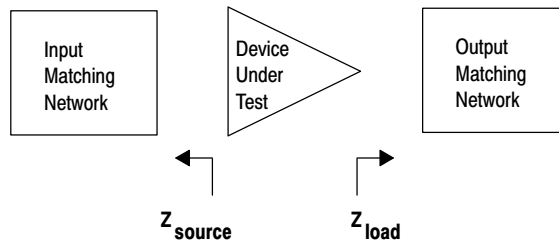
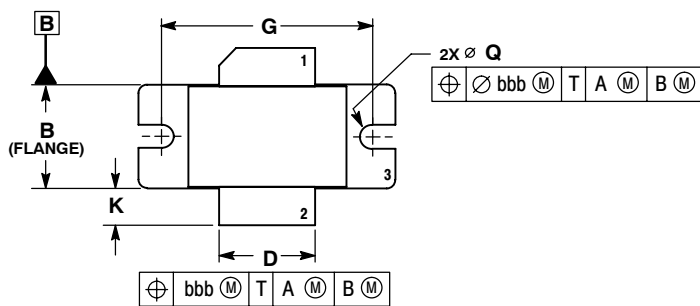


Figure 15. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS

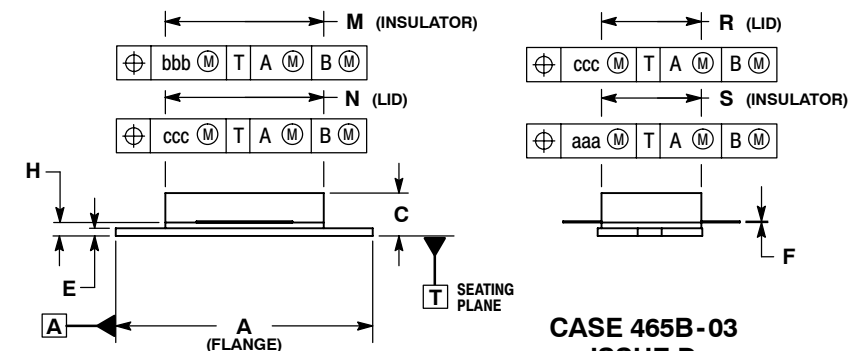


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
 4. DELETED

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.535	0.545	13.6	13.8
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
Q	Ø .118	Ø .138	Ø 3.00	Ø 3.51
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

- STYLE 1:
 PIN 1. DRAIN
 2. GATE
 3. SOURCE

**CASE 465B-03
 ISSUE D
 NI-880
 MRFE6S9205HR3**

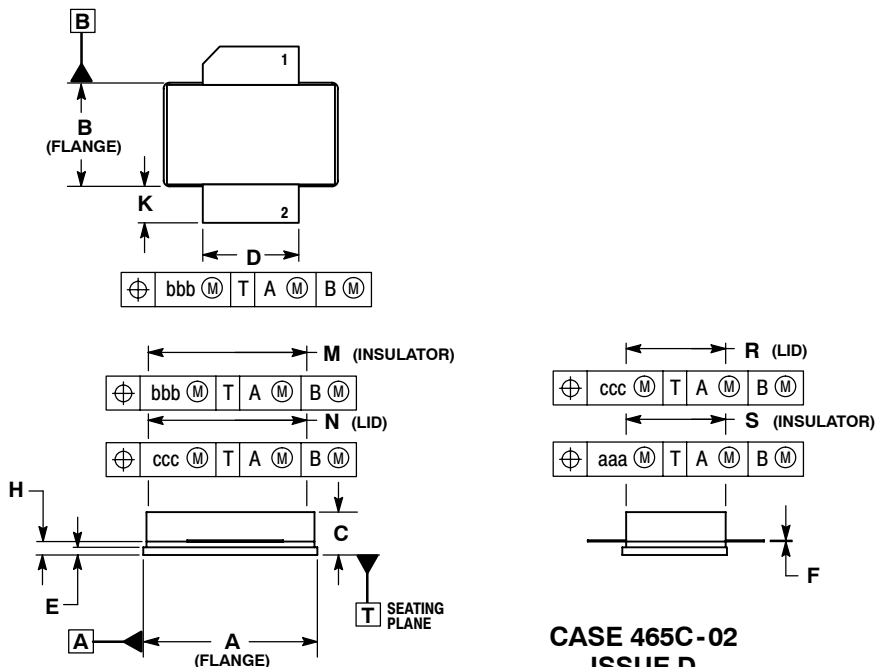


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DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.905	0.915	22.99	23.24
B	0.535	0.545	13.60	13.80
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

- STYLE 1:
 PIN 1. DRAIN
 2. GATE
 3. SOURCE

**CASE 465C-02
 ISSUE D
 NI-880S
 MRFE6S9205HSR3**



PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Oct. 2007	<ul style="list-style-type: none">• Initial Release of Data Sheet

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