



# RF Power Field Effect Transistor

## N-Channel Enhancement-Mode Lateral MOSFET

Designed for broadband commercial and industrial applications with frequencies up to 1000 MHz. The high gain and broadband performance of this device make it ideal for large-signal, common-source amplifier applications in 26 volt base station equipment.

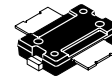
- Typical Performance at 945 MHz, 26 Volts  
Output Power — 30 Watts PEP  
Power Gain — 20 dB  
Efficiency — 41% (Two Tones)  
IMD — -31 dBc
- Integrated ESD Protection
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 945 MHz, 30 Watts CW Output Power

### Features

- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Dual-Lead Bolt-down Plastic Package Can Also Be Used As Surface Mount.
- 200°C Capable Plastic Package
- N Suffix Indicates Lead-Free Terminations. RoHS Compliant.
- TO-270-2 in Tape and Reel. R1 Suffix = 500 Units per 24 mm, 13 inch Reel.

**MRF9030NR1**

**945 MHz, 30 W, 26 V  
LATERAL N-CHANNEL  
BROADBAND  
RF POWER MOSFET**



**CASE 1265-09, STYLE 1  
TO-270-2  
PLASTIC**

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	- 0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	- 0.5, + 15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	$P_D$	139 0.93	W W/°C
Storage Temperature Range	$T_{stg}$	- 65 to +150	°C
Operating Junction Temperature	$T_J$	200	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (1)	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.08	°C/W

**Table 3. ESD Protection Characteristics**

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum)
Charge Device Model	C7 (Minimum)

**Table 4. Moisture Sensitivity Level**

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

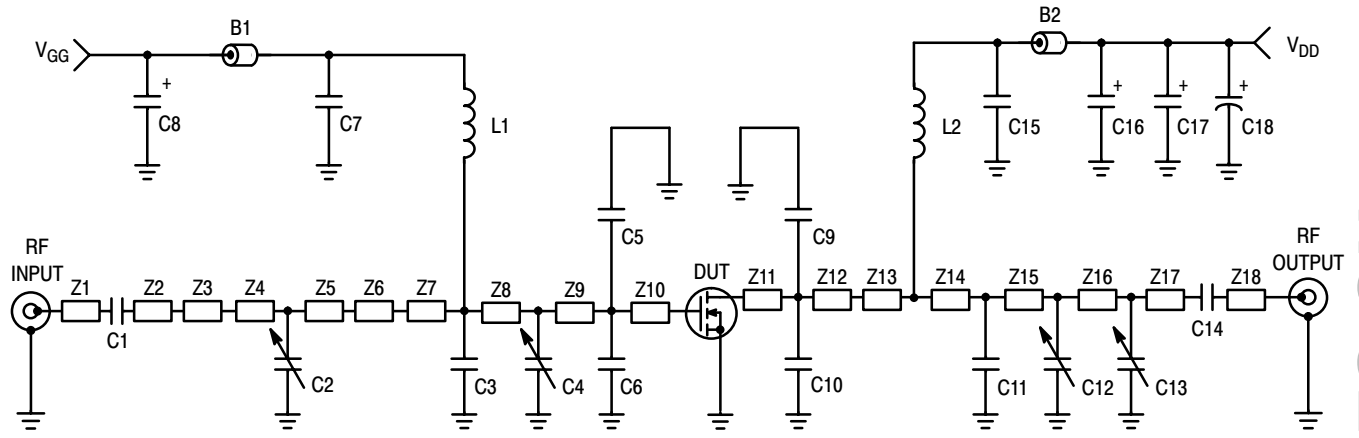
1. MTTF calculator available at <http://www.freescale.com/rtf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

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**Table 5. Electrical Characteristics** ( $T_c = 25^\circ\text{C}$  Unless Otherwise Noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Off Characteristics</b>					
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 26\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$
<b>On Characteristics</b>					
Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 100\ \mu\text{Adc}$ )	$V_{GS(th)}$	2	2.9	4	Vdc
Gate Quiescent Voltage ( $V_{DS} = 26\text{ Vdc}$ , $I_D = 250\ \text{mAdc}$ )	$V_{GS(Q)}$	3	3.8	5	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 0.7\ \text{Adc}$ )	$V_{DS(on)}$	—	0.23	0.4	Vdc
Forward Transconductance ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 2\ \text{Adc}$ )	$g_{fs}$	—	2.7	—	S
<b>Dynamic Characteristics</b>					
Input Capacitance ( $V_{DS} = 26\text{ Vdc} \pm 30\ \text{mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{iss}$	—	49	—	pF
Output Capacitance ( $V_{DS} = 26\text{ Vdc} \pm 30\ \text{mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{oss}$	—	27	—	pF
Reverse Transfer Capacitance ( $V_{DS} = 26\text{ Vdc} \pm 30\ \text{mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{rss}$	—	1.2	—	pF
<b>Functional Tests</b> (In Freescale Test Fixture)					
Two-Tone Common-Source Amplifier Power Gain ( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 30\ \text{W PEP}$ , $I_{DQ} = 250\ \text{mA}$ , $f_1 = 945.0\ \text{MHz}$ , $f_2 = 945.1\ \text{MHz}$ )	$G_{ps}$	18	20	—	dB
Two-Tone Drain Efficiency ( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 30\ \text{W PEP}$ , $I_{DQ} = 250\ \text{mA}$ , $f_1 = 945.0\ \text{MHz}$ , $f_2 = 945.1\ \text{MHz}$ )	$\eta$	37	41	—	%
3rd Order Intermodulation Distortion ( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 30\ \text{W PEP}$ , $I_{DQ} = 250\ \text{mA}$ , $f_1 = 945.0\ \text{MHz}$ , $f_2 = 945.1\ \text{MHz}$ )	IMD	—	-31	-28	dBc
Input Return Loss ( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 30\ \text{W PEP}$ , $I_{DQ} = 250\ \text{mA}$ , $f_1 = 945.0\ \text{MHz}$ , $f_2 = 945.1\ \text{MHz}$ )	IRL	—	-13	-9	dB
Two-Tone Common-Source Amplifier Power Gain ( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 30\ \text{W PEP}$ , $I_{DQ} = 250\ \text{mA}$ , $f_1 = 930.0\ \text{MHz}$ , $f_2 = 930.1\ \text{MHz}$ and $f_1 = 960.0\ \text{MHz}$ , $f_2 = 960.1\ \text{MHz}$ )	$G_{ps}$	—	20	—	dB
Two-Tone Drain Efficiency ( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 30\ \text{W PEP}$ , $I_{DQ} = 250\ \text{mA}$ , $f_1 = 930.0\ \text{MHz}$ , $f_2 = 930.1\ \text{MHz}$ and $f_1 = 960.0\ \text{MHz}$ , $f_2 = 960.1\ \text{MHz}$ )	$\eta$	—	40.5	—	%
3rd Order Intermodulation Distortion ( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 30\ \text{W PEP}$ , $I_{DQ} = 250\ \text{mA}$ , $f_1 = 930.0\ \text{MHz}$ , $f_2 = 930.1\ \text{MHz}$ and $f_1 = 960.0\ \text{MHz}$ , $f_2 = 960.1\ \text{MHz}$ )	IMD	—	-31	—	dBc
Input Return Loss ( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 30\ \text{W PEP}$ , $I_{DQ} = 250\ \text{mA}$ , $f_1 = 930.0\ \text{MHz}$ , $f_2 = 930.1\ \text{MHz}$ and $f_1 = 960.0\ \text{MHz}$ , $f_2 = 960.1\ \text{MHz}$ )	IRL	—	-12	—	dB

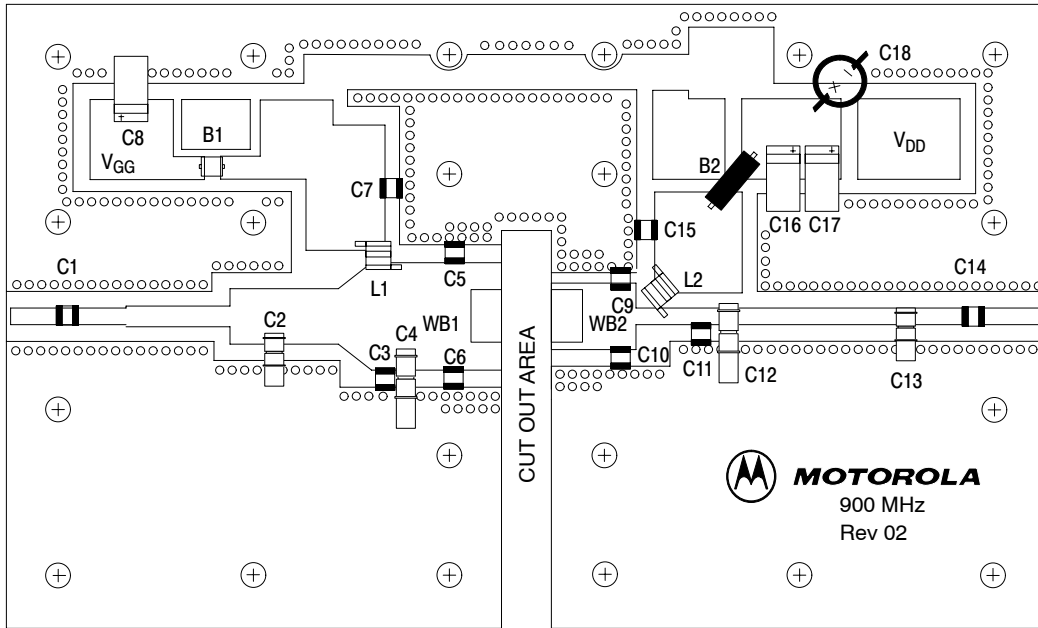


Z1	0.260" x 0.060" Microstrip	Z11	0.360" x 0.270" Microstrip
Z2	0.240" x 0.060" Microstrip	Z12	0.050" x 0.270" Microstrip
Z3	0.500" x 0.100" Microstrip	Z13	0.110" x 0.060" Microstrip
Z4	0.200" x 0.270" Microstrip	Z14	0.220" x 0.060" Microstrip
Z5	0.330" x 0.270" Microstrip	Z15	0.100" x 0.060" Microstrip
Z6	0.140" x 0.270" x 0.520", Taper	Z16	0.870" x 0.060" Microstrip
Z7	0.040" x 0.520" Microstrip	Z17	0.240" x 0.060" Microstrip
Z8	0.090" x 0.520" Microstrip	Z18	0.340" x 0.060" Microstrip
Z9	0.370" x 0.520" Microstrip (MRF9030NR1)	Board	Taconic RF - 35-0300, $\epsilon_r = 3.5$
Z10	0.290" x 0.520" Microstrip (MRF9030NBR1)		
	0.130" x 0.520" Microstrip (MRF9030NR1)		
	0.210" x 0.520" Microstrip (MRF9030NBR1)		

**Figure 1. 930-960 MHz Broadband Test Circuit Schematic**

**Table 6. 930 - 960 MHz Broadband Test Circuit Component Designations and Values**

Part	Description	Part Number	Manufacturer
B1	Short Ferrite Bead, Surface Mount	2743019447	Fair-Rite
B2	Long Ferrite Bead, Surface Mount	2743029446	Fair-Rite
C1, C7, C14, C15	47 pF Chip Capacitors	ATC100B470JT500XT	ATC
C2	0.6-4.5 Variable Capacitor, Gigatrim	27271SL	Johanson
C3, C11	3.9 pF Chip Capacitors	ATC100B3R6BT500XT	ATC
C4, C12	0.8-8.0 Variable Capacitors, Gigatrim	27291SL	Johanson
C5, C6	6.8 pF Chip Capacitors	ATC100B7R5JT500XT	ATC
C8, C16, C17	10 $\mu$ F, 35 V Tantalum Chip Capacitors	T491D106K035AT	Kemet
C9, C10	10 pF Chip Capacitors	ATC100B100JT500XT	ATC
C13	1.8 pF Chip Capacitor (MRF9030NR1) 0.6-4.5 Variable Capacitor, Gigatrim (MRF9030NBR1)	ATC100B1R8BT500XT 27271SL	ATC Johanson
C18	220 $\mu$ F Electrolytic Chip Capacitor	MCAX63V227M13X22	Multicomp
L1, L2	12.5 nH Coilcraft Inductors	A04T-5	Coilcraft



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**Figure 2. 930-960 MHz Broadband Test Circuit Component Layout**

TYPICAL CHARACTERISTICS

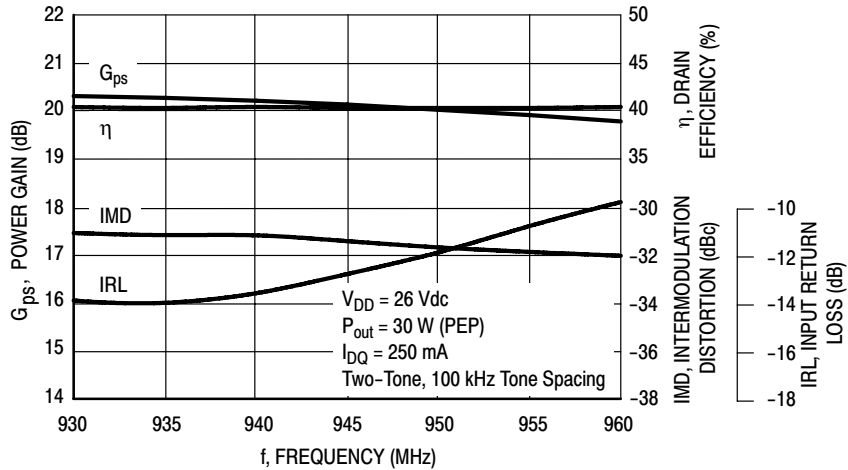


Figure 3. Class AB Broadband Circuit Performance

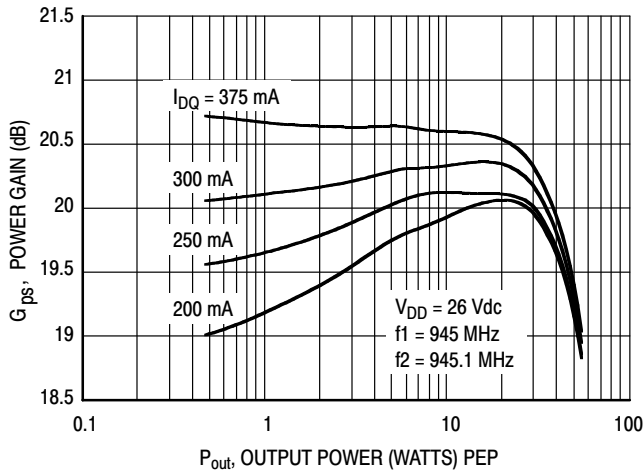


Figure 4. Power Gain versus Output Power

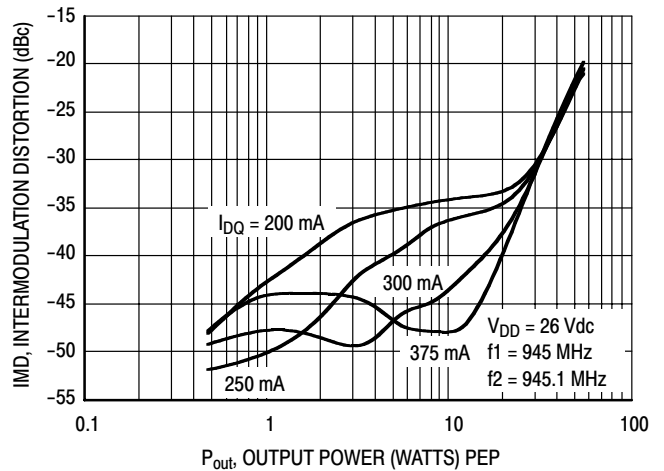


Figure 5. Intermodulation Distortion versus Output Power

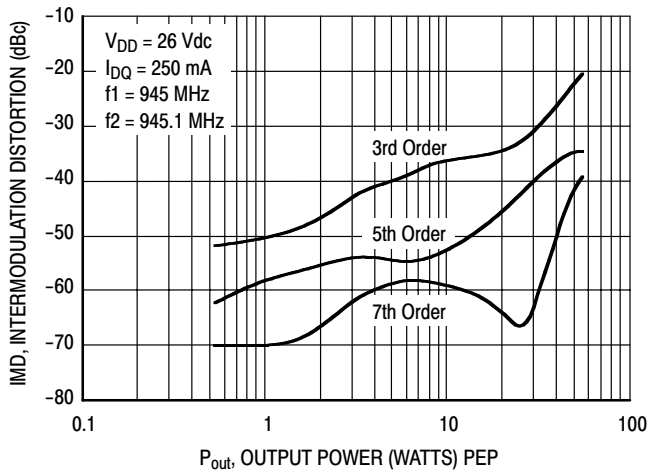


Figure 6. Intermodulation Distortion Products versus Output Power

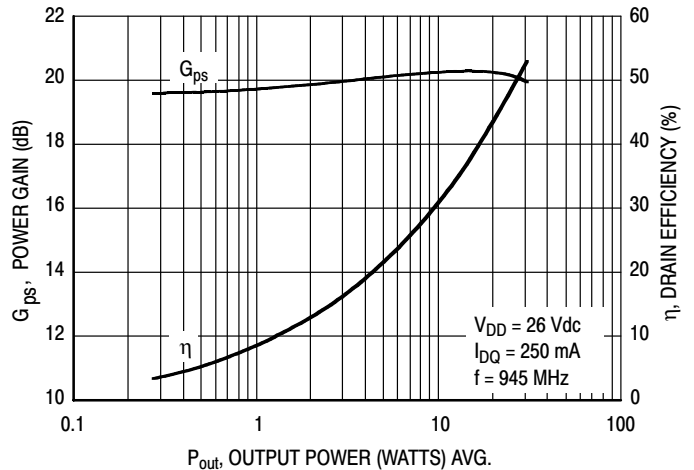
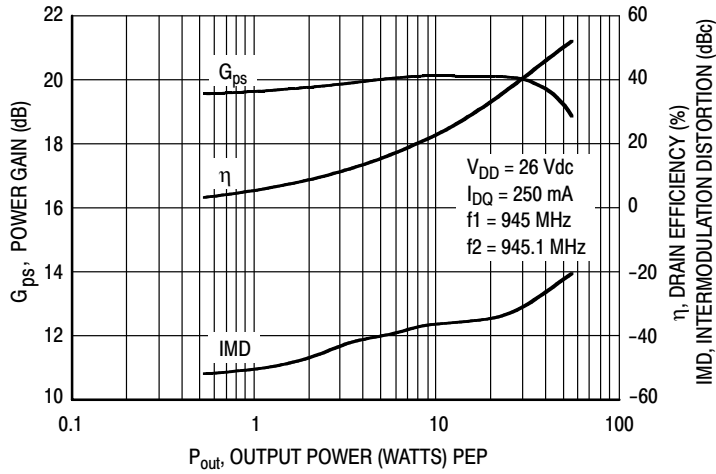
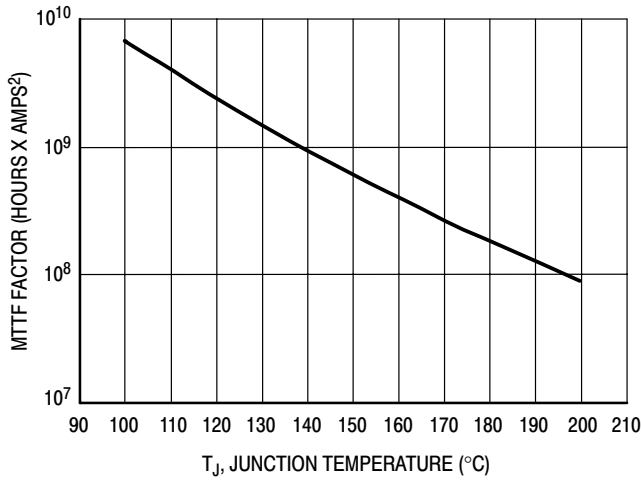


Figure 7. Power Gain and Efficiency versus Output Power

**TYPICAL CHARACTERISTICS**

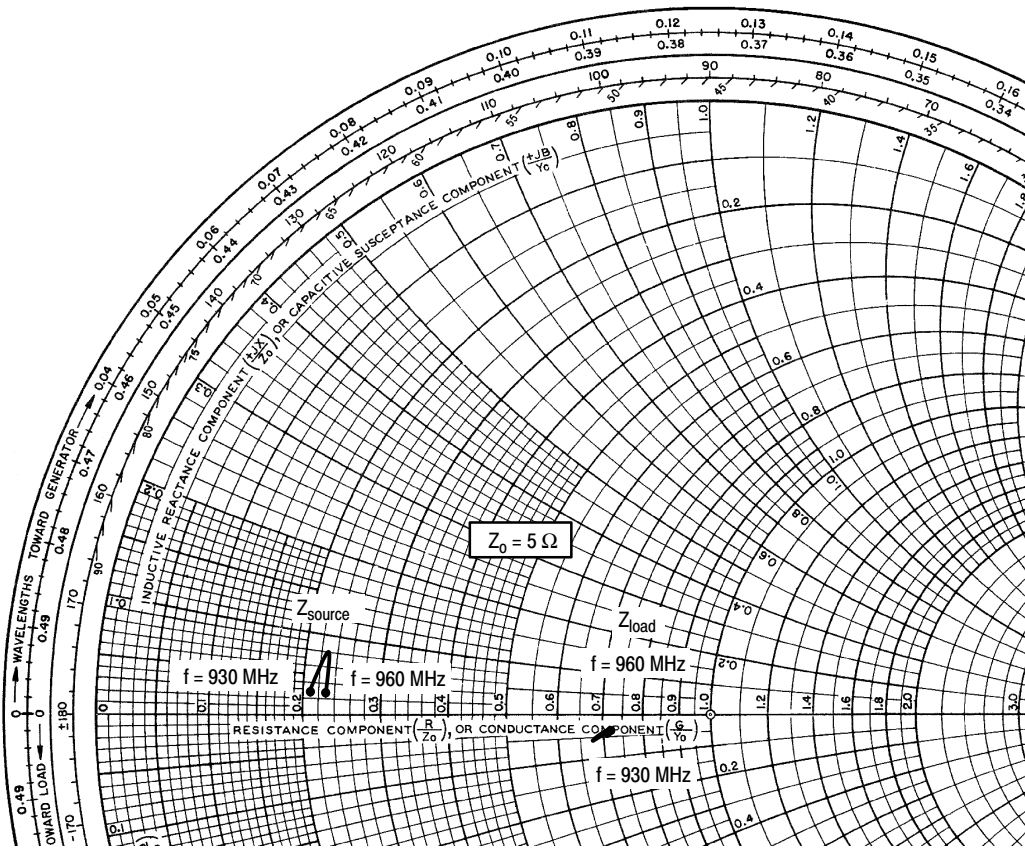


**Figure 8. Power Gain, Efficiency and IMD versus Output Power**



This above graph displays calculated MTTF in hours x ampere<sup>2</sup> drain current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTTF factor by  $I_D^2$  for MTTF in a particular application.

**Figure 9. MTTF Factor versus Junction Temperature**



$V_{DD} = 26\text{ V}$ ,  $I_{DQ} = 250\text{ mA}$ ,  $P_{out} = 30\text{ Watts (PEP)}$

f MHz	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
930	$1.07 + j0.160$	$3.53 - j0.20$
945	$1.14 + j0.385$	$3.41 - j0.24$
960	$1.17 + j0.170$	$3.60 - j0.17$

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

Note:  $Z_{load}$  was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

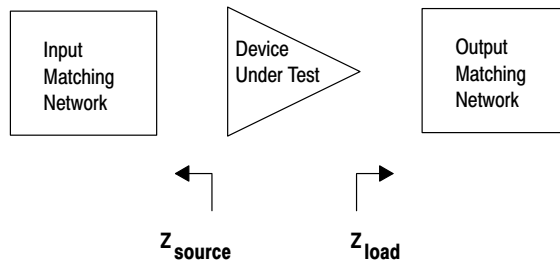
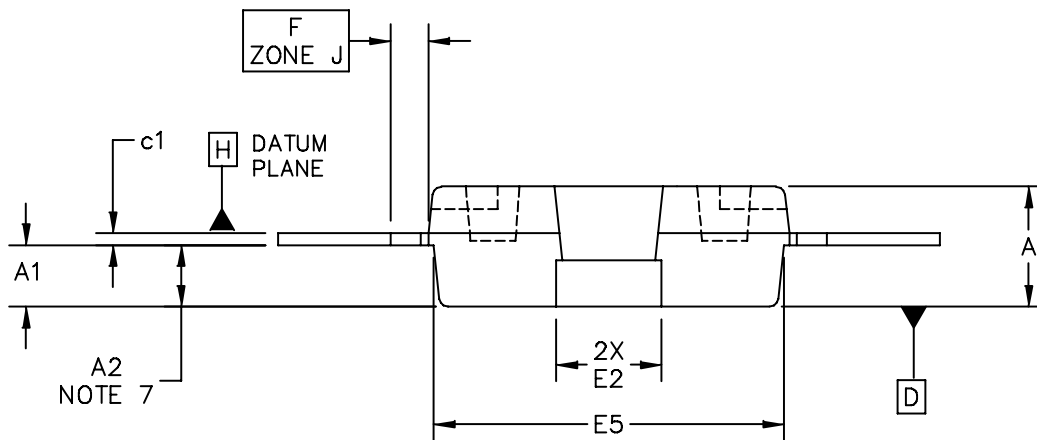
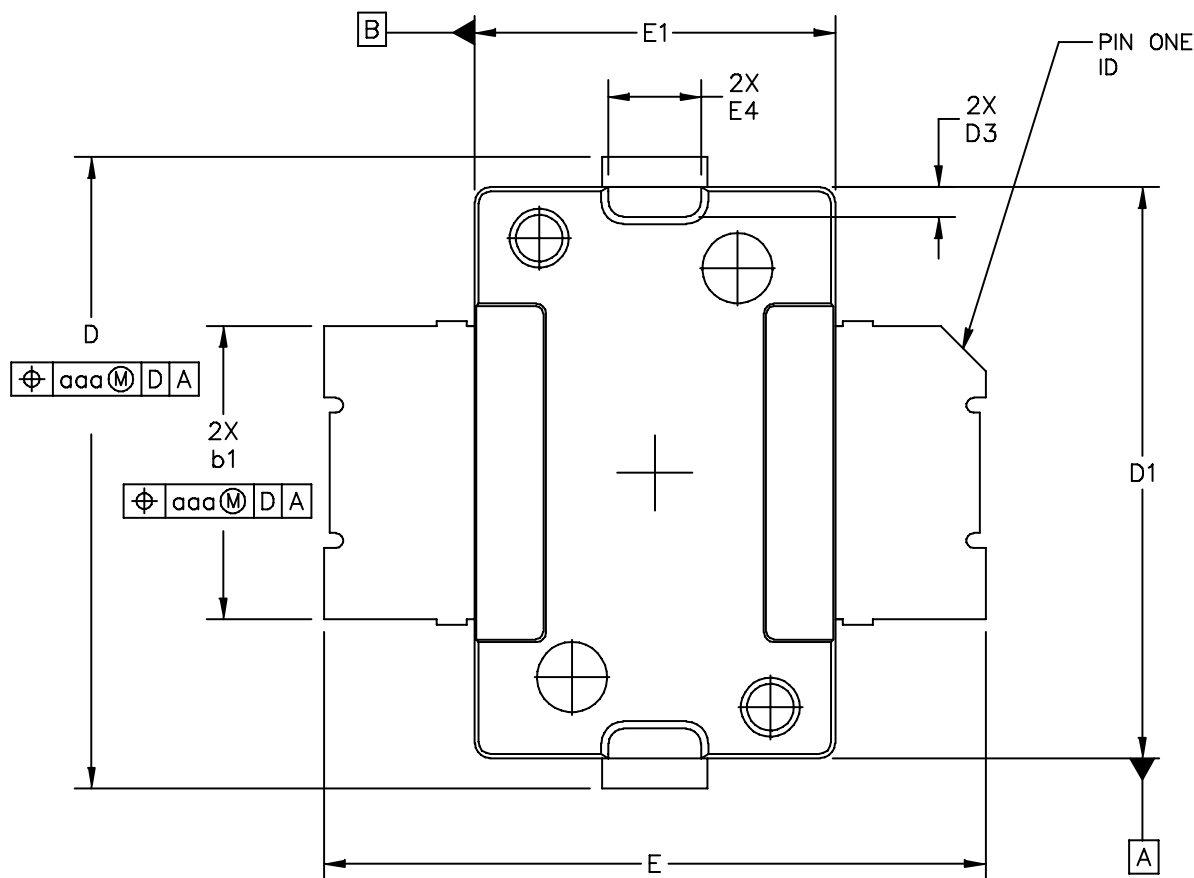


Figure 10. Series Equivalent Source and Load Impedance

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PACKAGE DIMENSIONS

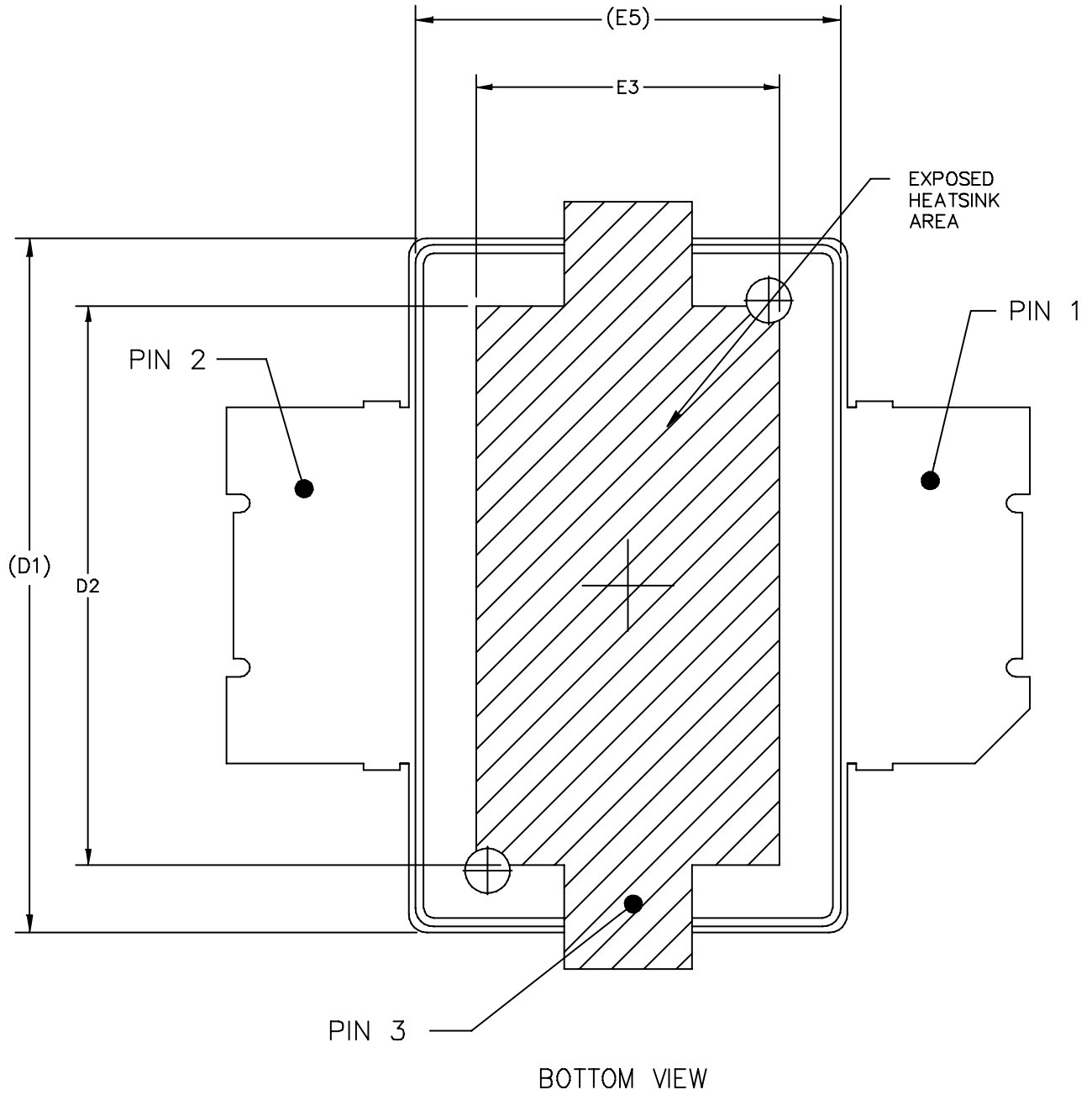


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		CASE NUMBER: 1265-09		29 JUN 2007	
		STANDARD: JEDEC TO-270 AA			



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MRF9030NR1

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D1" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION "A2" APPLIES WITHIN ZONE "J" ONLY.
8. DIMENSIONS "D" AND "E2" DO NOT INCLUDE MOLD PROTRUSION. OVERALL LENGTH INCLUDING MOLD PROTRUSION SHOULD NOT EXCEED 0.430 INCH FOR DIMENSION "D" AND 0.080 INCH FOR DIMENSION "E2". DIMENSIONS "D" AND "E2" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -D-.

STYLE 1:  
 PIN 1 - DRAIN  
 PIN 2 - GATE  
 PIN 3 - SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.078	.082	1.98	2.08	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b1	.193	.199	4.90	5.06
A2	.040	.042	1.02	1.07	c1	.007	.011	0.18	0.28
D	.416	.424	10.57	10.77	aaa	.004		0.10	
D1	.378	.382	9.60	9.70					
D2	.290	----	7.37	----					
D3	.016	.024	0.41	0.61					
E	.436	.444	11.07	11.28					
E1	.238	.242	6.04	6.15					
E2	.066	.074	1.68	1.88					
E3	.150	----	3.81	----					
E4	.058	.066	1.47	1.68					
E5	.231	.235	5.87	5.97					

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			STANDARD: JEDEC TO-270 AA		

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## PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

### Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
12	Sept. 2008	<ul style="list-style-type: none"><li>• Data sheet revised to reflect part status change, p. 1, including use of applicable overlay.</li><li>• Replaced Case Outline 1265-08 with 1265-09, Issue K, p. 1, 8-10. Corrected cross hatch pattern in bottom view and changed its dimensions (D2 and E3) to minimum value on source contact (D2 changed from Min - Max .290 - .320 to .290 Min; E3 changed from Min - Max .150 - .180 to .150 Min). Added JEDEC Standard Package Number.</li><li>• Updated Part Numbers in Table 6, Component Designations and Values, to RoHS compliant part numbers, p. 3</li><li>• Removed Fig. 3, Test Circuit Component Layout (MRF9030NBR1) and Fig. 12, Series Equivalent Source and Load Impedance (MRF9030NBR1), renumbered Figures accordingly, p. 4-7</li><li>• Added Product Documentation and Revision History, p. 11</li></ul>

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