

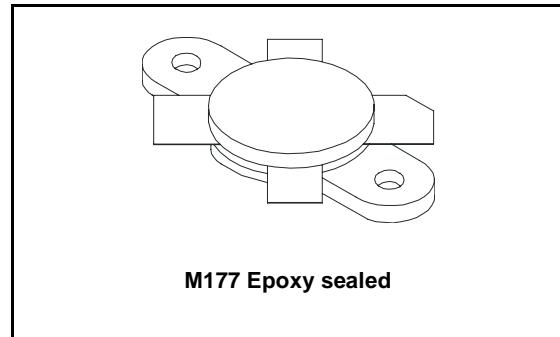


SD2943

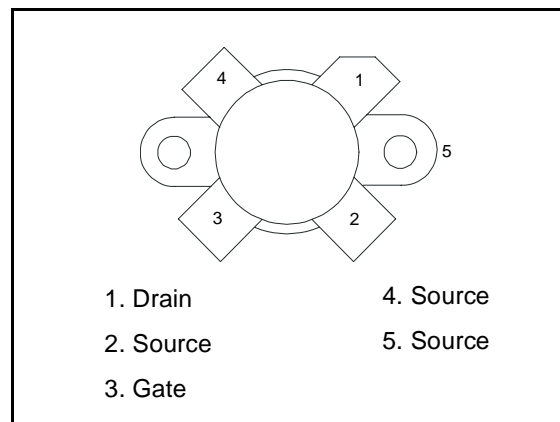
RF Power Transistor HF/VHF/UHF N - Channel MOSFETs

General Features

- HIGH POWER CAPABILITY
- POUT = 350W MIN. WITH 22dB GAIN @ 30 MHz
- PSAT = 450 W
- LOW $R_{DS(on)}$
- THERMALLY ENHANCED PACKAGING FOR LOWER JUNCTION TEMPERATURES
- GOLD METALLIZATION
- EXCELLENT THERMAL STABILITY
- COMMON SOURCE CONFIGURATION



Pin Connection



Description

The SD2943 is a gold metallized N-Channel MOS field-effect RF power transistor. It is intended for use in 50 V dc large signal applications up to 150 MHz. SD2943 offers a 20% higher power saturation than SD2933, it is ideal for ISM applications where reliability and ruggedness are critical factors.

Order Codes

Part Number	Marking	Package	Packaging
SD2943	SD2943	M177	Plastic Tray

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1 Electrical Data

1.1 Maximum Rating

Table 1. Absolute Maximum Rating ($T_{CASE} = 25^{\circ}C$)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}^{(1)}$	Drain Source Voltage	130	V
$V_{DGR}^{(2)}$	Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	130	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current	40	A
P_{DISS}	Power Dissipation	648	W
T_j	Max. Operating Junction Temperature	200	$^{\circ}C$
E_{AS}	Avalanche Energy, Single Pulse ($I_D = 60A$)	1500	mJ
$E_{AR}^{(2)}$	Avalanche Energy, Repetitive	50	mJ
T_{STG}	Storage Temperature	-65 to +150	$^{\circ}C$

1. $T_j = 150^{\circ}C$

2. Repetitive rating: Pulse width limited by maximum junction temperature; Repetitive avalanche causes additional power losses that can be calculated as: $PAV = EAR * f$

1.2 Thermal Data

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction to Case thermal resistance	0.27	$^{\circ}C/W$

1.3 Electrical Characteristics ($T_{CASE} = 25^{\circ}C$)

Table 3. Static

Symbol	Test Conditions			Min.	Typ.	Max.	Unit
$V_{(BR)DSS}^{(1)}$	$V_{GS} = 0 V$	$I_{DS} = 200 mA$		130			V
I_{DSS}	$V_{GS} = 0 V$	$V_{DS} = 50 V$				200	μA
I_{GSS}	$V_{GS} = 20 V$	$V_{DS} = 0 V$				500	nA
$V_{GS(Q)}$	$V_{DS} = 10 V$	$I_D = 250 mA$		2		4	V
$V_{DS(ON)}$	$V_{GS} = 10 V$	$I_D = 20 A$				2	V
$G_{FS}^{(2)}$	$V_{DS} = 10 V$	$I_D = 10 A$		10			mho
C_{ISS}	$V_{GS} = 0 V$	$V_{DS} = 50 V$	$f = 1 MHz$		830		pF
C_{OSS}	$V_{GS} = 0 V$	$V_{DS} = 50 V$	$f = 1 MHz$		470		pF
C_{RSS}	$V_{GS} = 0 V$	$V_{DS} = 50 V$	$f = 1 MHz$		35		pF

1. $T_J = 150^{\circ}C$

2. G_{FS} sorts for each unit see [Table 5](#)

Table 4. Dynamic

Symbol	Test Conditions			Min.	Typ.	Max.	Unit
P_{OUT}	$V_{DD} = 50 V$	$I_{DQ} = 250 mA$	$f = 30 MHz$	350	450		W
G_{PS}	$V_{DD} = 50 V$	$I_{DQ} = 250 mA$	$P_{OUT} = 350 W$	22	25		dB
h_D	$V_{DD} = 50 V$	$I_{DQ} = 250 mA$	$P_{OUT} = 350 W$	60	65		%
Load Mismatch	$V_{DD} = 50 V$	$I_{DQ} = 250 mA$	$P_{OUT} = 350 W$	3:1			VSWR
	All Phase Angles						

Table 5. G_{FS} SORTS

Symbol	Value
A	10 ÷ 10.99
B	11 ÷ 11.99
C	12 ÷ 12.99
D	13 ÷ 13.99
E	14 ÷ 14.99
F	15 ÷ 15.99
G	16 ÷ 16.99
H	17 ÷ 18

2 Impedance

Figure 1. Impedance Data Schematic

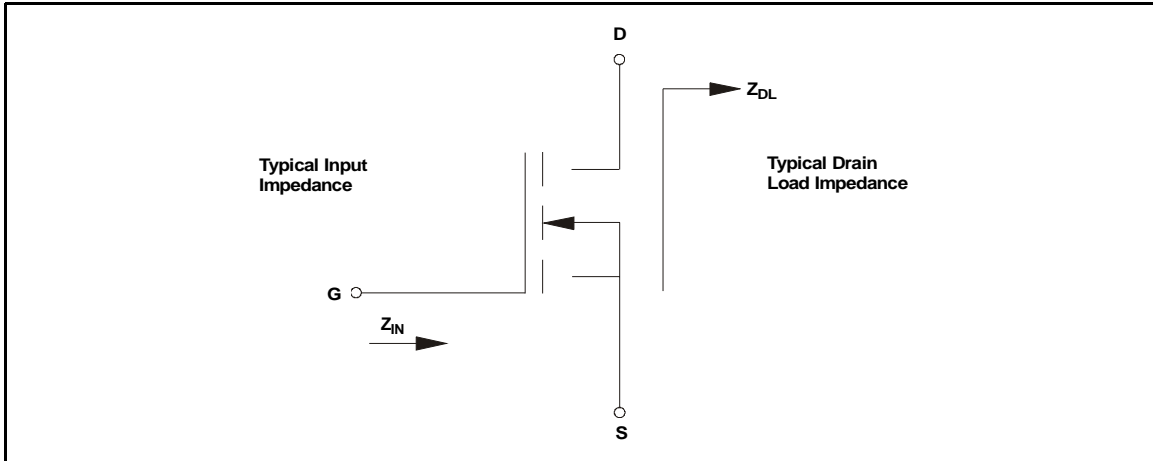


Table 6. Impedance Data

f	$Z_{IN} (\Omega)$	$Z_{DL} (\Omega)$
30 MHz	$1.3 - j 2.9$	$3.1 + j 2.3$
108 MHz	$1.4 - j 2.4$	$1.9 + j 1.4$
175 MHz	$1.4 - j 2.2$	$1.7 + j 1.6$

3 Typical Performance

Figure 2. Capacitance Vs Drain Voltage

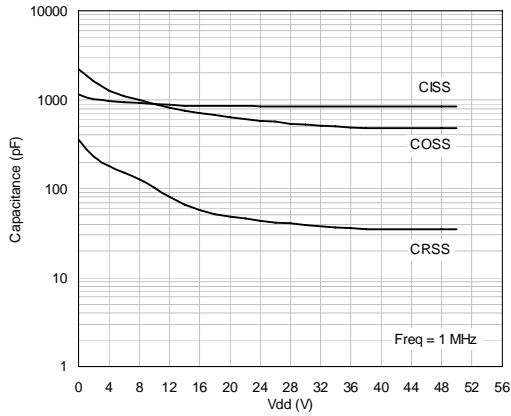


Figure 3. Drain Current Vs Gate Voltage

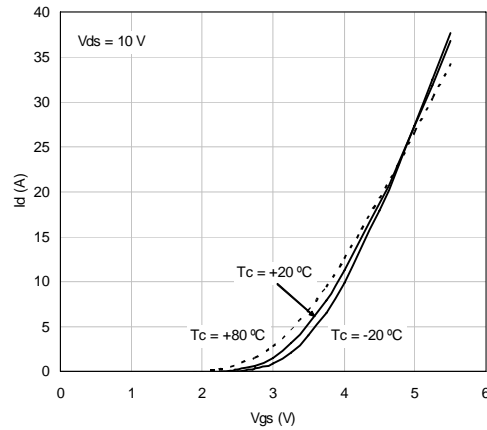


Figure 4. Gate-Source Voltage Vs Case Temp. Figure 5. Max. Therm. Resist. Vs Case Temp.

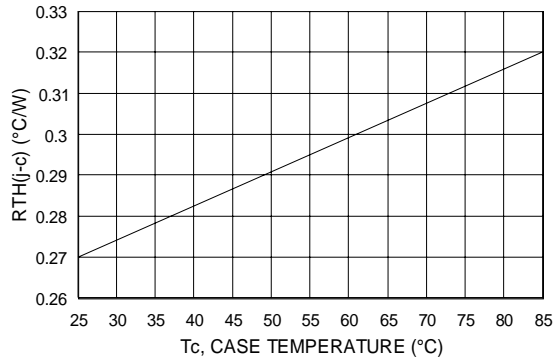
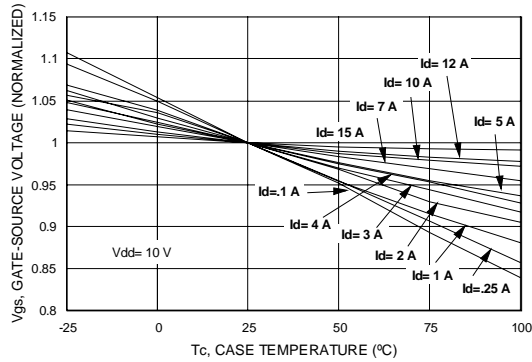


Figure 6. Pout Vs Input Power & Drain Voltage **Figure 7. Pout Vs Input Power & Case Temp.**

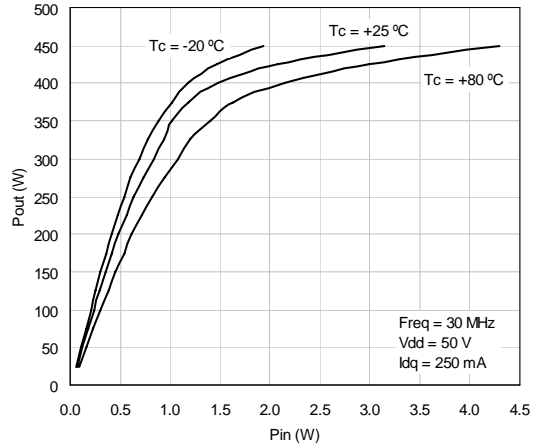
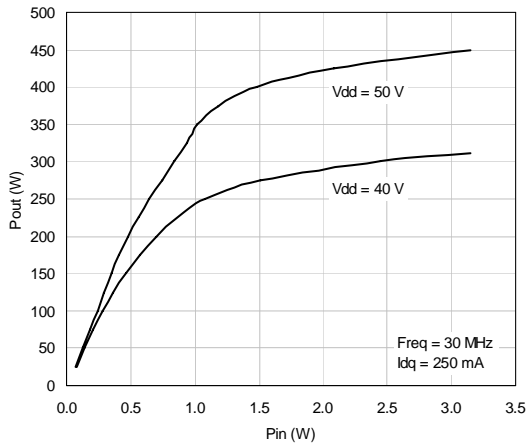


Table 7. Efficiency Vs Pout

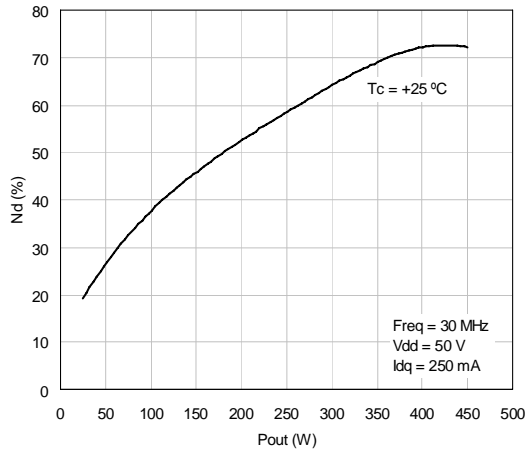


Figure 8. Power Gain Vs Pout & Case Temp.

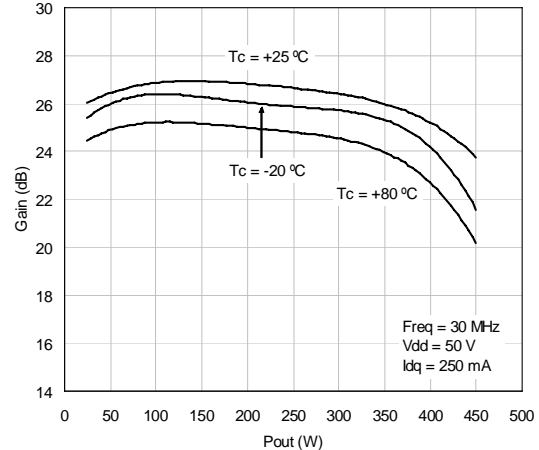


Figure 9. Pout Vs Gate Voltage

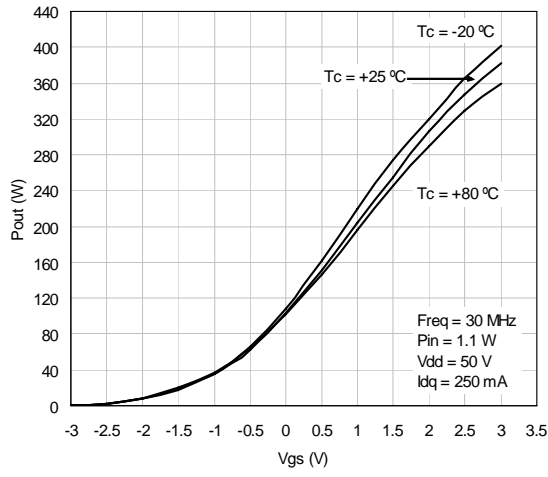
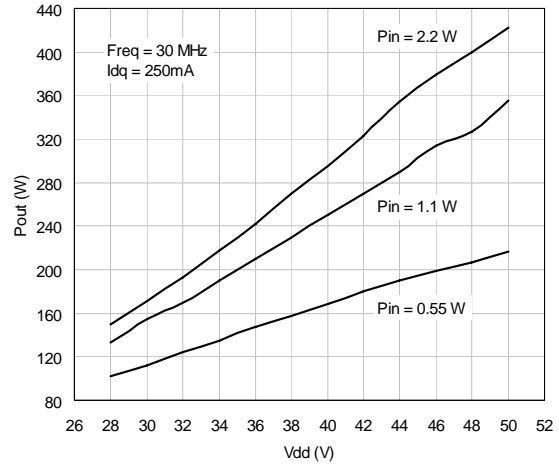
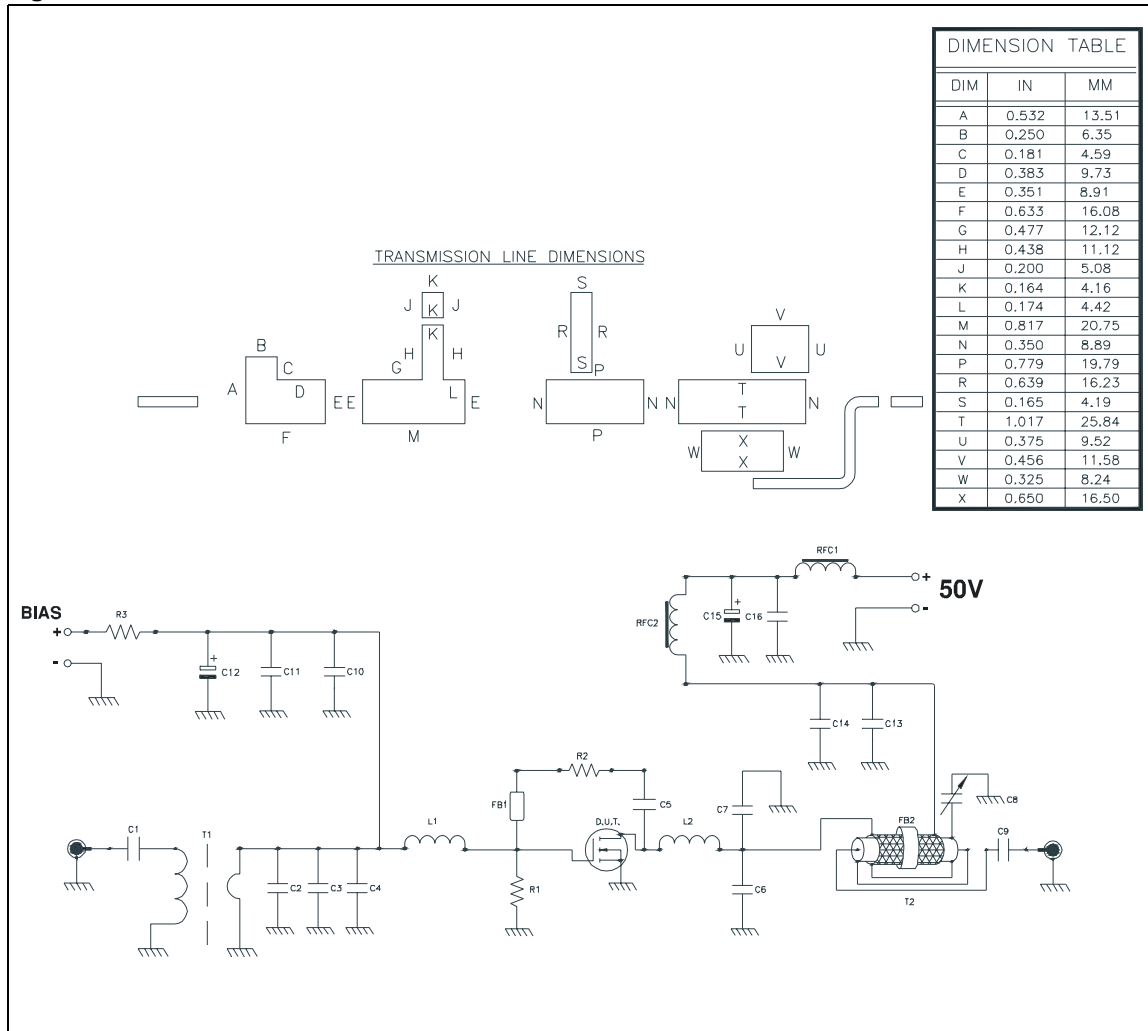


Figure 10. Pout Vs Drain Voltage



4 Test Circuit

Figure 11. 30 MHz Test Circuit Schematic



Note: 1 Dimension at component symbol are reference for component placement.

2 Gap between group and trasmission files are 0.056[1.42] typ.

3 Transmission line are not 1:1 scale.

4 Input and output trasmission line are 50Ω

Table 8. 30 MHz Test Circuit Component Part List

Symbol	Description
C1,C9	0.01 μ F / 500 V SURFACE MOUNT CERAMIC CHIP CAPACITOR
C2, C3	750 pF ATC 700B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C4	300 pF ATC 700B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C5,C10,C11,C14,C16	10000 pF ATC 200B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C6	510 pF ATC 700B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C7	300 pF ATC 700B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C8	175-680 pF TYPE 46 STANDARD TRIMMER CAPACITOR
C12	47 μ F / 63 V ALUMINUM ELECTROLYTIC RADIAL LEAD CAPACITOR
C13	1200 pF ATC 700B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C15	100 μ F / 63 V ALUMINUM ELECTROLYTIC RADIAL LEAD CAPACITOR
R1,R3	1 K Ω 1 W SURFACE MOUNT CHIP RESISTOR
R2	560 Ω 2 W WIRE-WOUND AXIAL LEAD RESISTOR
T1	HF 2-30 MHz SURFACE MOUNT 9:1 TRANSFORMER
T2	RG - 142B/U 50 Ω COAXIAL CABLE OD = 0.165[4.18] L 15"[381.00] COVERED WITH 15"[381.00] TINNED COPPER TUBULAR BRAND 13/65" [5.1] WIDTH
L1	1 3/4 TURN AIR-WOUND 16 AWG ID = 0.219 [5.56] POLY-COATED MAGNET WIRE
L2	1 3/4 TURN AIR-WOUND 12 AWG ID = 0.250 [6.34] BUS BAR WIRE
RFC1,RFC2	3 TURNS 14 AWG WIRE THROUGH FAIR RITE TOROID
FB1	SURFACE MOUNT EMI SHIELD BEAD
FB2	TOROID
PCB	ULTRALAM 2000. 0.030" THK, $\epsilon_r = 2.55$, 2 Oz ED CU BOTH SIDES

Figure 12. 30 MHz Test Circuit Photomaster

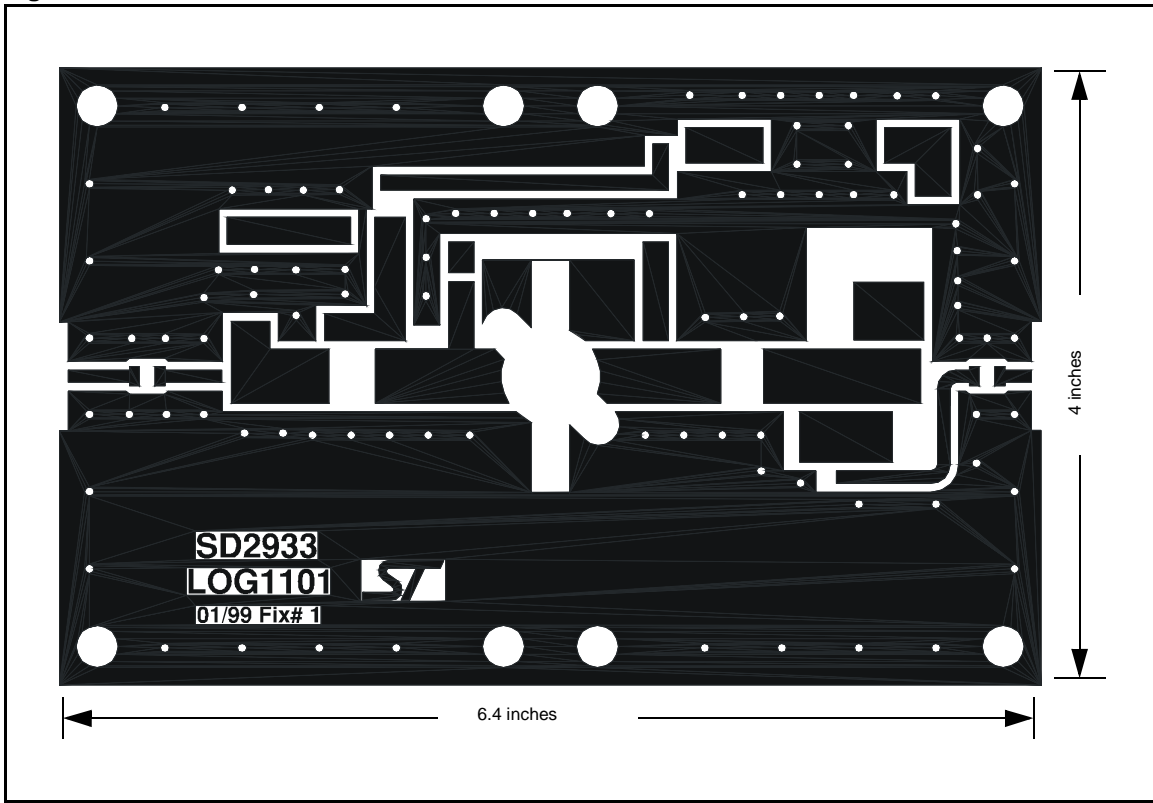
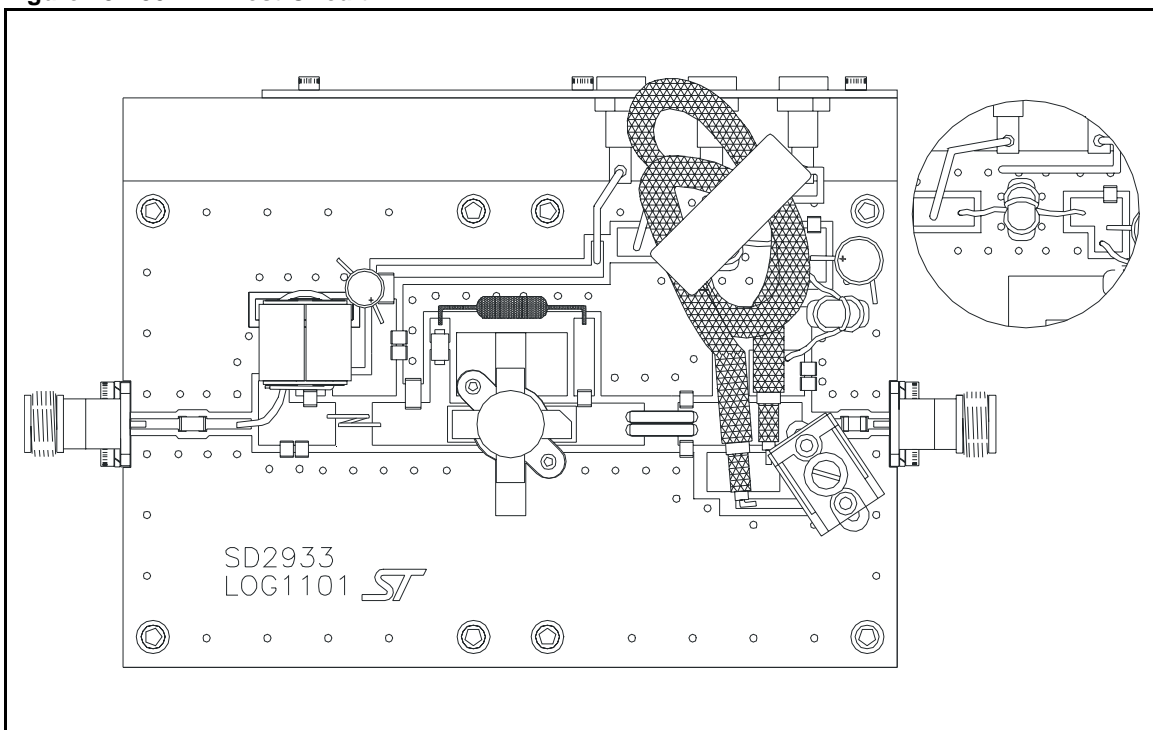


Figure 13. 30 MHz Test Circuit

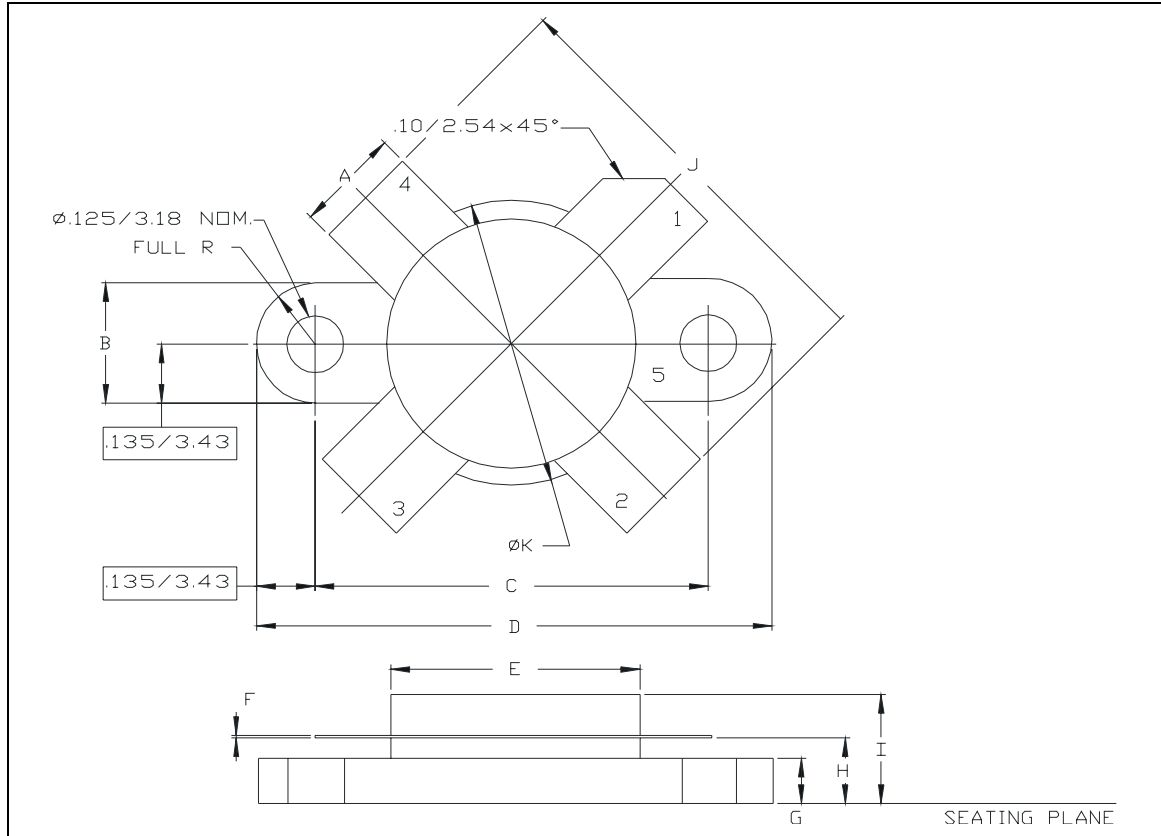


5 Mechanical Data

Table 9. M177 (.550 DIA 4/L N/HERM W/FLG)

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP	MAX.
A	5.72		5.97	0.225		0.235
B	6.73		6.96	0.265		0.275
C	21.84		22.10	0.860		0.870
D	28.70		28.96	1.130		1.140
E	13.84		14.10	0.545		0.555
F	0.08		0.18	0.003		0.007
G	2.49		2.74	0.098		0.108
H	3.81		4.32	0.150		0.170
I			7.11			0.280
J	27.43		28.45	1.080		1.120
K	15.88		16.13	0.625		0.635

Figure 14. M177 Package Dimensions



6 Revision History

Date	Revision	Description of Changes
18-Oct-2005	1	First Issue.
04-Jan-2006	2	Complete version

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