# **BLF6G22-180PN**

## **Power LDMOS transistor**

Rev. 02 — 23 April 2008

**Product data sheet** 

### 1. Product profile

### 1.1 General description

180 W LDMOS power transistor for base station applications at frequencies from 2000 MHz to 2200 MHz.

Table 1. Typical performance

RF performance at  $T_{case}$  = 25 °C in a common source class-AB production test circuit.

Mode of operation	f	V <sub>DS</sub>	P <sub>L(AV)</sub>	Gp	η <sub>D</sub>	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
2-carrier W-CDMA	2110 to 2170	32	50	17.5	27.5	-35 <mark>[1]</mark>

<sup>[1]</sup> Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7.5 dB at 0.01 % probability on CCDF per carrier; carrier spacing 5 MHz.

#### **CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

### 1.2 Features

- Typical 2-carrier W-CDMA performance at frequencies of 2110 MHz and 2170 MHz, a supply voltage of 32 V and an I<sub>Dq</sub> of 1600 mA:
  - Average output power = 50 W
  - Power gain = 17.5 dB (typ)
  - ◆ Efficiency = 27.5 %
  - ◆ ACPR = -35 dBc
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (2000 MHz to 2200 MHz)
- Internally matched for ease of use
- Qualified up to a supply voltage of 32 V
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)



### 1.3 Applications

■ RF power amplifiers for W-CDMA base stations and multicarrier applications in the 2000 MHz to 2200 MHz frequency range

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline Graphic symbol
1	drain1	
2	drain2	1 2 1
3	gate1	5 3
4	gate2	3 4 5
5	source	[1] 4 2 2 sym117

<sup>[1]</sup> Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package	)	
	Name	Description	Version
BLF6G22-180PN	-	flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads	SOT539A

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-0.5	+13	V
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>case</sub>	case temperature		-	150	°C
Tj	junction temperature		-	225	°C

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
R <sub>th(j-case)</sub>	thermal resistance from junction to case	$T_{case} = 80  ^{\circ}C;  P_{L(AV)} = 50  W$	0.45	K/W

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#### 6. Characteristics

Table 6. Characteristics

 $T_i = 25 \,^{\circ}C$  per section; unless otherwise specified.

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Parameter	Conditions	Min	Тур	Max	Unit		
drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 0.5 \text{ mA}$	65	-	-	V		
gate-source threshold voltage	$V_{DS} = 10 \text{ V}; I_{D} = 144 \text{ mA}$	1.575	1.9	2.3	V		
gate-source quiescent voltage	$V_{DS} = 32 \text{ V}; I_{D} = 800 \text{ mA}$	1.725	2.1	2.45	V		
drain leakage current	$V_{GS} = 0 V$						
	V <sub>DS</sub> = 28 V	-	-	3	μΑ		
	$V_{DS} = 60 \text{ V}$	-	-	5	μΑ		
drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	25	-	Α		
gate leakage current	$V_{GS} = 11 \text{ V}; V_{DS} = 0 \text{ V}$	-	-	300	nΑ		
forward transconductance	$V_{DS} = 10 \text{ V}; I_D = 7.2 \text{ A}$	-	10	-	S		
drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $I_D = 5 \text{ A}$	-	0.1	0.165	Ω		
	drain-source breakdown voltage gate-source threshold voltage gate-source quiescent voltage drain leakage current  drain cut-off current  gate leakage current forward transconductance drain-source on-state	$\begin{array}{ll} \text{drain-source breakdown} & \text{V}_{GS} = 0 \text{ V; I}_D = 0.5 \text{ mA} \\ \text{voltage} \\ \text{gate-source threshold voltage} & \text{V}_{DS} = 10 \text{ V; I}_D = 144 \text{ mA} \\ \text{gate-source quiescent voltage} & \text{V}_{DS} = 32 \text{ V; I}_D = 800 \text{ mA} \\ \text{drain leakage current} & \text{V}_{GS} = 0 \text{ V} \\ \hline & \text{V}_{DS} = 28 \text{ V} \\ \hline & \text{V}_{DS} = 60 \text{ V} \\ \text{drain cut-off current} & \text{V}_{GS} = \text{V}_{GS(th)} + 3.75 \text{ V; } \\ \hline & \text{V}_{DS} = 10 \text{ V} \\ \text{gate leakage current} & \text{V}_{GS} = 11 \text{ V; V}_{DS} = 0 \text{ V} \\ \text{forward transconductance} & \text{V}_{DS} = 10 \text{ V; I}_D = 7.2 \text{ A} \\ \text{drain-source on-state} & \text{V}_{GS} = \text{V}_{GS(th)} + 3.75 \text{ V;} \\ \end{array}$	$\begin{array}{llllllllllllllllllllllllllllllllllll$	$\begin{array}{c} \text{drain-source breakdown} \\ \text{voltage} \\ \\ \text{gate-source threshold voltage} \\ \text{gate-source quiescent voltage} \\ \\ \text{V}_{DS} = 10 \text{ V; I}_{D} = 144 \text{ mA} \\ 1.575 & 1.9 \\ \\ \text{gate-source quiescent voltage} \\ \\ \text{V}_{DS} = 32 \text{ V; I}_{D} = 800 \text{ mA} \\ 1.725 & 2.1 \\ \\ \text{drain leakage current} \\ \\ \hline \\ V_{DS} = 28 \text{ V} \\ \\ \hline \\ V_{DS} = 28 \text{ V} \\ \\ \hline \\ V_{DS} = 60 \text{ V} \\ \\ \\ \text{drain cut-off current} \\ \\ \hline \\ \text{V}_{GS} = V_{GS(th)} + 3.75 \text{ V; } \\ \\ \hline \\ \text{Solution} \\ \\ \text{Solution} \\$	$\begin{array}{c} \text{drain-source breakdown} \\ \text{voltage} \\ \\ \text{gate-source threshold voltage} \\ \text{gate-source quiescent voltage} \\ \\ \text{V}_{DS} = 10 \text{ V; I}_{D} = 144 \text{ mA} \\ \text{1.575} \\ \text{1.9} \\ \text{2.3} \\ \text{2.45} \\ \\ \text{drain leakage current} \\ \\ \begin{array}{c} V_{GS} = 32 \text{ V; I}_{D} = 800 \text{ mA} \\ \text{1.725} \\ \text{2.1} \\ \text{2.45} \\ \\ \text{2.45} \\ \\ \text{V}_{DS} = 28 \text{ V} \\ \text{V}_{DS} = 28 \text{ V} \\ \text{V}_{DS} = 60 \text{ V} \\ \\ \text{V}_{DS} = 60 \text{ V} \\ \\ \text{V}_{DS} = 10 \text{ V} \\ \\ \text{V}_{DS} = 10 \text{ V} \\ \\ \text{Sate leakage current} \\ \text{V}_{GS} = 11 \text{ V; V}_{DS} = 0 \text{ V} \\ \text{V}_{DS} = 10 \text{ V} \\ \\ \text{Grain-source on-state} \\ \text{V}_{GS} = V_{GS(th)} + 3.75 \text{ V;} \\ \text{Color of the current} \\ Color of the$		

### 7. Application information

#### Table 7. Application information

Mode of operation: 2-carrier W-CDMA; PAR 7.5 dB at 0.01 % probability on CCDF; 3GPP test model 1; 1 to 64 PDPCH;  $f_1$  = 2112.5 MHz;  $f_2$  = 2117.5 MHz;  $f_3$  = 2162.5 MHz;  $f_4$  = 2167.5 MHz; RF performance at  $V_{DS}$  = 32 V;  $I_{Dq}$  = 1600 mA;  $T_{case}$  = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Gp	power gain	$P_{L(AV)} = 50 \text{ W}$	16.3	17.5	18.7	dB
RLin	input return loss	$P_{L(AV)} = 50 \text{ W}$	-	-10	-6.5	dB
$\eta_{D}$	drain efficiency	$P_{L(AV)} = 50 \text{ W}$	25	27.5	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 50 \text{ W}$	-	-35	-33	dBc

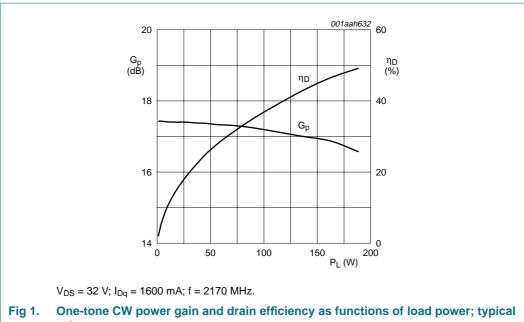
#### Table 8. Application information

Mode of operation: 1-carrier W-CDMA; PAR 7.5 dB at 0.01 % probability on CCDF; 3GPP test model 1; 1 to 64 PDPCH;  $f_1$  = 2162.5 MHz;  $f_2$  = 2167.5 MHz; RF performance at  $V_{DS}$  = 32 V;  $I_{Dq}$  = 1600 mA;  $T_{case}$  = 25 °C; unless otherwise specified; in a class-AB production test circuit.

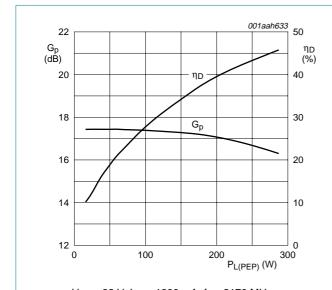
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
PARO	output peak-to-average ratio	$P_{L(AV)} = 115 \text{ W};$ at 0.01 % probability on CCDF	4.05	4.5	-	dB

### 7.1 Ruggedness in class-AB operation

The BLF6G22-180PN is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS}$  = 28 V;  $I_{Dq}$  = 1600 mA;  $P_L$  = 180 W (CW); f = 2170 MHz.

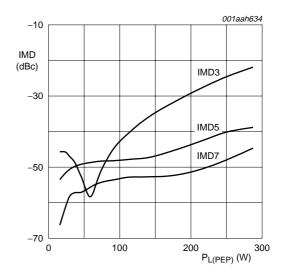


values



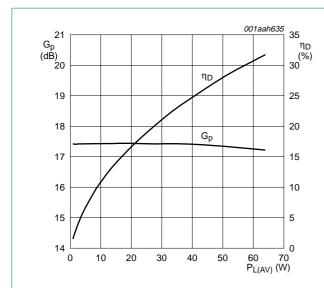
 $V_{DS}$  = 32 V;  $I_{Dq}$  = 1600 mA;  $f_1$  = 2170 MHz;  $f_2$  = 2170.1 MHz.

Fig 2. Two-tone CW power gain and drain efficiency as functions of peak envelope load power; typical values



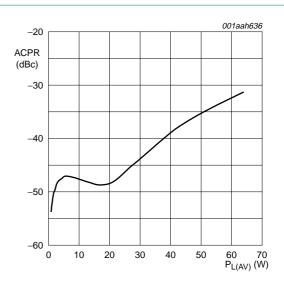
 $V_{DS} = 32 \ V; \ I_{Dq} = 1600 \ mA; \ f_1 = 2170 \ MHz; \ f_2 = 2170.1 \ MHz.$ 

Fig 3. Two-tone intermodulation distortion as a function of peak envelope load power; typical values



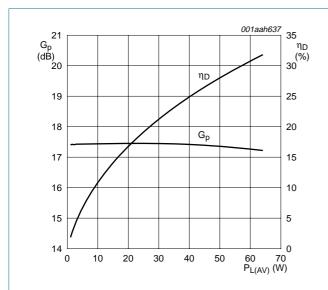
 $V_{DS} = 32 \text{ V}; I_{Dq} = 1600 \text{ mA}; f_1 = 2162.5 \text{ MHz}; f_2 = 2167.5 \text{ MHz}; carrier spacing 5 \text{ MHz}.$ 

Fig 4. 2-carrier W-CDMA power gain and drain efficiency as functions of average load power; typical values



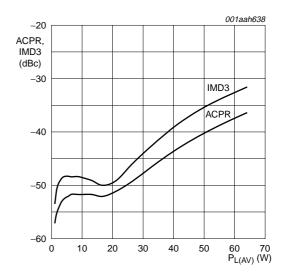
 $V_{DS} = 32 \text{ V; } I_{Dq} = 1600 \text{ mA; } f_1 = 2162.5 \text{ MHz; } f_2 = 2167.5 \text{ MHz; } \text{carrier spacing 5 MHz.}$ 

Fig 5. 2-carrier W-CDMA adjacent channel power ratio as function of average load power; typical values



 $V_{DS}$  = 32 V;  $I_{Dq}$  = 1600 mA;  $f_1$  = 2157.5 MHz;  $f_2$  = 2167.5 MHz; carrier spacing 10 MHz.

Fig 6. 2-carrier W-CDMA power gain and drain efficiency as functions of average load power; typical values

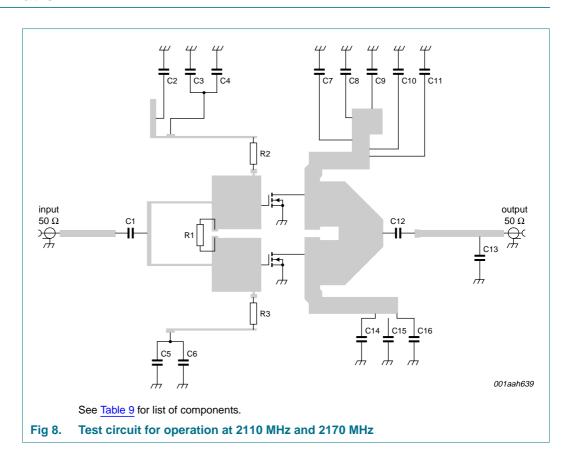


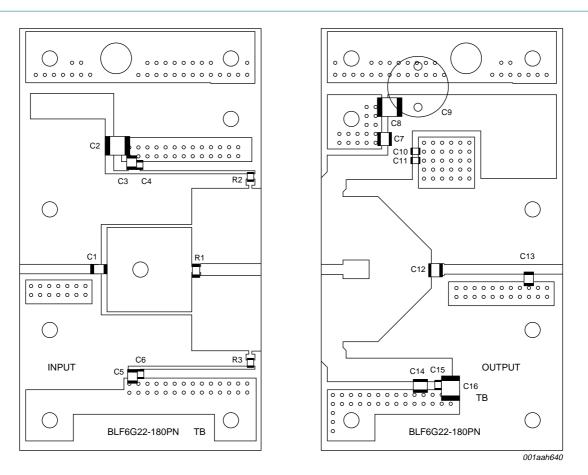
$$\begin{split} V_{DS} = 32 \text{ V; } I_{Dq} = 1600 \text{ mA; } f_1 = 2157.5 \text{ MHz;} \\ f_2 = 2167.5 \text{ MHz; } carrier \text{ spacing } 10 \text{ MHz.} \end{split}$$

Fig 7. 2-carrier W-CDMA adjacent channel power ratio and third order intermodulation distortion as functions of average load power; typical values

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## 8. Test information





Striplines are on a double copper-clad Rogers R04350 Printed-Circuit Board (PCB) with  $\epsilon_r$  = 3.5 and thickness = 0.76 mm. See Table 9 for list of components.

Fig 9. Component layout for 2110 MHz and 2170 MHz test circuit

**Table 9. List of components** For test circuit, see Figure 8 and Figure 9.

Component	Description	Value	Remarks
C1, C3, C5	ATC multilayer ceramic chip capacitor	10 pF	<u>[1]</u>
C2, C8, C16	TDK multilayer ceramic chip capacitor	4.7 μF	
C4, C6	TDK multilayer ceramic chip capacitor	220 nF	
C7, C14	ATC multilayer ceramic chip capacitor	10 pF	[2]
C9	electrolytic capacitor	220 $\mu F$ ; 63 V	
C10, C11, C15	Murata ceramic chip capacitor	100 nF	
C12	ATC multilayer ceramic chip capacitor	15 pF	[2]
C13	ATC multilayer ceramic chip capacitor	0.3 pF	[1]
R1	chip resistor	33 Ω	
R2, R3	chip resistor	$5.6~\Omega$	

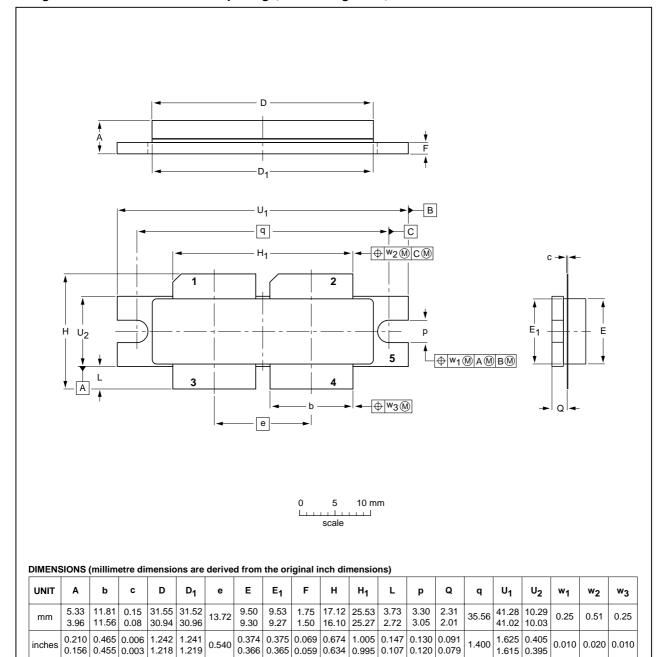
<sup>[1]</sup> American technical ceramics type 100B or capacitor of same quality.

<sup>[2]</sup> American technical ceramics type 180R or capacitor of same quality.

### 9. Package outline

#### Flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads

SOT539A



OUTLINE		REFER	RENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE
SOT539A					<del>99-12-28</del> 00-03-03

Fig 10. Package outline SOT539A

### 10. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
IMD	InterModulation Distortion
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
PDPCH	transmission Power of the Dedicated Physical CHannel
RF	Radio Frequency
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

## 11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF6G22-180PN_2	20080423	Product data sheet	-	BLF6G22-180PN_1
BLF6G22-180PN_1	20080221	Preliminary data sheet	-	-

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#### 12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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