

NTMS4107N

Power MOSFET

30 V, 18 A, Single N-Channel, SO-8

Features

- Ultra Low $R_{DS(on)}$ (at 4.5 V_{GS}), Low Gate Resistance and Low Q_G
- Optimized for Low Side Synchronous Applications
- High Speed Switching Capability
- Pb-Free Package is Available

Applications

- Notebook Computer Vcore Applications
- Network Applications
- DC-DC Converters

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	30	V
Gate-to-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	15	A
		$T_A = 85^\circ\text{C}$	11	
	$t \leq 10\text{ s}$	$T_A = 25^\circ\text{C}$	18	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	1.67	W
		$t \leq 10\text{ s}$	2.5	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	11	A
		$T_A = 85^\circ\text{C}$	8.0	
		$T_A = 25^\circ\text{C}$	0.93	
Power Dissipation (Note 2)		P_D		W
Pulsed Drain Current	$t_p = 10\ \mu\text{s}$	I_{DM}	56	A
Operating Junction and Storage Temperature		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Continuous Source Current (Body Diode)		I_S	3.0	A
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 30\text{ V}$, $V_{GS} = 10\text{ V}$, $I_{PK} = 32\text{ A}$, $L = 1\text{ mH}$, $R_G = 25\ \Omega$)		E_{AS}	512	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	75	$^\circ\text{C/W}$
Junction-to-Ambient - $t \leq 10\text{ s}$ (Note 1)	$R_{\theta JA}$	50	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	135	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

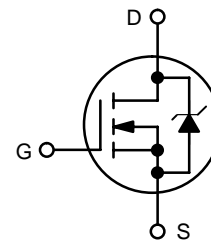
1. Surface-mounted on FR4 board using 1" sq. pad size (Cu area = 1.127" sq. [1 oz] including traces).
2. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.412" sq.).



ON Semiconductor®

<http://onsemi.com>

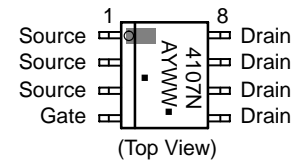
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
30 V	3.4 m Ω @ 10 V	18 A
	4.7 m Ω @ 4.5 V	



MARKING DIAGRAM/ PIN ASSIGNMENT



SO-8
CASE 751
STYLE 12



4107N = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package
 (Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTMS4107NR2	SO-8	2500/Tape & Reel
NTMS4107NR2G	SO-8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTMS4107N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			21		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 24 V	T _J = 25°C		1.0	μA
			T _J = 125°C		10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	1.0		2.5	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J			7.4		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 14 A		4.7	5.5	mΩ
		V _{GS} = 10 V, I _D = 15 A		3.4	4.5	
Forward Transconductance	g _{FS}	V _{DS} = 15 V, I _D = 18 A		25		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 15 V		6000		pF
Output Capacitance	C _{OSS}			1030		
Reverse Transfer Capacitance	C _{RSS}			550		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 15 V, I _D = 18 A		45		nC
Threshold Gate Charge	Q _{G(TH)}			6.5		
Gate-to-Source Charge	Q _{GS}			16.3		
Gate-to-Drain Charge	Q _{GD}			19.3		
Gate Resistance	R _G			0.60		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DS} = 15 V, I _D = 1.0 A, R _G = 6.0 Ω		9.0		ns
Rise Time	t _r			10		
Turn-Off Delay Time	t _{d(OFF)}			94		
Fall Time	t _f			38		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 3.0 A	T _J = 25°C	0.8	1.1	V
			T _J = 125°C	0.6		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 3.0 A		41		ns
Charge Time	t _a			20		
Discharge Time	t _b			21		
Reverse Recovery Charge	Q _{RR}			48		

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

NTMS4107N

TYPICAL PERFORMANCE CURVES

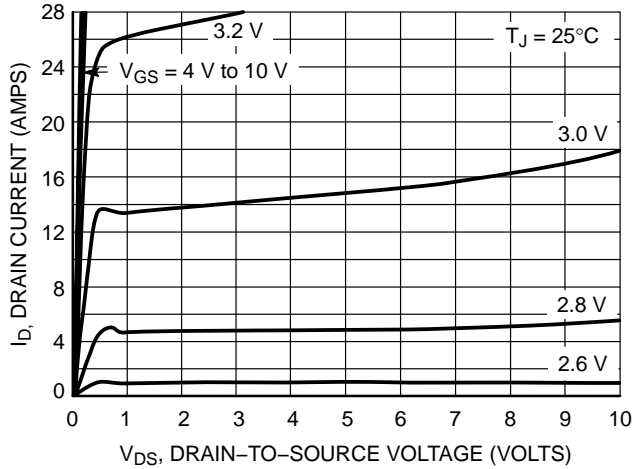


Figure 1. On-Region Characteristics

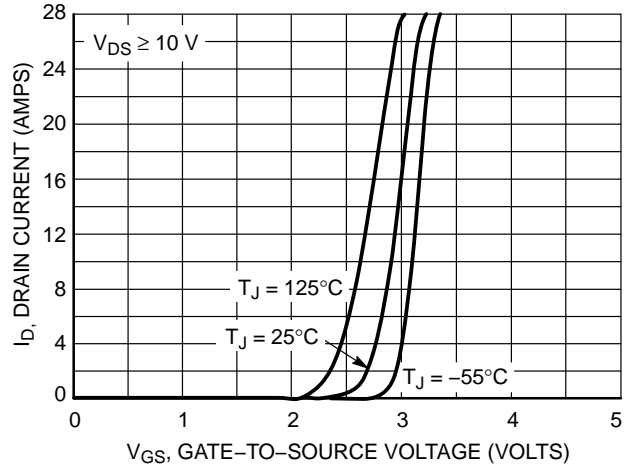


Figure 2. Transfer Characteristics

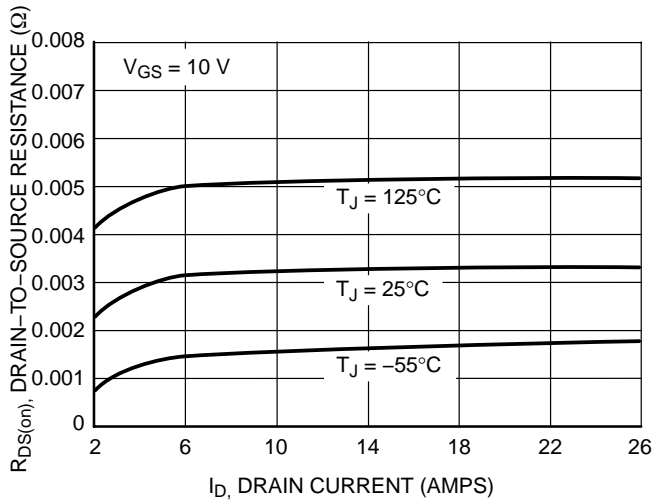


Figure 3. On-Resistance vs. Drain Current and Temperature

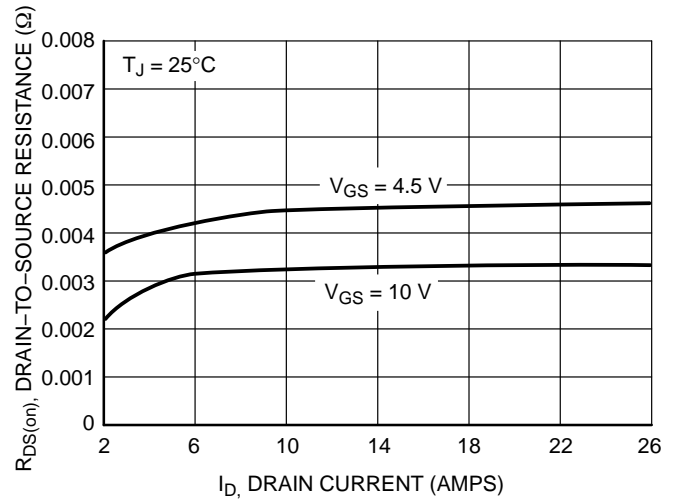


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

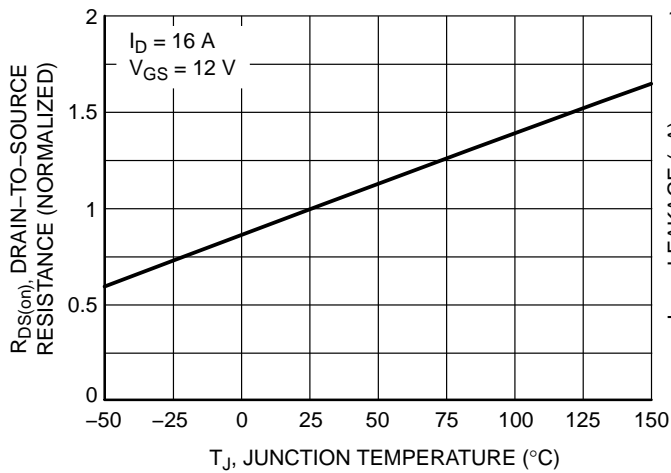


Figure 5. On-Resistance Variation with Temperature

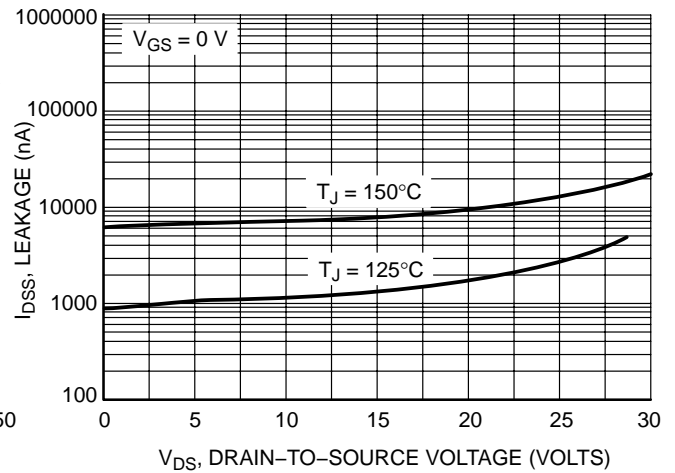


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NTMS4107N

TYPICAL PERFORMANCE CURVES

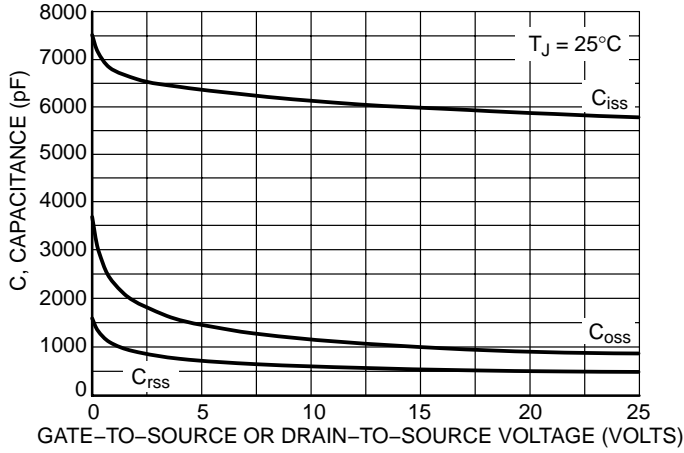


Figure 7. Capacitance Variation

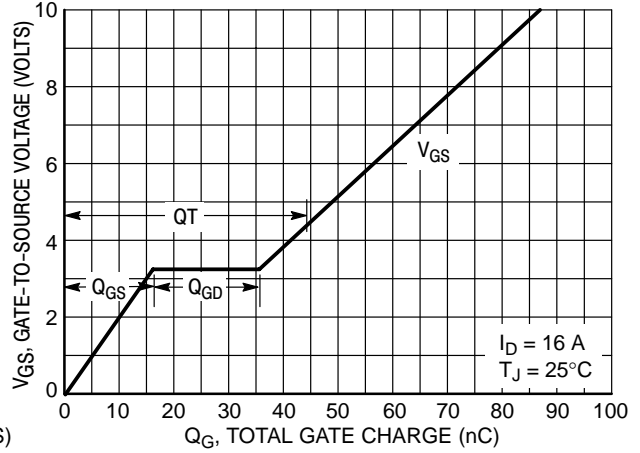


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

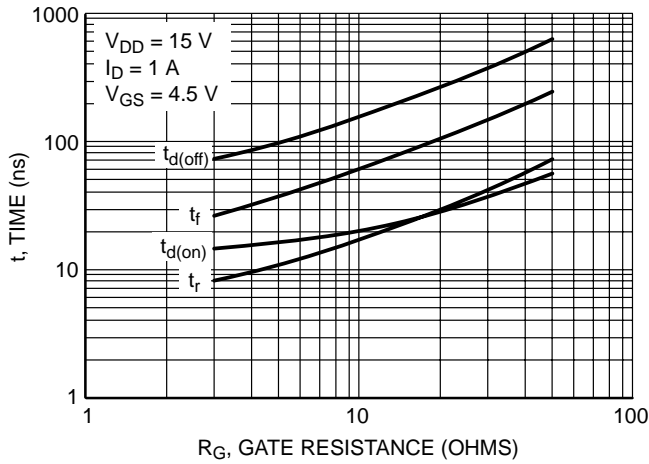


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

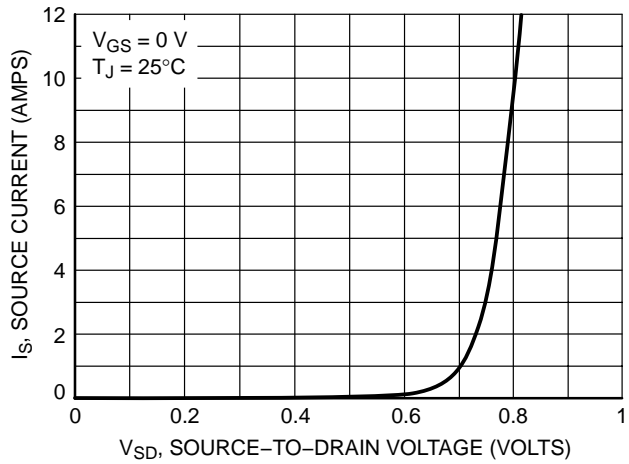


Figure 10. Diode Forward Voltage vs. Current

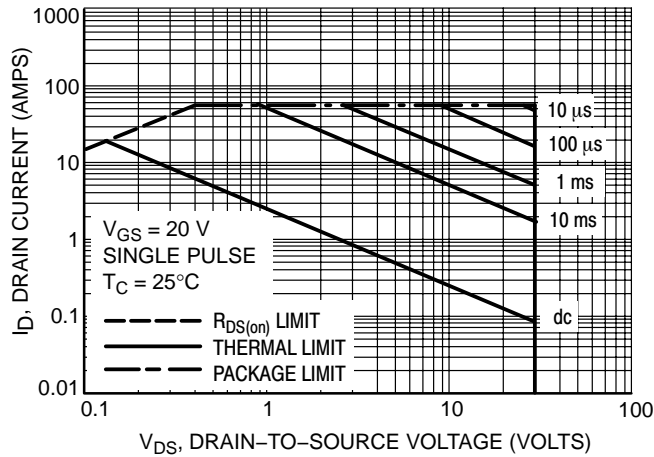
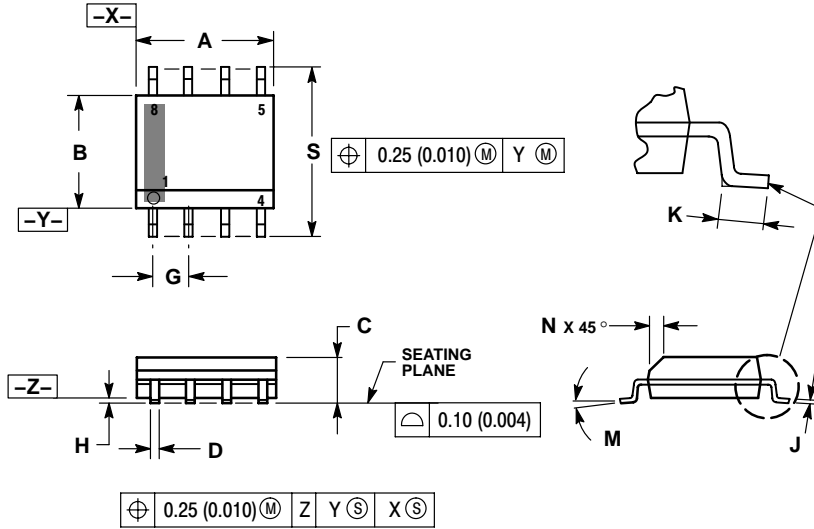


Figure 11. Maximum Rated Forward Biased Safe Operating Area

NTMS4107N

PACKAGE DIMENSIONS

SO-8
CASE 751-07
ISSUE AG



NOTES:

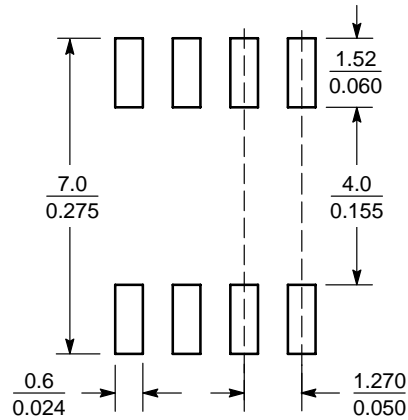
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 12:

- PIN 1: SOURCE
2: SOURCE
3: SOURCE
4: GATE
5: DRAIN
6: DRAIN
7: DRAIN
8: DRAIN


SOLDERING FOOTPRINT*



SCALE 6:1 ($\frac{\text{mm}}{\text{inches}}$)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTMS4107N

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your
local Sales Representative.

NTMS4107N/D