# **Power MOSFET**

# 20 V, 4.5 A, Dual N-Channel, ChipFET™

#### **Features**

- Low R<sub>DS(on)</sub> and Fast Switching Speed
- Leadless ChipFET Package has 40% Smaller Footprint than TSOP-6. Ideal Device for Applications Where Board Space is at a Premium.
- ChipFET Package Exhibits Excellent Thermal Capabilities. Ideal for Applications Where Heat Transfer is Required.
- Pb-Free Packages are Available

#### **Applications**

- DC-DC Buck or Boost Converters
- Low Side Switching
- Optimized for Battery and Low Side Switching Applications in Computing and Portable Equipment

#### **MAXIMUM RATINGS** (T<sub>.I</sub> = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit	
Drain-to-Source Voltage			V <sub>DSS</sub>	20	V	
Gate-to-Source Voltage			$V_{GS}$	±8.0	V	
Continuous Drain	Steady	T <sub>A</sub> =25°C	I <sub>D</sub>	3.3	Α	
Current (Note 1)	State	T <sub>A</sub> =85°C		2.4		
	t ≤ 5 s	T <sub>A</sub> =25°C		4.5		
Power Dissipation (Note 1)	Steady State	T <sub>A</sub> =25°C	P <sub>D</sub>	1.13	W	
Continuous Drain	Steady	T <sub>A</sub> =25°C	I <sub>D</sub>	2.5	Α	
Current (Note 2)		T <sub>A</sub> =85°C		1.8		
Power Dissipation (Note 2)	State	T <sub>A</sub> =25°C	$P_{D}$	0.64	W	
Pulsed Drain Current	t <sub>p</sub> =10 μ	S	I <sub>DM</sub>	10	Α	
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>STG</sub>	–55 to 150	°C	
Source Current (Body Diode)			Is	2.6	Α	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C	

## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	110	°C/W
Junction–to–Ambient – $t \le 5$ s (Note 1)	$R_{\theta JA}$	60	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta,IA}$	195	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
- Surface Mounted on FR4 Board using the minimum recommended pad size (Cu area = 0.214 in sq).
- 3. ESD Rating Information: Human Body Model (HBM) Class 0.

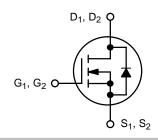


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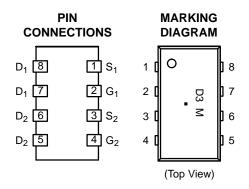
V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> MAX	
20 V	40 mΩ @ 4.5 V	4.5 A	
20 V	55 mΩ @ 2.5 V	4.071	

#### **N-Channel MOSFET**





ChipFET CASE 1206A STYLE 2



D3 = Specific Device Code

M = Month Code

= Pb-Free Package

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Units
OFF CHARACTERISTICS	•	•				•
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V	20			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 16 V			1.0	μΑ
		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 16 V, T <sub>J</sub> = 125°C			10	1
Gate-to-Source Leakage Current	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8.0 \text{ V}$			±100	nA
ON CHARACTERISTICS (Note 4)						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	0.6	0.75	1.2	V
Drain-to-Source On-Resistance	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 3.3 \text{ A}$		40	65	mΩ
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 2.3 A		55	105	1
Forward Transconductance	9FS	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 3.3 A		6.0		S
CHARGES AND CAPACITANCES	•			•	•	•
Input Capacitance	C <sub>iss</sub>			465		pF
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 \text{ V, f} = 1.0 \text{ MHz,}$ $V_{DS} = 16 \text{ V}$		65		
Reverse Transfer Capacitance	C <sub>rss</sub>	V DS = 10 V		30		
Total Gate Charge	Q <sub>G(TOT)</sub>			4.0		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>	$V_{GS} = 2.5 \text{ V}, V_{DS} = 16 \text{ V},$ $I_D = 3.3 \text{ A}$		0.4		
Gate-to-Source Charge	Q <sub>GS</sub>			0.8		
Gate-to-Drain Charge	$Q_{GD}$	1		2.0		
Total Gate Charge	Q <sub>G(TOT)</sub>			6.0		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>	$V_{GS} = 4.5 \text{ V}, V_{DS} = 10 \text{ V},$		0.5		1 !
Gate-to-Source Charge	Q <sub>GS</sub>	I <sub>D</sub> = 3.3 A		0.8		1
Gate-to-Drain Charge	$Q_{GD}$	1		1.7		1
SWITCHING CHARACTERISTICS (Note !	5)	•		•	•	•
Turn-On Delay Time	t <sub>d(on)</sub>			6.0		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 16 V,		17		1
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D = 3.3 \text{ A}, R_G = 2.5 \Omega$		17		1
Fall Time	t <sub>f</sub>	1		5.1		1
DRAIN-SOURCE DIODE CHARACTERIS	TICS	l				
Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0 \text{ V, } I_{S} = 2.6 \text{ A}$		0.8	1.15	V
Reverse Recovery Time	t <sub>RR</sub>			19.5		ns
Charge Time	t <sub>a</sub>	$V_{GS} = 0 \text{ V, } I_{S} = 2.6 \text{ A,}$		6.0		1
Discharge Time	t <sub>b</sub>	$dl_S/dt = 100 \text{ A/}\mu\text{s}$		13		1
Reverse Recovery Charge	Q <sub>RR</sub>	1		7.0		nC
· •				1	ı	

<sup>4.</sup> Pulse Test: Pulse Width  $\leq$  300  $\mu$ s, Duty Cycle  $\leq$  2%.

## **ORDERING INFORMATION**

ONDERING IN GRAINTION				
Device	Package	Shipping <sup>†</sup>		
NTHD5904NT1	ChipFET	3000 / Tape & Reel		
NTHD5904NT1G ChipFET (Pb-Free)		3000 / Tape & Reel		
NTHD5904NT3	ChipFET	10,000 / Tape & Reel		
NTHD5904NT3G	ChipFET (Pb-Free)	10,000 / Tape & Reel		

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

<sup>5.</sup> Switching characteristics are independent of operating junction temperatures.

## TYPICAL PERFORMANCE CURVES (T<sub>J</sub> = 25°C unless otherwise noted)

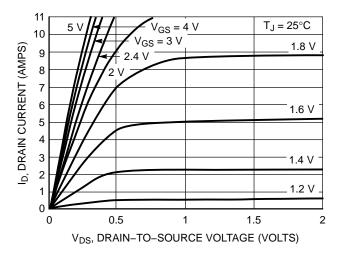


Figure 1. On-Region Characteristics

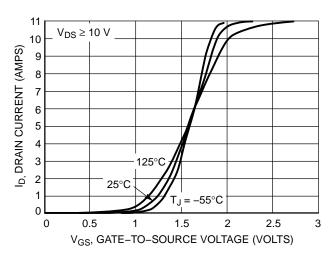


Figure 2. Transfer Characteristics

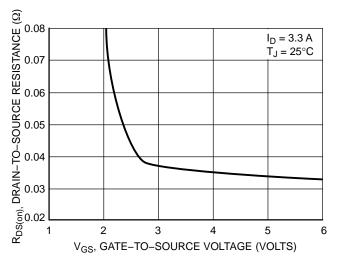


Figure 3. On-Resistance vs. Gate-to-Source Voltage

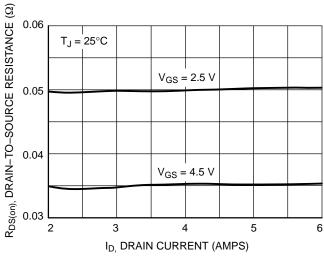


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

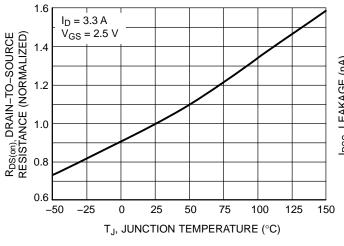


Figure 5. On–Resistance Variation with Temperature

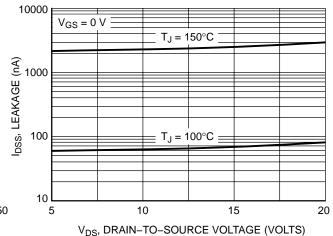
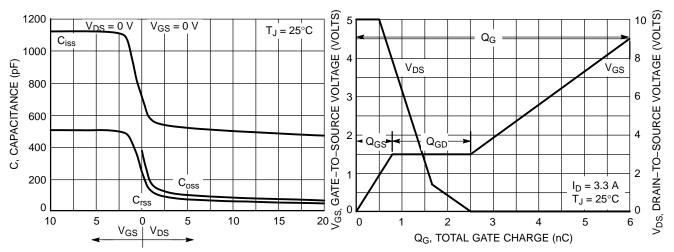


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# TYPICAL PERFORMANCE CURVES (T<sub>J</sub> = 25°C unless otherwise noted)



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 7. Capacitance Variation

Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

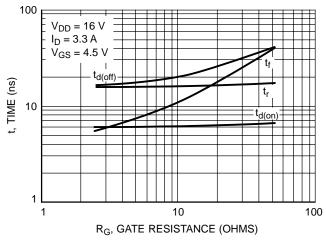


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

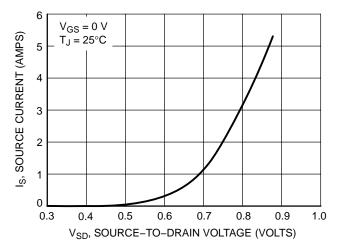
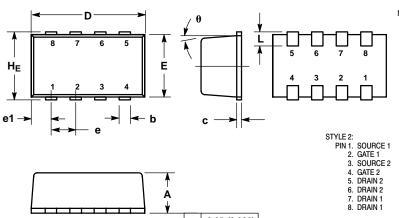


Figure 10. Diode Forward Voltage vs. Current

#### **PACKAGE DIMENSIONS**

## ChipFET™ CASE 1206A-03 ISSUE G



0.05 (0.002)

- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

  2. CONTROLLING DIMENSION: MILLIMETER.

  3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.

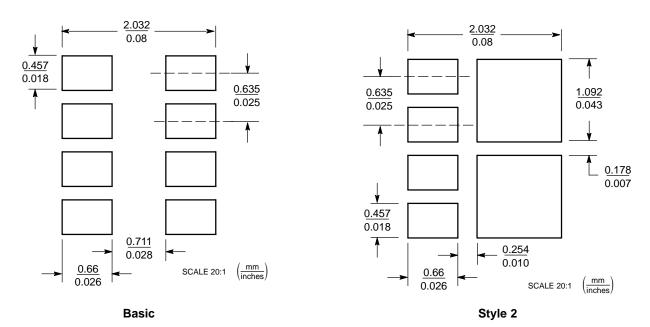
  4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.

  5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.

  6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

	MILLIMETERS				INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX		
Α	1.00	1.05	1.10	0.039	0.041	0.043		
b	0.25	0.30	0.35	0.010	0.012	0.014		
С	0.10	0.15	0.20	0.004	0.006	0.008		
D	2.95	3.05	3.10	0.116	0.120	0.122		
E	1.55	1.65	1.70	0.061	0.065	0.067		
е	0.65 BSC				0.025 BSC			
e1	0.55 BSC			0.022 BSC				
L	0.28	0.35	0.42	0.011	0.014	0.017		
HE	1.80	1.90	2.00	0.071	0.075	0.079		
θ	5° NOM				5° NOM			

## **SOLDERING FOOTPRINT\***



\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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