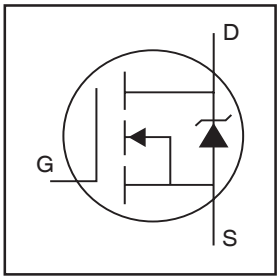
PD - 96896

International
IOR Rectifier

**AUTOMOTIVE MOSFET**

# IRLR3705Z
# IRLU3705Z

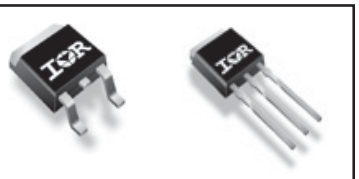
HEXFET® Power MOSFET




$V_{DSS}$ = 55V

$R_{DS(on)}$ = 8.0mΩ

$I_D$ = 42A



D-Pak IRLR3705Z | I-Pak IRLU3705Z

## Features

- Logic Level
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax

## Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating . These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

## Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V (Silicon Limited) | 89 | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10V | 63 | |
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V (Package Limited) | 42 | |
| $I_{DM}$ | Pulsed Drain Current ① | 360 | |
| $P_D$ @$T_C$ = 25°C | Power Dissipation | 130 | W |
| | Linear Derating Factor | 0.88 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 16 | V |
| $E_{AS\ (Thermally\ limited)}$ | Single Pulse Avalanche Energy② | 110 | mJ |
| $E_{AS}$ (Tested ) | Single Pulse Avalanche Energy Tested Value ⑥ | 190 | |
| $I_{AR}$ | Avalanche Current ① | See Fig.12a, 12b, 15, 16 | A |
| $E_{AR}$ | Repetitive Avalanche Energy ⑤ | | mJ |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to + 175 | °C |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case ) | |
| | Mounting Torque, 6-32 or M3 screw | 10 lbf•in (1.1N•m) | |

## Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case ⑧ | ––– | 1.14 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB mount) ⑦⑧ | ––– | 40 | |
| $R_{\theta JA}$ | Junction-to-Ambient ⑧ | ––– | 110 | |

HEXFET® is a registered trademark of International Rectifier.

## Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 55 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 250µA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.053 | — | V/°C | Reference to 25°C, $I_D$ = 1mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | 6.5 | 8.0 | mΩ | $V_{GS}$ = 10V, $I_D$ = 42A ③ |
| | | — | — | 11 | | $V_{GS}$ = 5.0V, $I_D$ = 34A ③ |
| | | — | — | 12 | | $V_{GS}$ = 4.5V, $I_D$ = 21A ③ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.0 | — | 3.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA |
| gfs | Forward Transconductance | 89 | — | — | S | $V_{DS}$ = 25V, $I_D$ = 42A |
| $I_{DSS}$ | Drain-to-Source Leakage Current | — | — | 20 | µA | $V_{DS}$ = 55V, $V_{GS}$ = 0V |
| | | — | — | 250 | | $V_{DS}$ = 55V, $V_{GS}$ = 0V, $T_J$ = 125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | — | — | 200 | nA | $V_{GS}$ = 16V |
| | Gate-to-Source Reverse Leakage | — | — | -200 | | $V_{GS}$ = -16V |
| $Q_g$ | Total Gate Charge | — | 44 | 66 | | $I_D$ = 42A |
| $Q_{gs}$ | Gate-to-Source Charge | — | 13 | — | nC | $V_{DS}$ = 44V |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | — | 22 | — | | $V_{GS}$ = 5.0V ③ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 17 | — | | $V_{DD}$ = 28V |
| $t_r$ | Rise Time | — | 150 | — | | $I_D$ = 42A |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 33 | — | ns | $R_G$ = 4.2 Ω |
| $t_f$ | Fall Time | — | 70 | — | | $V_{GS}$ = 5.0V ③ |
| $L_D$ | Internal Drain Inductance | — | 4.5 | — | | Between lead, |
| | | | | | nH | 6mm (0.25in.) |
| $L_S$ | Internal Source Inductance | — | 7.5 | — | | from package |
| | | | | | | and center of die contact |
| $C_{iss}$ | Input Capacitance | — | 2900 | — | | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | — | 420 | — | | $V_{DS}$ = 25V |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 230 | — | pF | $f$ = 1.0MHz |
| $C_{oss}$ | Output Capacitance | — | 1550 | — | | $V_{GS}$ = 0V, $V_{DS}$ = 1.0V, $f$ = 1.0MHz |
| $C_{oss}$ | Output Capacitance | — | 320 | — | | $V_{GS}$ = 0V, $V_{DS}$ = 44V, $f$ = 1.0MHz |
| $C_{oss}$ eff. | Effective Output Capacitance | — | 500 | — | | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 44V ④ |

## Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current | — | — | 42 | | MOSFET symbol |
| | (Body Diode) | | | | A | showing the |
| $I_{SM}$ | Pulsed Source Current | — | — | 360 | | integral reverse |
| | (Body Diode) ① | | | | | p-n junction diode. |
| $V_{SD}$ | Diode Forward Voltage | — | — | 1.3 | V | $T_J$ = 25°C, $I_S$ = 42A, $V_{GS}$ = 0V ③ |
| $t_{rr}$ | Reverse Recovery Time | — | 21 | 42 | ns | $T_J$ = 25°C, $I_F$ = 42A, $V_{DD}$ = 28V |
| $Q_{rr}$ | Reverse Recovery Charge | — | 14 | 28 | nC | di/dt = 100A/µs ③ |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) | | | | |

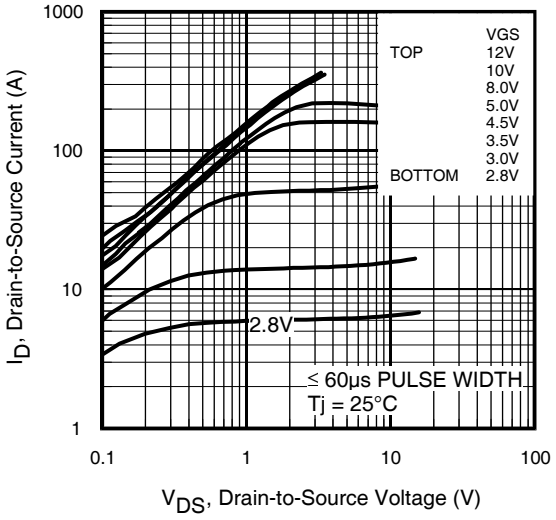



**Fig 1.** Typical Output Characteristics

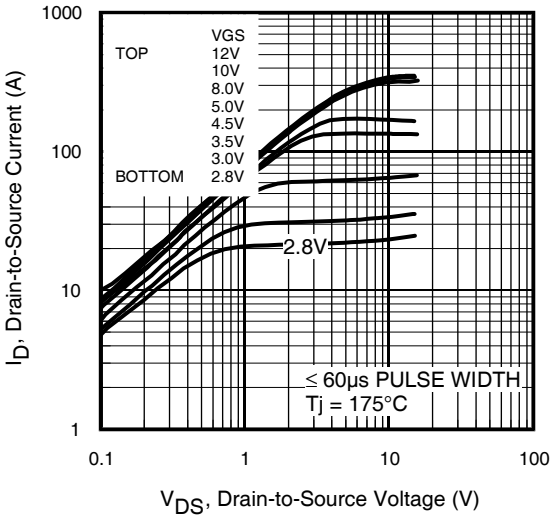



**Fig 2.** Typical Output Characteristics

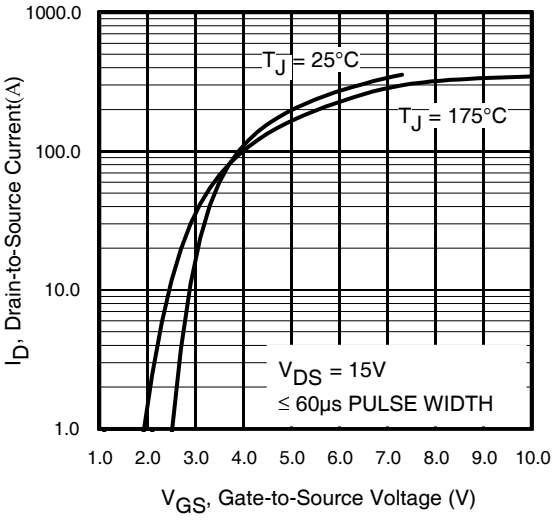



**Fig 3.** Typical Transfer Characteristics

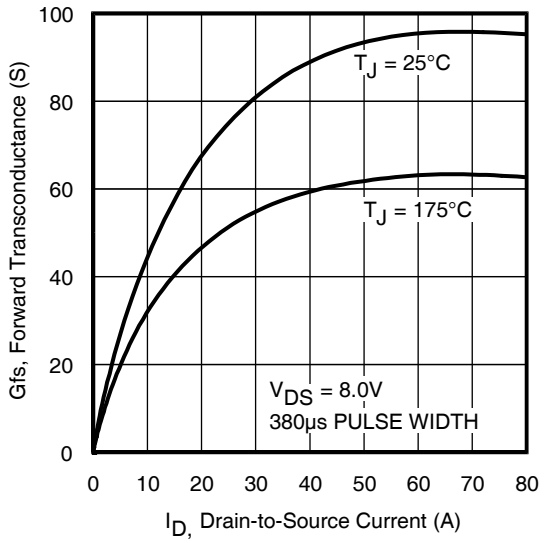



**Fig 4.** Typical Forward Transconductance vs. Drain Current

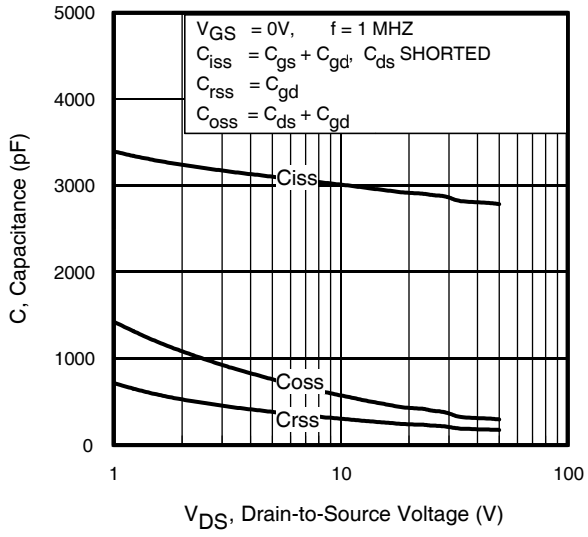



**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage

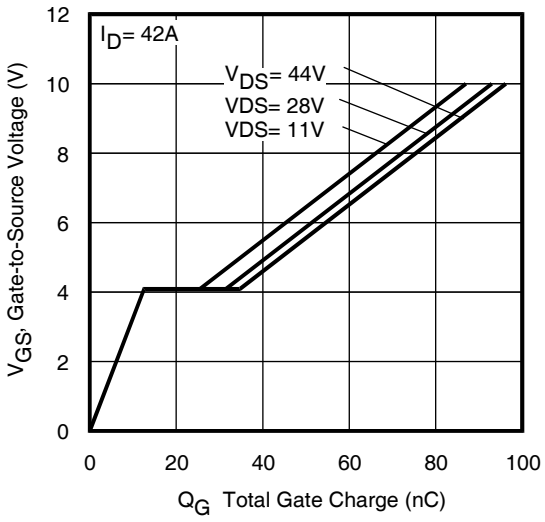



**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

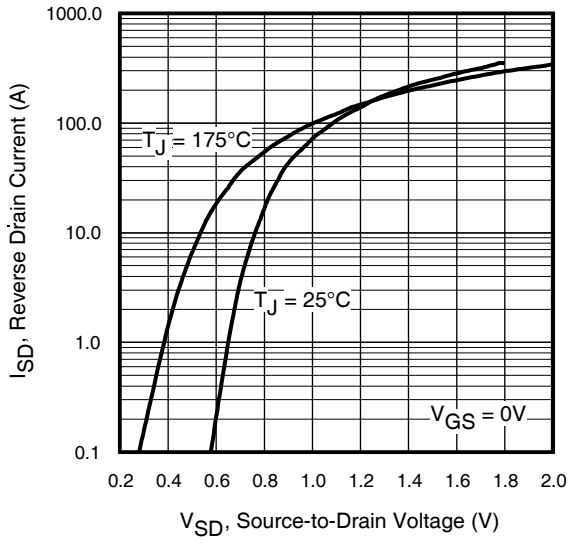



**Fig 7.** Typical Source-Drain Diode Forward Voltage

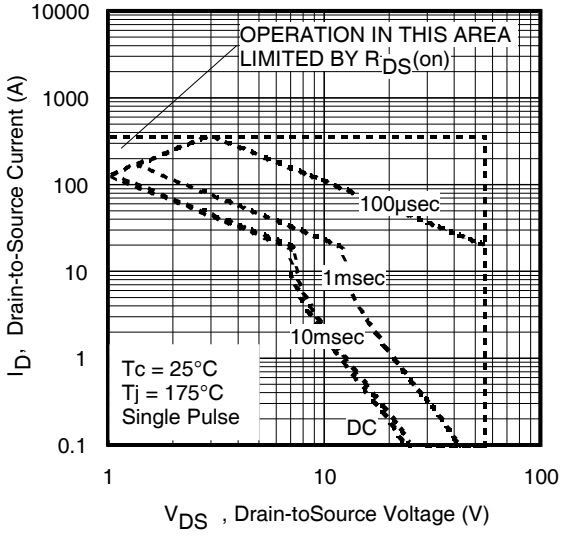



**Fig 8.** Maximum Safe Operating Area

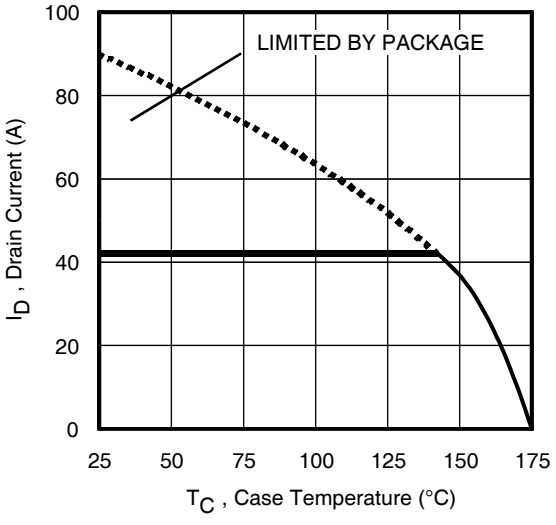



**Fig 9.** Maximum Drain Current vs. Case Temperature

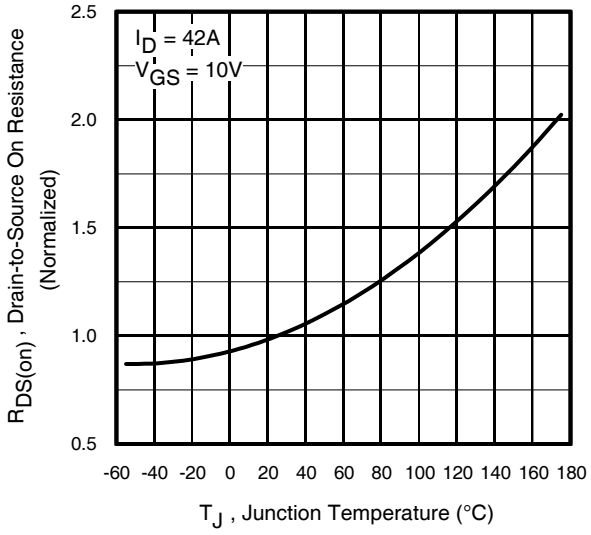



**Fig 10.** Normalized On-Resistance vs. Temperature

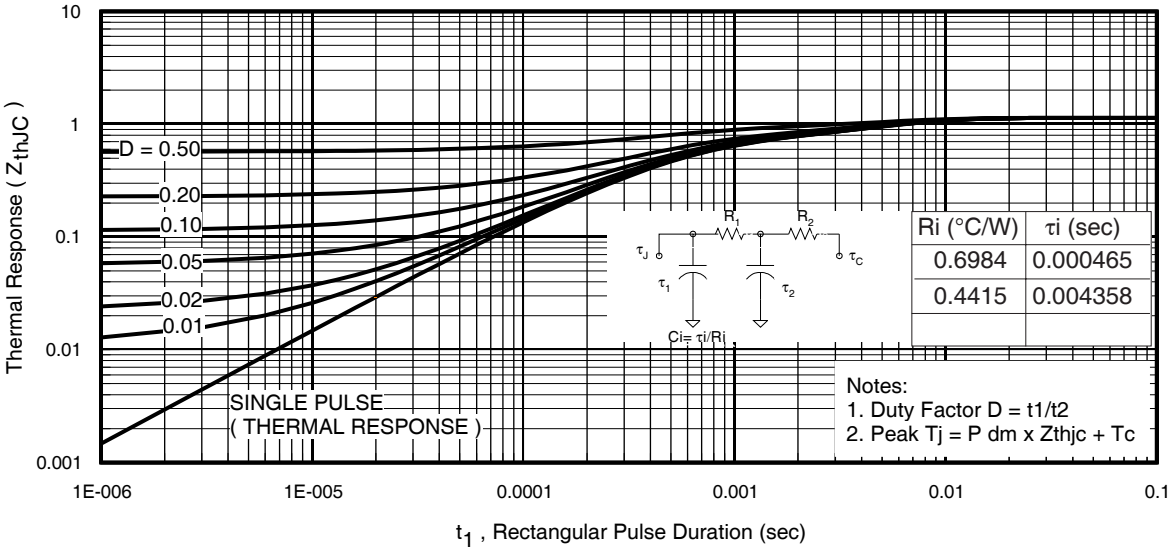



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

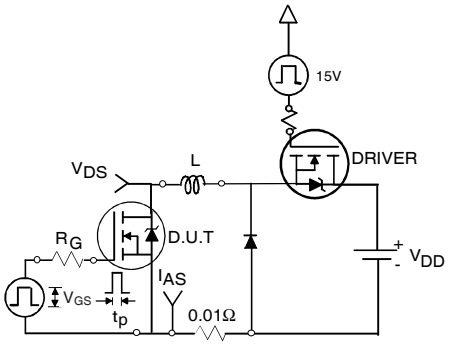



**Fig 12a.** Unclamped Inductive Test Circuit

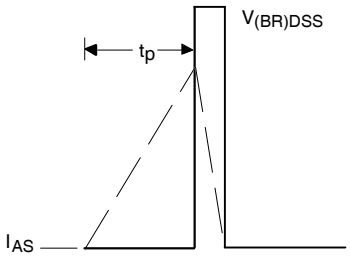



**Fig 12b.** Unclamped Inductive Waveforms

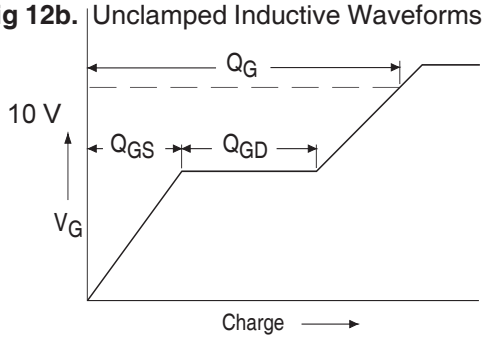



**Fig 13a.** Basic Gate Charge Waveform

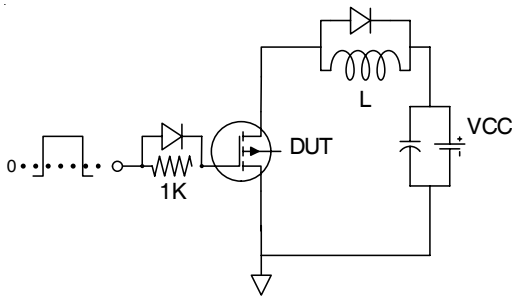



**Fig 13b.** Gate Charge Test Circuit

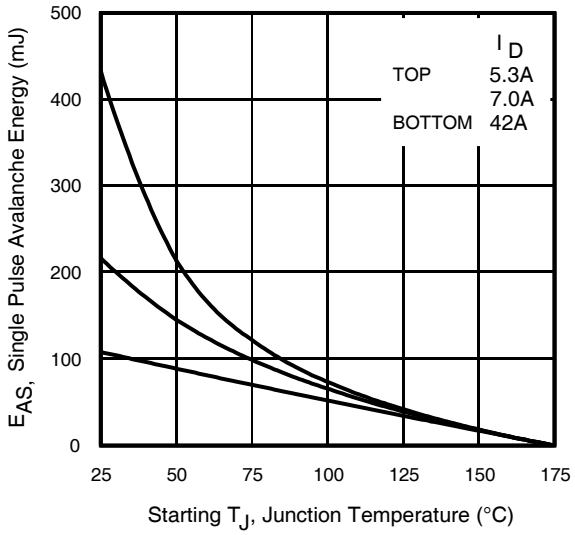



**Fig 12c.** Maximum Avalanche Energy vs. Drain Current

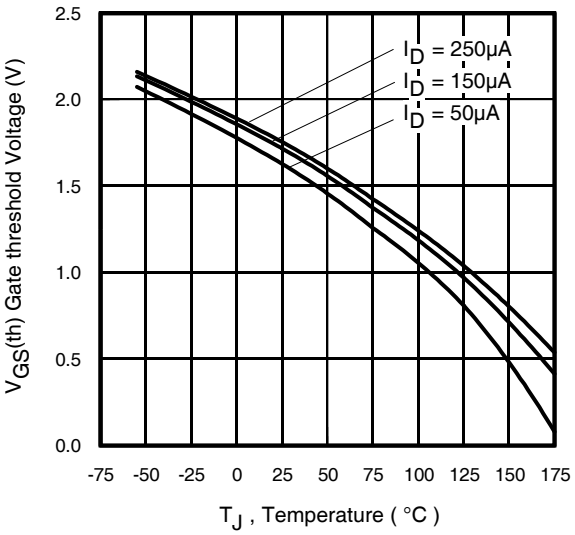



**Fig 14.** Threshold Voltage vs. Temperature

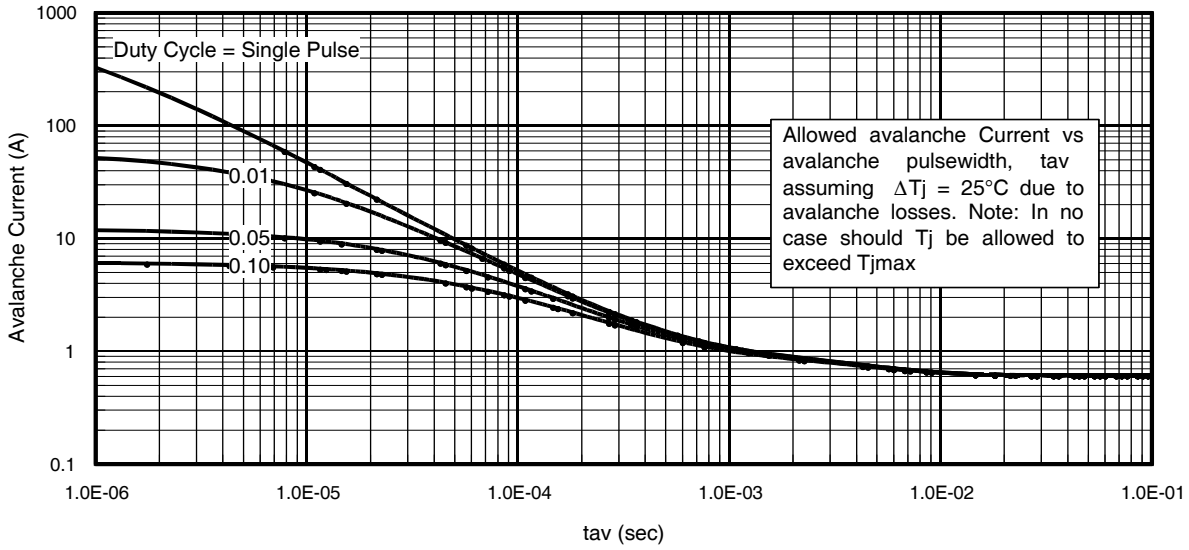



**Fig 15.** Typical Avalanche Current vs.Pulsewidth

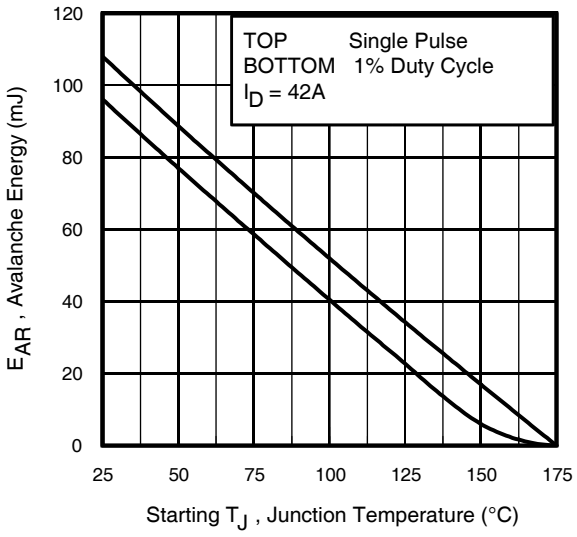



**Fig 16.** Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16: (For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of $T_{jmax}$. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as$T_{jmax}$ is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. $I_{av}$ = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed $T_{jmax}$ (assumed as 25°C in Figure 15, 16).
   $t_{av}$ = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

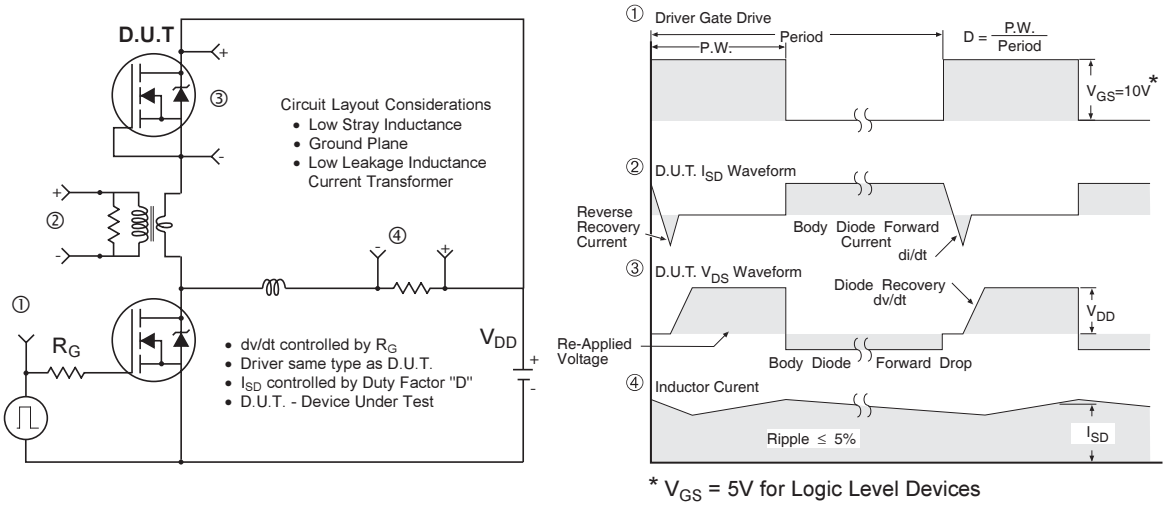



**Fig 17.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

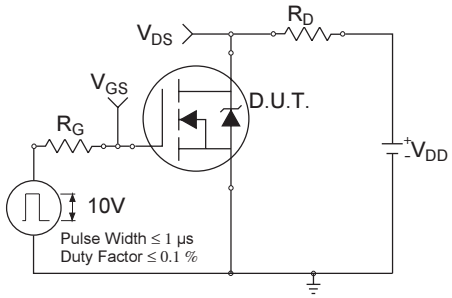



**Fig 18a.** Switching Time Test Circuit

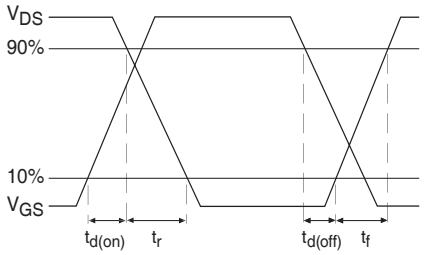
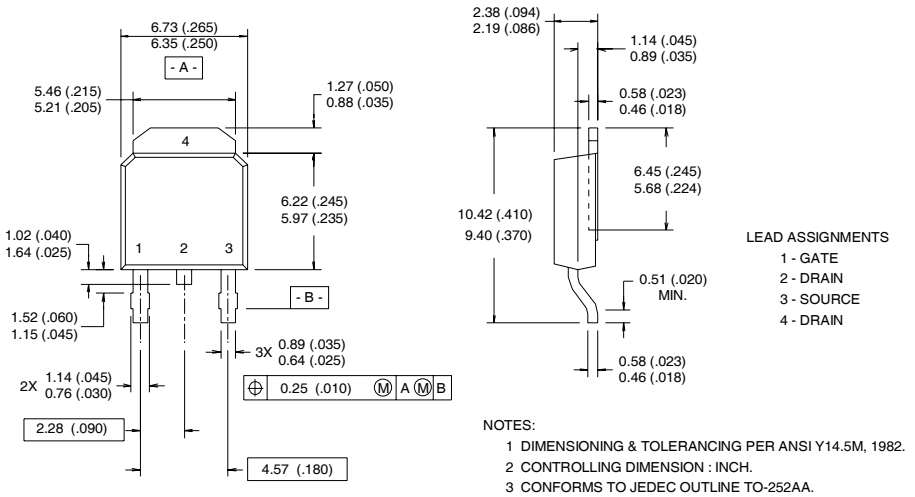



**Fig 18b.** Switching Time Waveforms

## D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)

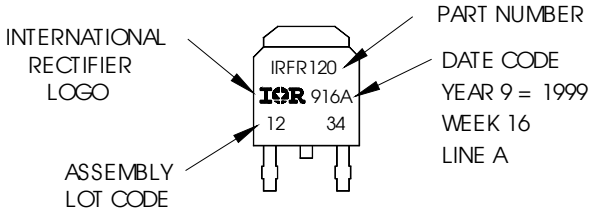



NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

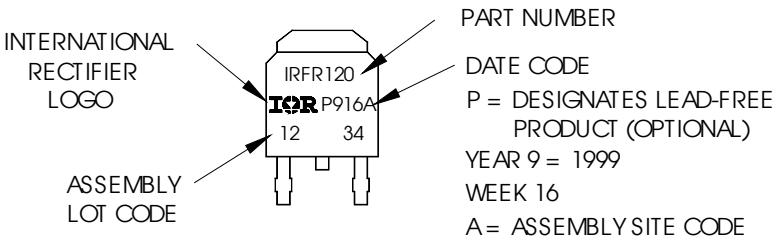
## D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates "Lead-Free"

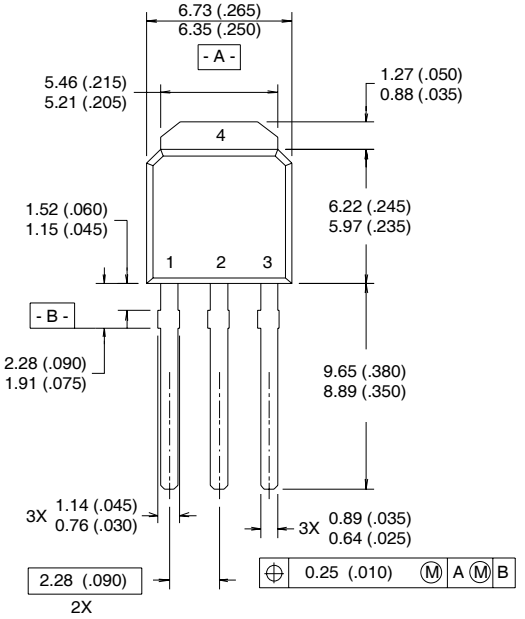


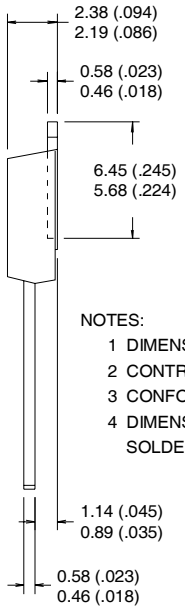

OR



## I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



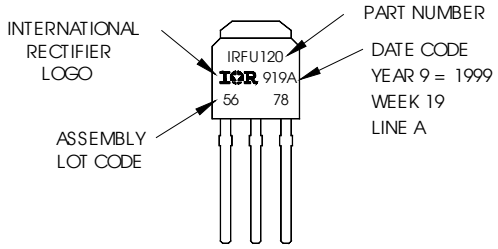

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

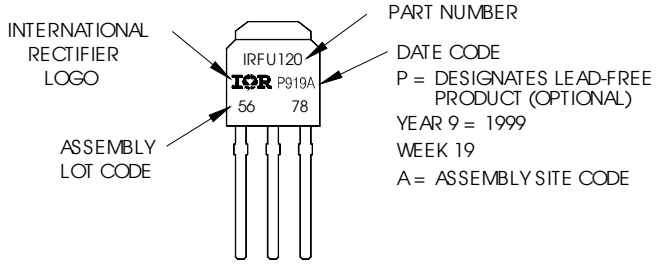
## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 1999
IN THE ASSEMBLY LINE "A"

**Note:** "P" in assembly line position indicates "Lead-Free"

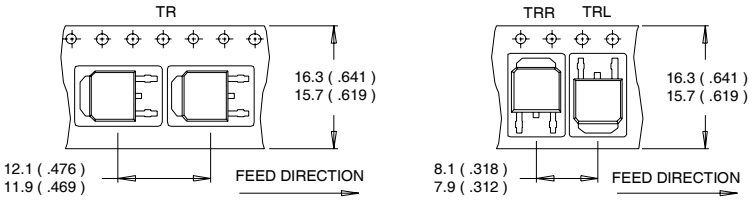



OR

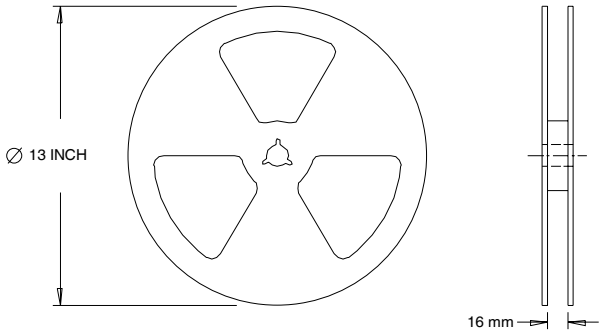


## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)




NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.




NOTES :
1. OUTLINE CONFORMS TO EIA-481.

**Notes:**

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Limited by $T_{Jmax}$, starting $T_J$ = 25°C, L = 0.12mH $R_G$ = 25Ω, $I_{AS}$ = 42A, $V_{GS}$ =10V. Part not recommended for use above this value.

③ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.

④ $C_{oss}$ eff. is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$ .

⑤ Limited by $T_{Jmax}$ , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

⑥ This value determined from sample failure population. 100% tested to this value in production.

⑦ When mounted on 1" square PCB (FR-4 or G-10 Material) . For recommended footprint and soldering techniques refer to application note #AN-994

⑧ $R_\theta$ is measured at $T_J$ approximately 90°C

Data and specifications subject to change without notice.
This product has been designed for the Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.9/04

Note:  For the most current drawings please refer to the IR website at:
http://www.irf.com/package/