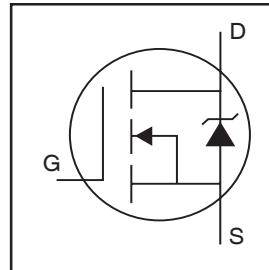


Features

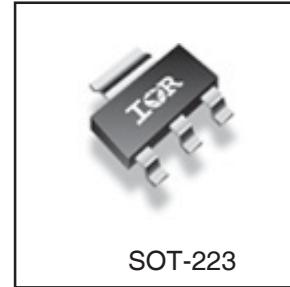
- Advanced Process Technology
- Ultra Low On-Resistance
- 150°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax



$V_{DSS} = 55V$
 $R_{DS(on)} = 57.5m\Omega$
 $I_D = 5.1A$

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 150°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



SOT-223

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited) ⑦	5.1	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ⑦	4.1	
I_{DM}	Pulsed Drain Current ①	41	
$P_D @ T_A = 25^\circ C$	Power Dissipation ⑦	2.8	
$P_D @ T_A = 25^\circ C$	Power Dissipation ⑧	1.0	W
	Linear Derating Factor ⑦	0.02	W/C
V_{GS}	Gate-to-Source Voltage	± 20	V
$E_{AS} (\text{Thermally limited})$	Single Pulse Avalanche Energy ②	13	mJ
$E_{AS} (\text{Tested})$	Single Pulse Avalanche Energy Tested Value ⑥	32	
I_{AR}	Avalanche Current ①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ
T_J	Operating Junction and	-55 to + 150	
T_{STG}	Storage Temperature Range		°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
R_{0JA}	Junction-to-Ambient (PCB mount, steady state) ⑦	—	45	°C/W
R_{0JA}	Junction-to-Ambient (PCB mount, steady state) ⑧	—	120	

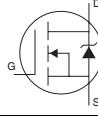
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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.053	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	46.2	57.5	$\text{m}\Omega$	$V_{\text{GS}} = 10\text{V}, I_D = 3.1\text{A}$ ③
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$
g_{fs}	Forward Transconductance	6.2	—	—	S	$V_{\text{DS}} = 25\text{V}, I_D = 3.1\text{A}$
I_{bss}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{\text{DS}} = 55\text{V}, V_{\text{GS}} = 0\text{V}$
		—	—	250		$V_{\text{DS}} = 55\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{\text{GS}} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{\text{GS}} = -20\text{V}$
Q_g	Total Gate Charge	—	9.1	14	nC	$I_D = 3.1\text{A}$
Q_{gs}	Gate-to-Source Charge	—	1.9	—		$V_{\text{DS}} = 44\text{V}$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	3.9	—		$V_{\text{GS}} = 10\text{V}$ ③
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	—	7.8	—	ns	$V_{\text{DD}} = 28\text{V}$
t_r	Rise Time	—	21	—		$I_D = 3.1\text{A}$
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time	—	30	—		$R_G = 53 \Omega$
t_f	Fall Time	—	23	—		$V_{\text{GS}} = 10\text{V}$ ③
C_{iss}	Input Capacitance	—	340	—	pF	$V_{\text{GS}} = 0\text{V}$
C_{oss}	Output Capacitance	—	68	—		$V_{\text{DS}} = 25\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	39	—		$f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	210	—		$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 1.0\text{V}, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	55	—		$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 44\text{V}, f = 1.0\text{MHz}$
$C_{\text{oss eff.}}$	Effective Output Capacitance	—	93	—		$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 0\text{V to } 44\text{V}$ ④

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	5.1	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	41		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 3.1\text{A}, V_{\text{GS}} = 0\text{V}$ ③
t_{rr}	Reverse Recovery Time	—	15	23	ns	$T_J = 25^\circ\text{C}, I_F = 3.1\text{A}, V_{\text{DD}} = 28\text{V}$
Q_{rr}	Reverse Recovery Charge	—	9.8	15	nC	$dI/dt = 100\text{A}/\mu\text{s}$ ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 2.8\text{mH}$ $R_G = 25\Omega$, $I_{AS} = 3.1\text{A}$, $V_{GS} = 10\text{V}$. Part not recommended for use above this value.
- ③ Pulse width $\leq 1.0\text{ms}$; duty cycle $\leq 2\%$.
- ④ $C_{\text{oss eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑤ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

⑥ This value determined from sample failure population. 100% tested to this value in production.

⑦ When mounted on 1 inch square copper board.

⑧ When mounted on FR-4 board using minimum recommended footprint.

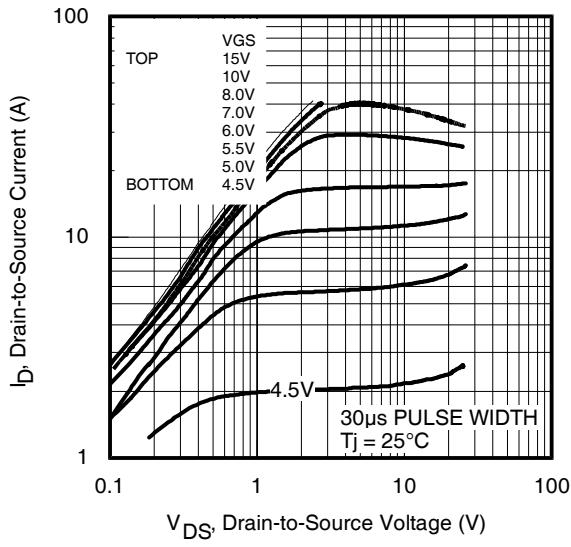


Fig 1. Typical Output Characteristics

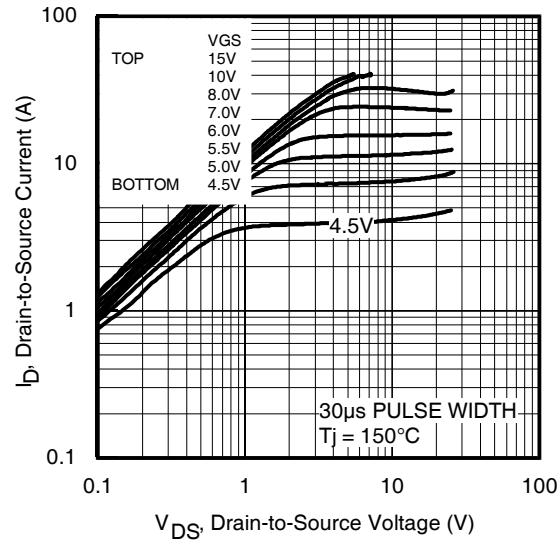


Fig 2. Typical Output Characteristics

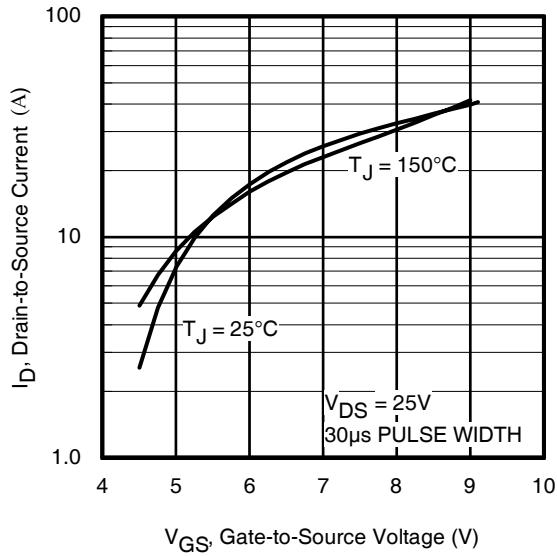


Fig 3. Typical Transfer Characteristics

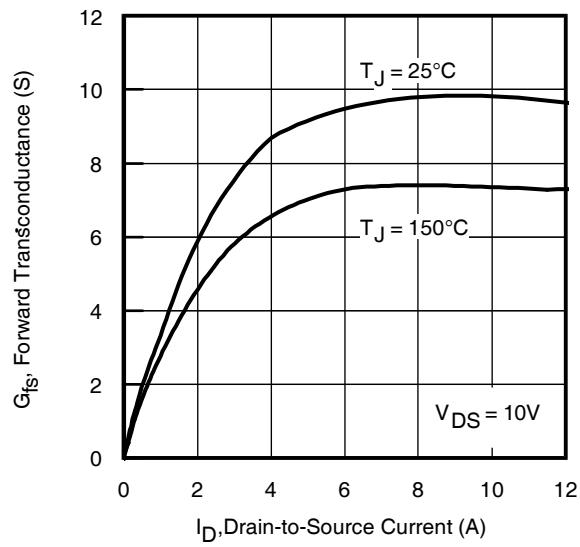


Fig 4. Typical Forward Transconductance vs. Drain Current

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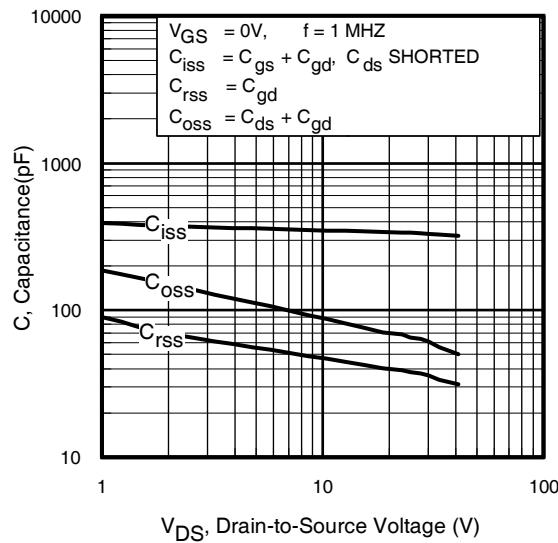


Fig 5. Typical Capacitance vs.
Drain-to-Source Voltage

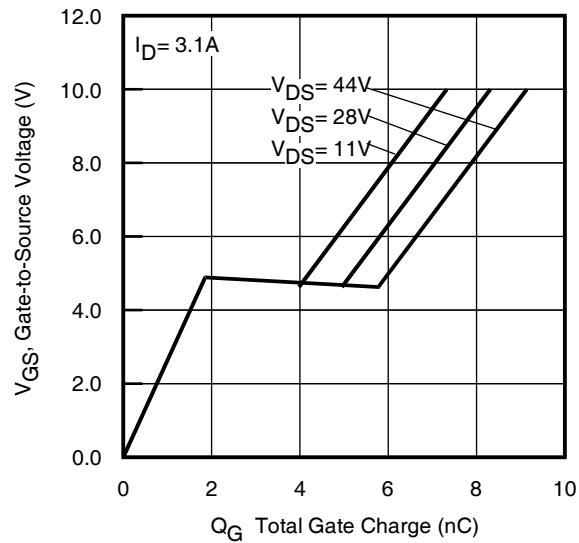


Fig 6. Typical Gate Charge vs.
Gate-to-Source Voltage

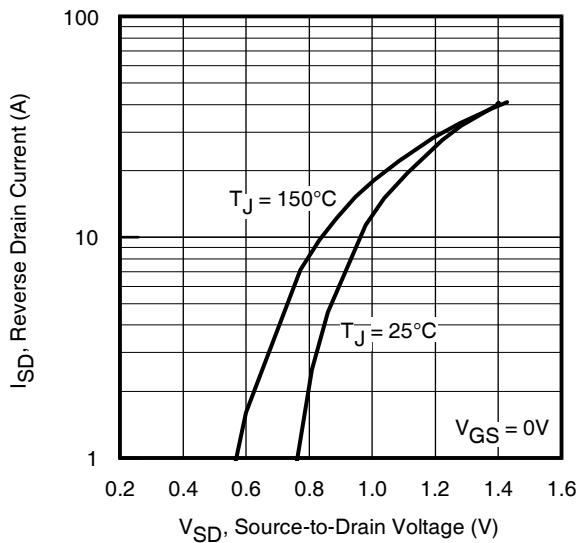


Fig 7. Typical Source-Drain Diode
Forward Voltage

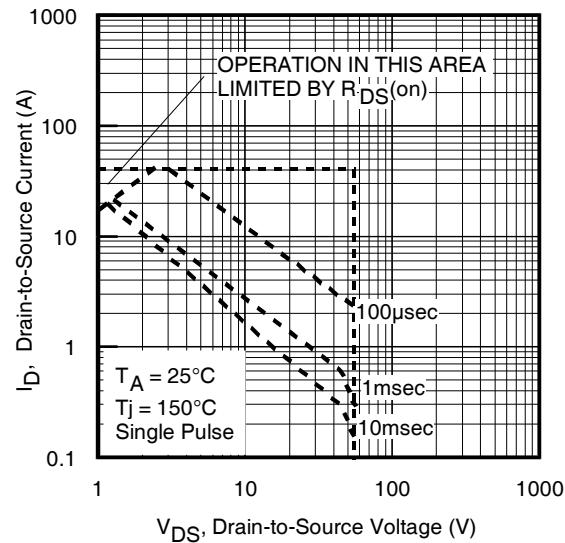


Fig 8. Maximum Safe Operating Area

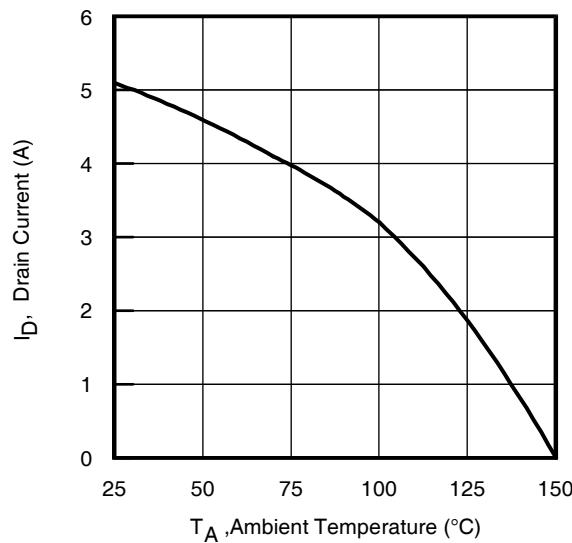


Fig 9. Maximum Drain Current vs.
Ambient Temperature

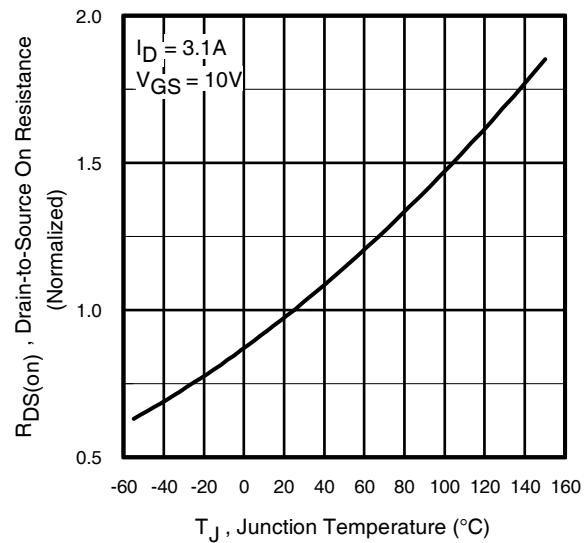


Fig 10. Normalized On-Resistance
vs. Temperature

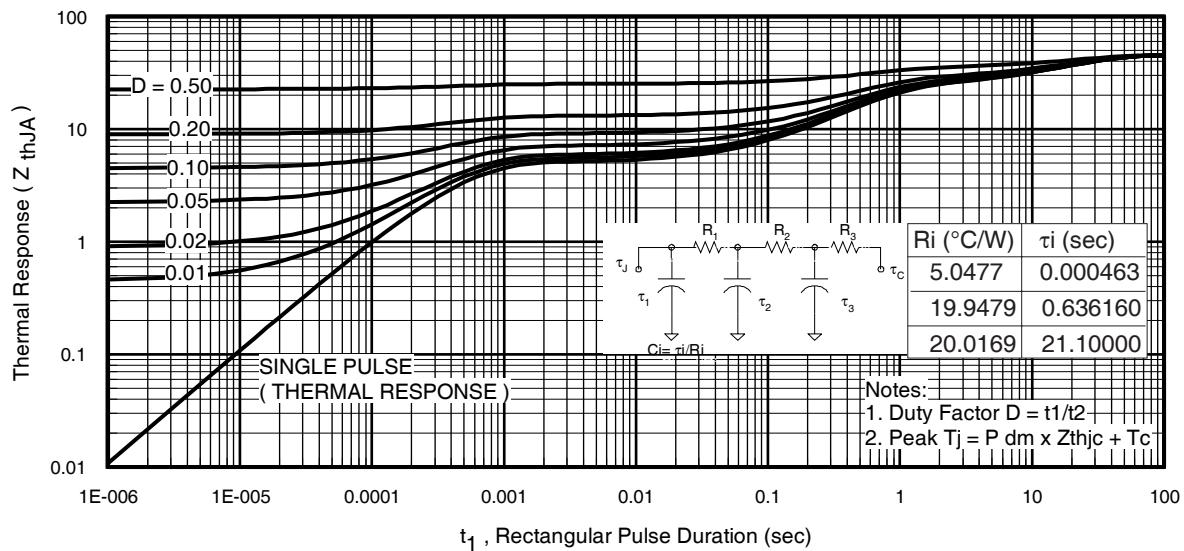


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

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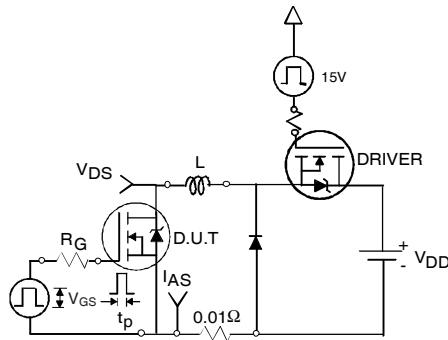


Fig 12a. Unclamped Inductive Test Circuit

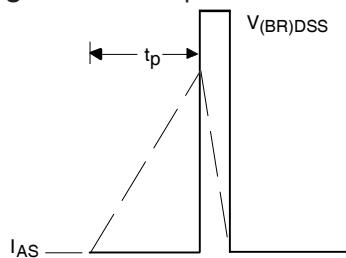


Fig 12b. Unclamped Inductive Waveforms

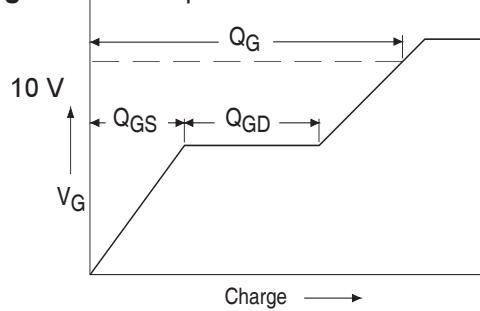


Fig 13a. Basic Gate Charge Waveform

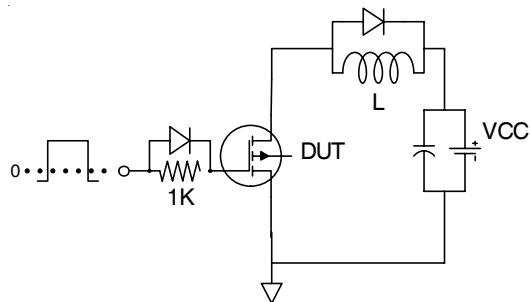


Fig 13b. Gate Charge Test Circuit

6

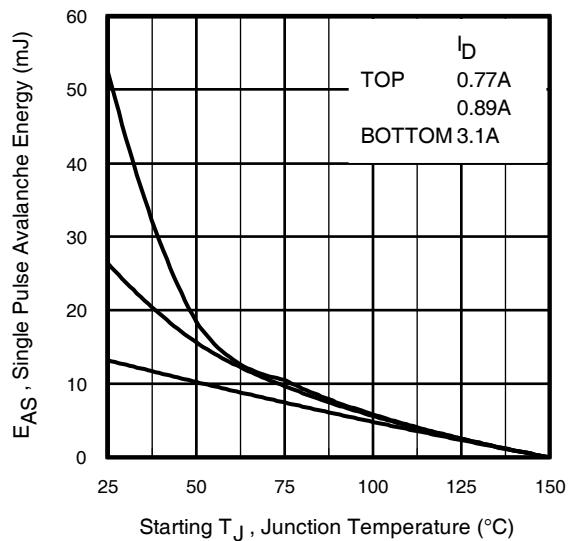


Fig 12c. Maximum Avalanche Energy vs. Drain Current

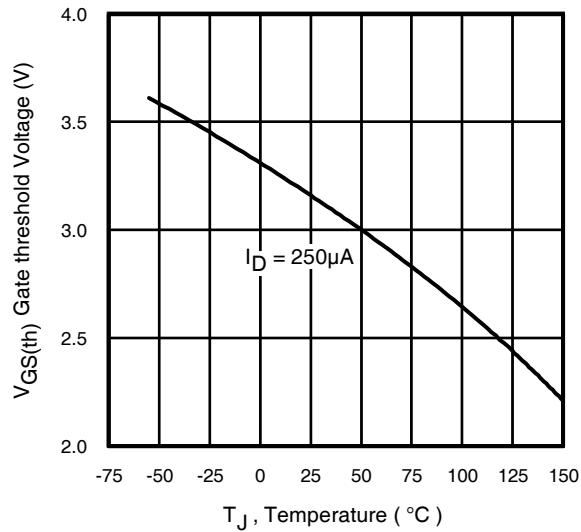


Fig 14. Threshold Voltage vs. Temperature

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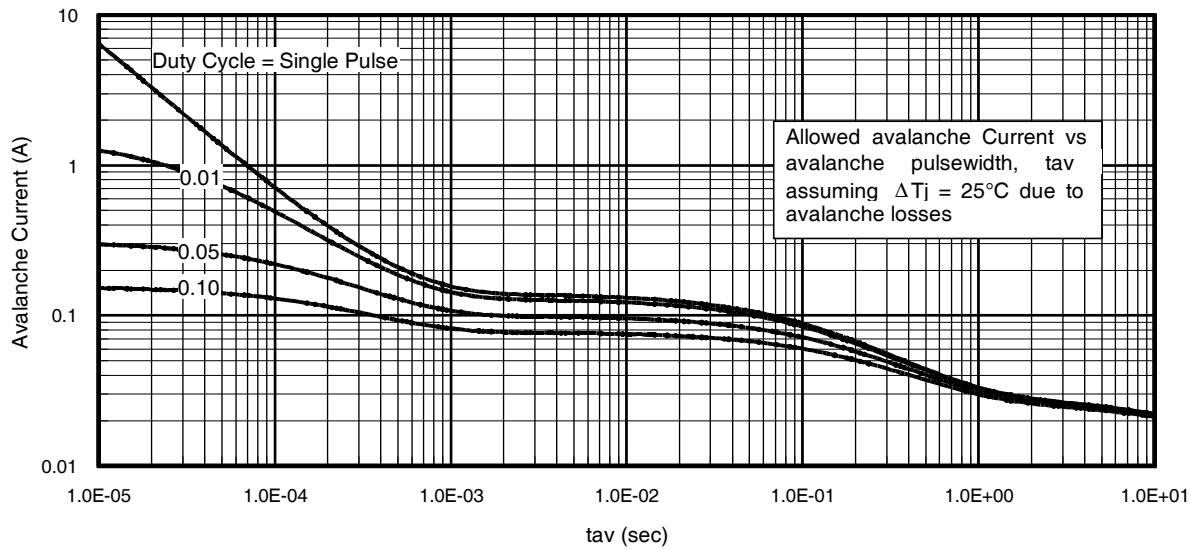


Fig 15. Typical Avalanche Current vs.Pulsewidth

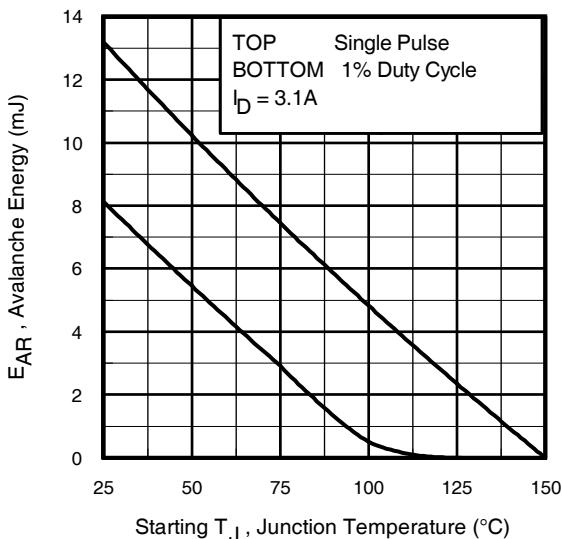


Fig 16. Maximum Avalanche Energy vs. Temperature

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**Notes on Repetitive Avalanche Curves , Figures 15, 16:
 (For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:
 Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

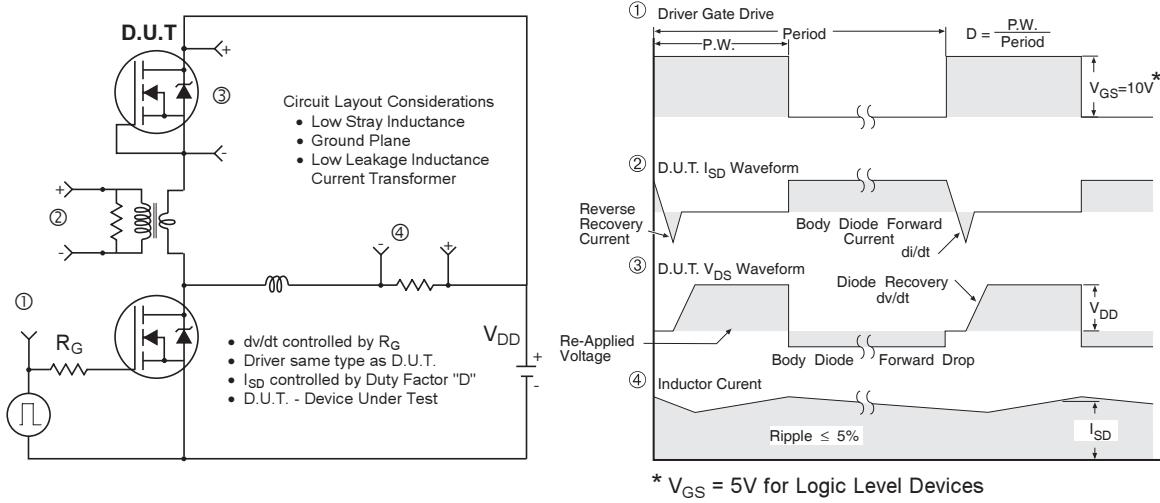


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

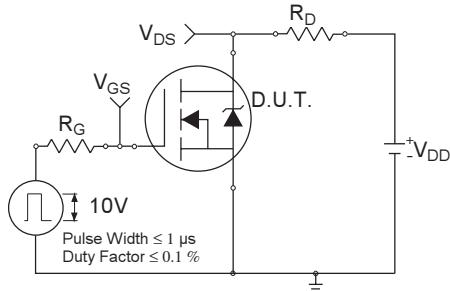


Fig 18a. Switching Time Test Circuit

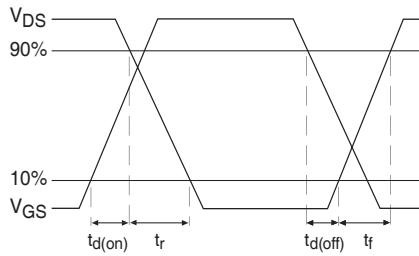
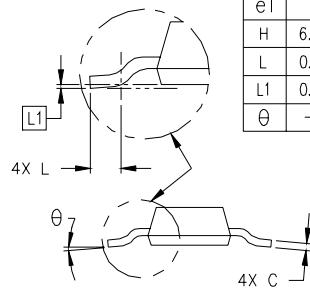
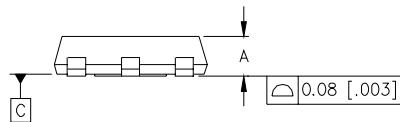
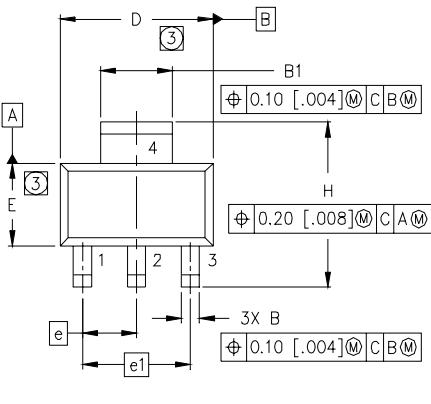


Fig 18b. Switching Time Waveforms

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SOT-223 (TO-261AA) Package Outline

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DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.55	1.80	.061	.071
B	0.65	0.85	.026	.033
B1	2.95	3.15	.116	.124
C	0.25	0.35	.010	.014
D	6.30	6.70	.248	.264
E	3.30	3.70	.130	.146
e	2.30	BSC	.0905	BSC
e1	4.60	BSC	.181	BSC
H	6.71	7.29	.264	.287
L	0.91	—	.036	—
L1	0.061	BSC	.0024	BSC
θ	—	10°	—	10°

LEAD ASSIGNMENTS

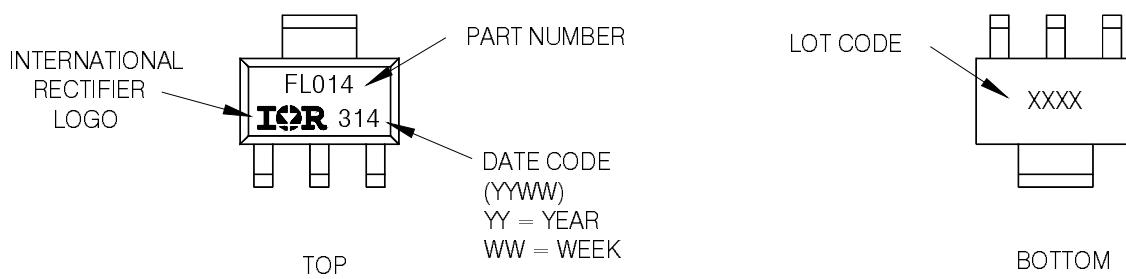
- 1 = GATE
- 2 = DRAIN
- 3 = SOURCE
- 4 = DRAIN

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS DO NOT INCLUDE MOLD FLASH.
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-261AA.
5. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

SOT-223 (TO-261AA) Part Marking Information

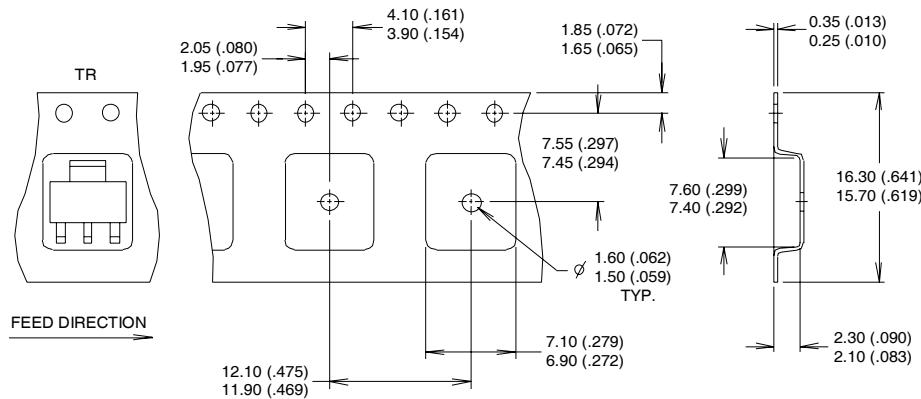
EXAMPLE: THIS IS AN IRFL014



IRFL024Z

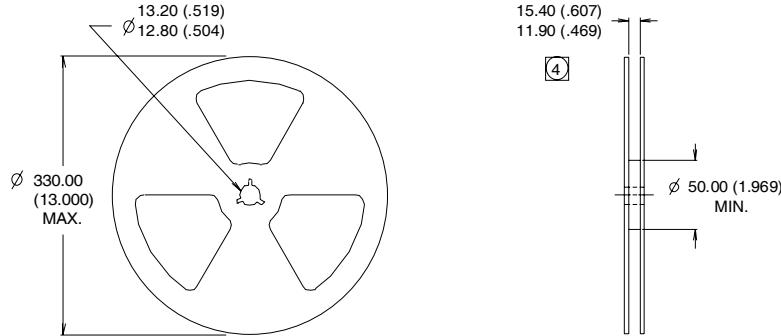
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SOT-223 (TO-261AA) Tape & Reel Information



NOTES :

1. CONTROLLING DIMENSION: MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.
3. EACH Ø330.00 (13.00) REEL CONTAINS 2,500 DEVICES.



NOTES :

1. OUTLINE CONFORMS TO EIA-418-1.
2. CONTROLLING DIMENSION: MILLIMETER..
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Data and specifications subject to change without notice.
This product has been designed for the Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

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Visit us at www.irf.com for sales contact information. 10/03