

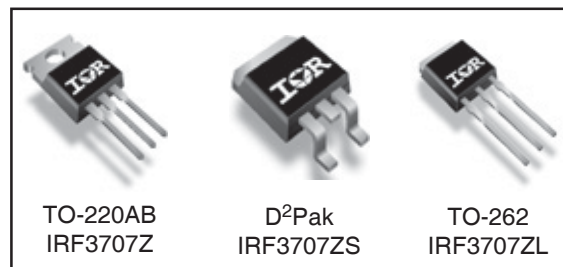
Applications

- High Frequency Synchronous Buck Converters for Computer Processor Power

V_{DSS}	R_{DS(on)} max	Qg
30V	9.5mΩ	9.7nC

Benefits

- Low R_{DS(on)} at 4.5V V_{GS}
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
V _{DS}	Drain-to-Source Voltage	30	V
V _{GS}	Gate-to-Source Voltage	± 20	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V ⑤	59⑦	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V ⑤	42⑦	
I _{DM}	Pulsed Drain Current ①	230	
P _D @ T _C = 25°C	Maximum Power Dissipation	57	W
P _D @ T _C = 100°C	Maximum Power Dissipation	28	
	Linear Derating Factor	0.38	W/°C
T _J	Operating Junction and Storage Temperature Range	-55 to + 175	°C
T _{STG}	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf·in (1.1 N·m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	2.653	°C/W
R _{θCS}	Case-to-Sink, Flat Greased Surface ③	0.50	—	
R _{θJA}	Junction-to-Ambient ③	—	62	
R _{θJA}	Junction-to-Ambient (PCB Mount) ④	—	40	

Notes ① through ⑦ are on page 12

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

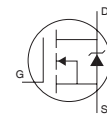
	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.023	—	mV/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	7.5	9.5	m Ω	$V_{GS} = 10V, I_D = 21A$ ③
		—	10	12.5		$V_{GS} = 4.5V, I_D = 17A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.35	1.80	2.25	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-5.3	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 24V, V_{GS} = 0V$
		—	—	150		$V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
g_{fs}	Forward Transconductance	81	—	—	S	$V_{DS} = 15V, I_D = 17A$
Q_g	Total Gate Charge	—	9.7	15	nC	$V_{DS} = 15V$ $V_{GS} = 4.5V$ $I_D = 17A$ See Fig. 16
Q_{gs1}	Pre-V _{th} Gate-to-Source Charge	—	2.8	—		
Q_{gs2}	Post-V _{th} Gate-to-Source Charge	—	1.0	—		
Q_{gd}	Gate-to-Drain Charge	—	3.4	—		
Q_{godr}	Gate Charge Overdrive	—	2.5	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	4.4	—		
Q_{oss}	Output Charge	—	6.2	—	nC	$V_{DS} = 16V, V_{GS} = 0V$
$t_{d(on)}$	Turn-On Delay Time	—	9.8	—	ns	$V_{DD} = 15V, V_{GS} = 4.5V$ ③ $I_D = 17A$ Clamped Inductive Load
t_r	Rise Time	—	41	—		
$t_{d(off)}$	Turn-Off Delay Time	—	12	—		
t_f	Fall Time	—	3.6	—		
C_{iss}	Input Capacitance	—	1210	—	pF	$V_{GS} = 0V$ $V_{DS} = 15V$ $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	260	—		
C_{rss}	Reverse Transfer Capacitance	—	130	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	40	mJ
I_{AR}	Avalanche Current ①	—	23	A
E_{AR}	Repetitive Avalanche Energy ①	—	5.7	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	59 ⑦	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	230		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	$T_J = 25^\circ\text{C}, I_S = 17A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	14	21	ns	$T_J = 25^\circ\text{C}, I_F = 17A, V_{DD} = 15V$
Q_{rr}	Reverse Recovery Charge	—	5.2	7.8	nC	$di/dt = 100A/\mu s$ ③



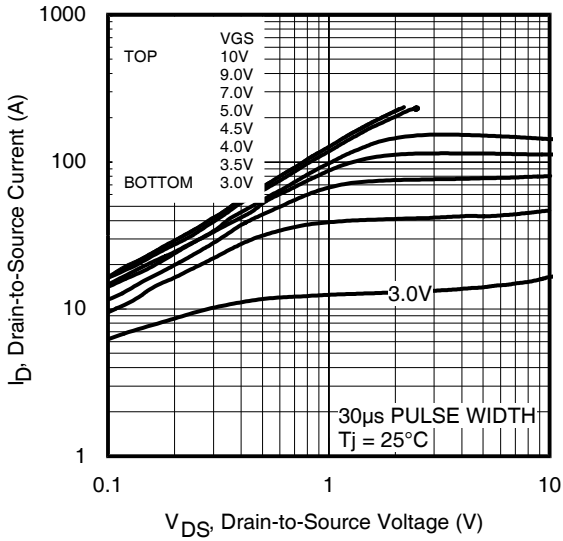


Fig 1. Typical Output Characteristics

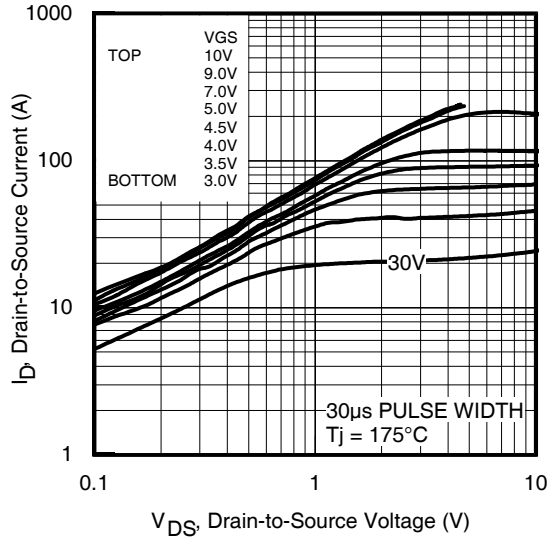


Fig 2. Typical Output Characteristics

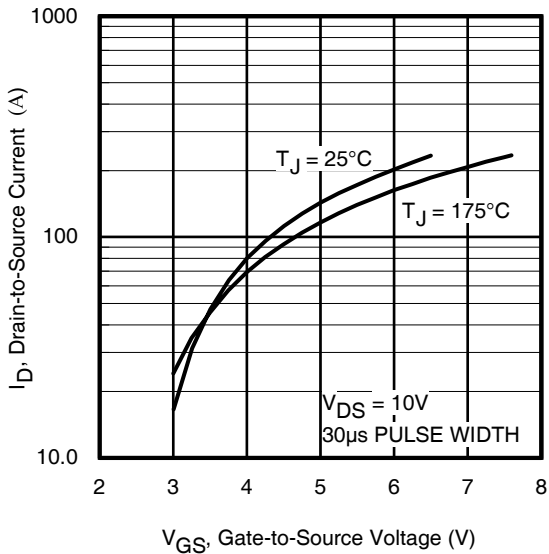


Fig 3. Typical Transfer Characteristics

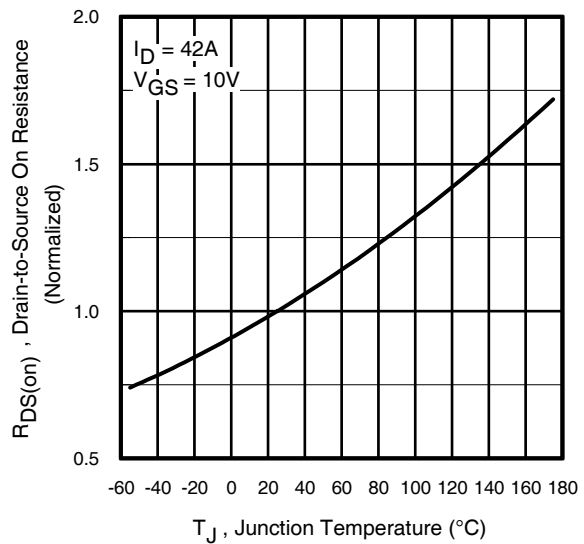


Fig 4. Normalized On-Resistance vs. Temperature

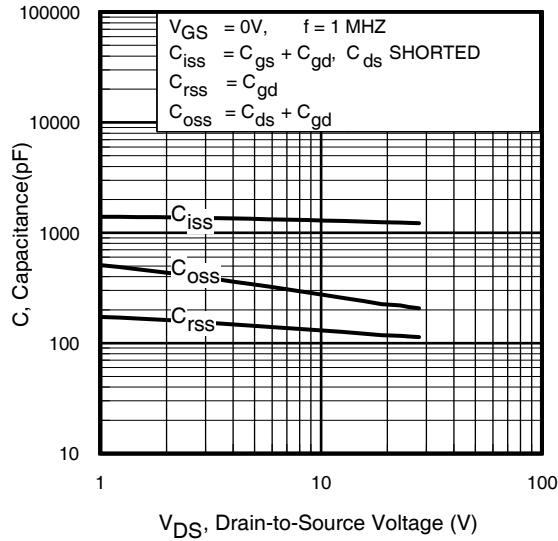


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

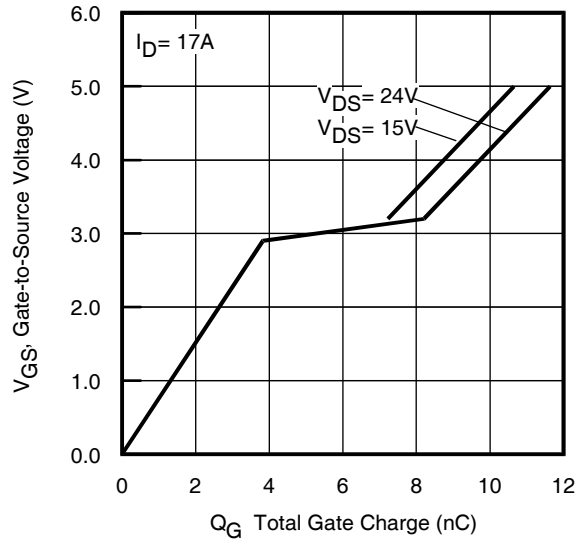


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

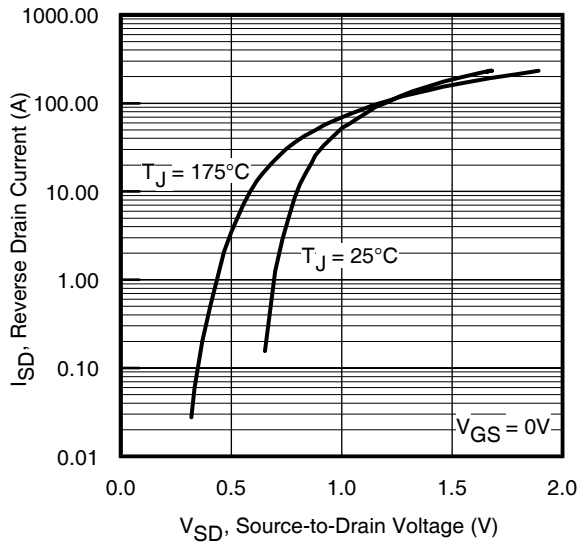


Fig 7. Typical Source-Drain Diode Forward Voltage

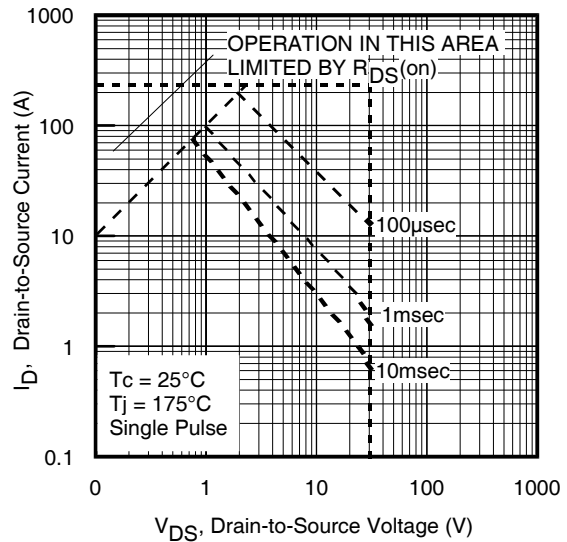


Fig 8. Maximum Safe Operating Area

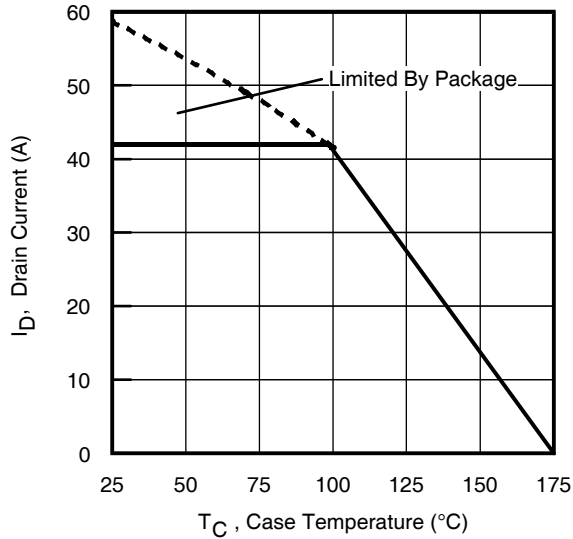


Fig 9. Maximum Drain Current vs. Case Temperature

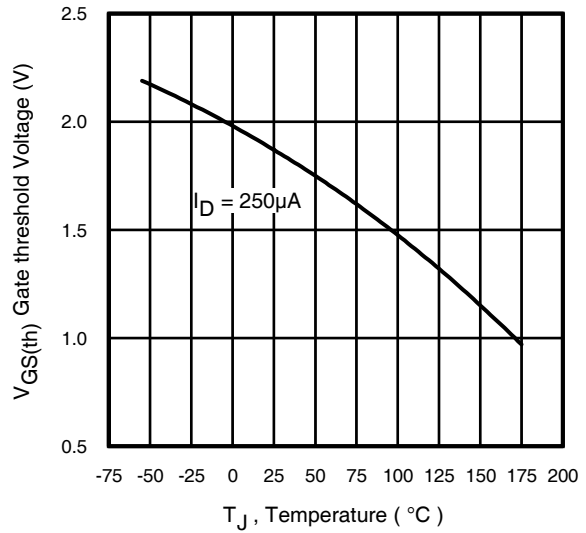


Fig 10. Threshold Voltage vs. Temperature

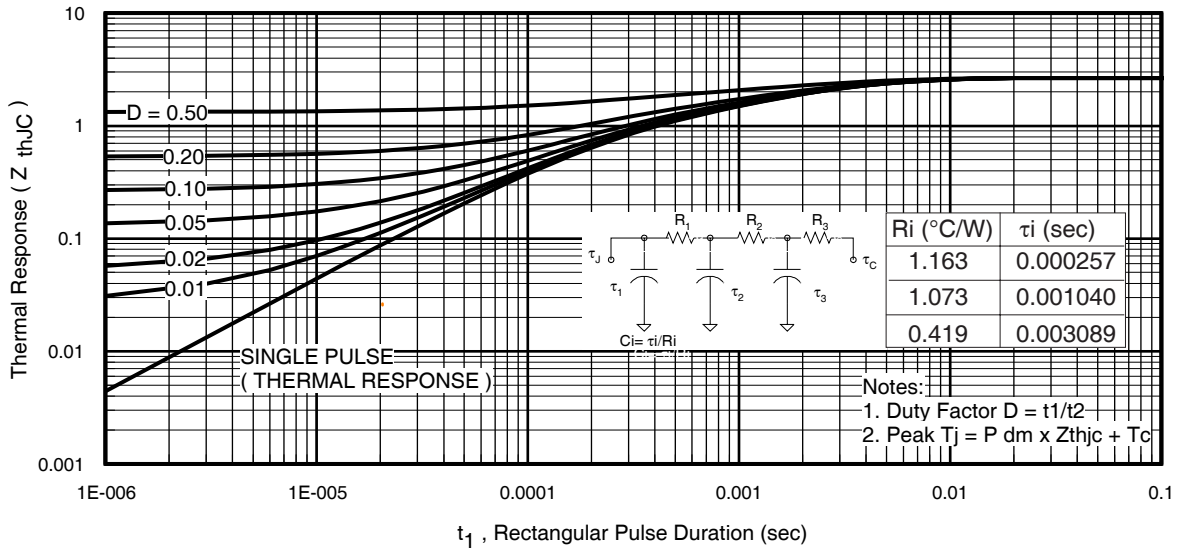


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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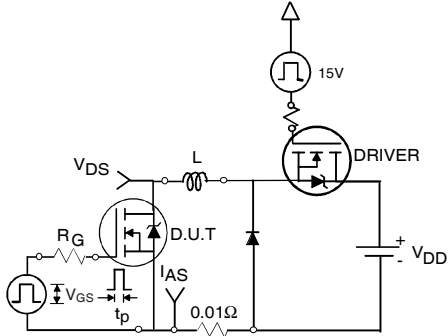


Fig 12a. Unclamped Inductive Test Circuit

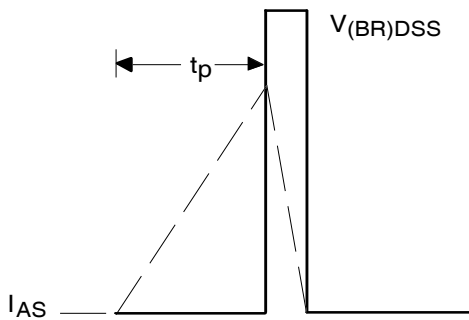


Fig 12b. Unclamped Inductive Waveforms

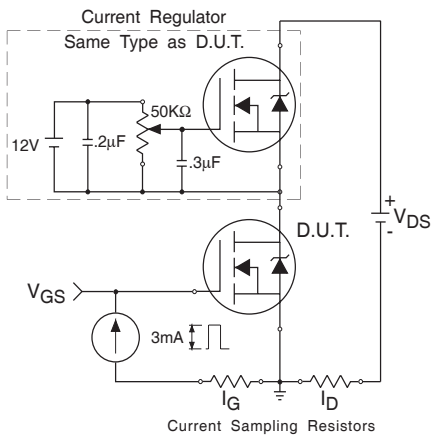


Fig 13. Gate Charge Test Circuit

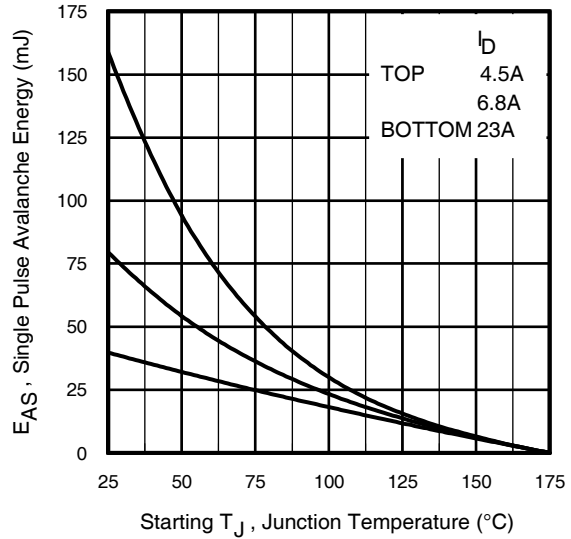


Fig 12c. Maximum Avalanche Energy vs. Drain Current

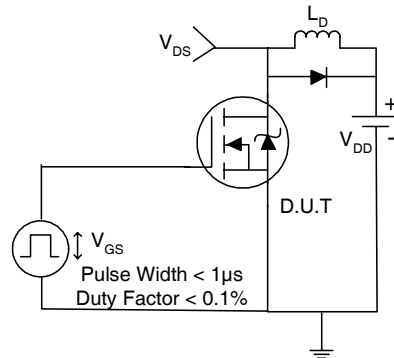


Fig 14a. Switching Time Test Circuit

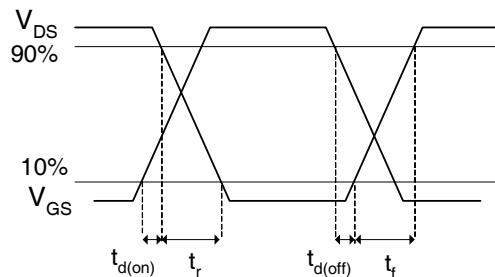


Fig 14b. Switching Time Waveforms

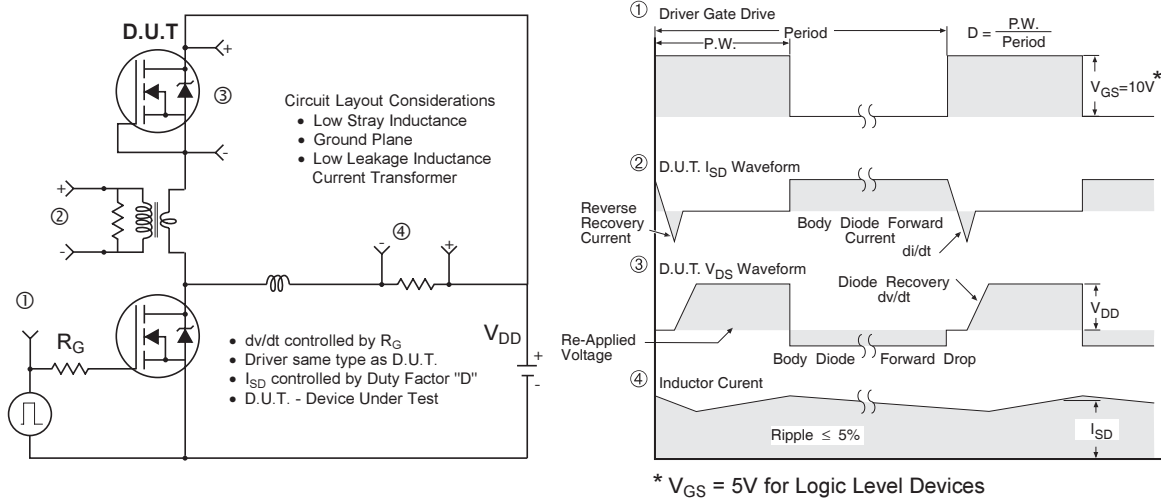


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET[®] Power MOSFETs

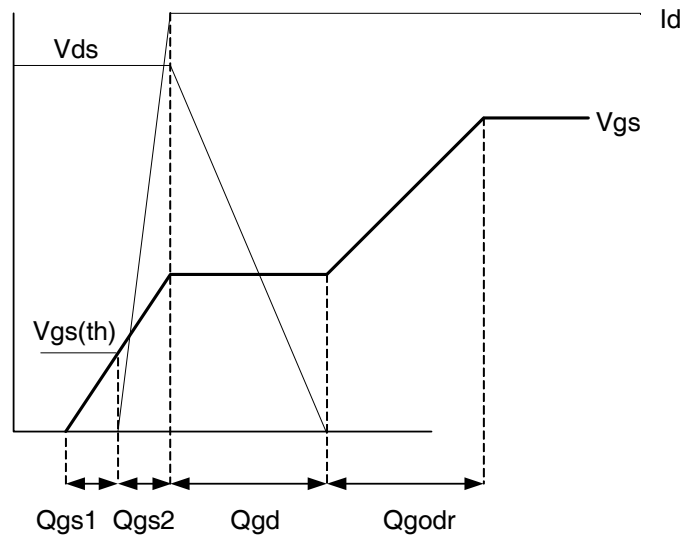


Fig 16. Gate Charge Waveform

Power MOSFET Selection for Non-Isolated DC/DC Converters

Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = \left(I_{rms}^2 \times R_{ds(on)} \right) + \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f \right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f \right) + \left(Q_g \times V_g \times f \right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f \right)$$

This simplified loss equation includes the terms Q_{gs2} and Q_{oss} which are new to Power MOSFET data sheets.

Q_{gs2} is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, Q_{gs1} and Q_{gs2} , can be seen from Fig 16.

Q_{gs2} indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to I_{dmax} at which time the drain voltage begins to change. Minimizing Q_{gs2} is a critical factor in reducing switching losses in Q1.

Q_{oss} is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how Q_{oss} is formed by the parallel combination of the voltage dependant (non-linear) capacitance's C_{ds} and C_{dg} when multiplied by the power supply input buss voltage.

Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P_{output}^*$$

$$P_{loss} = \left(I_{rms}^2 \times R_{ds(on)} \right) + \left(Q_g \times V_g \times f \right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f \right) + \left(Q_{rr} \times V_{in} \times f \right)$$

*dissipated primarily in Q1.

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge Q_{oss} and reverse recovery charge Q_{rr} both generate losses that are transferred to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and V_{in} . As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current. The ratio of Q_{gd}/Q_{gs1} must be minimized to reduce the potential for Cdv/dt turn on.

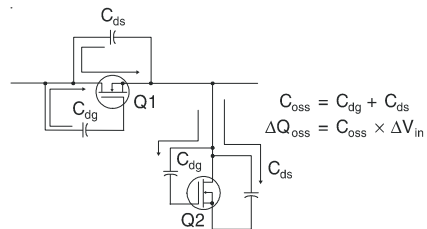
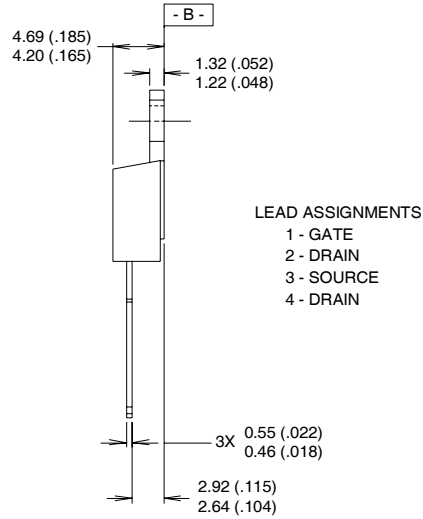
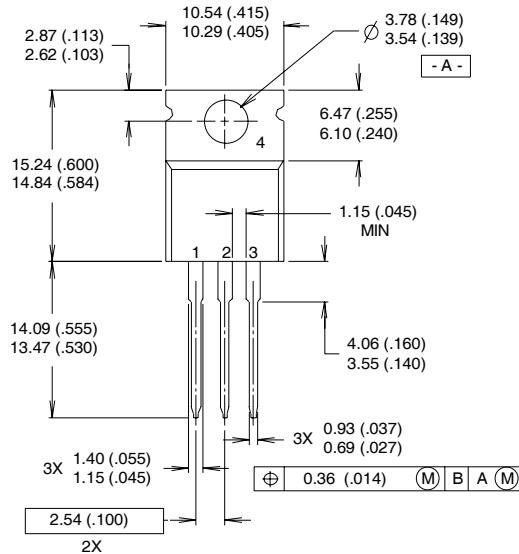


Figure A: Q_{oss} Characteristic

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

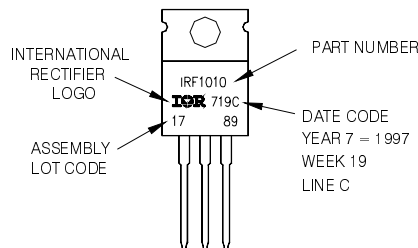


NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

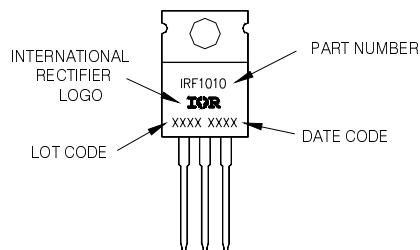
TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE 'C'



For GB Production

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 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE 'C'

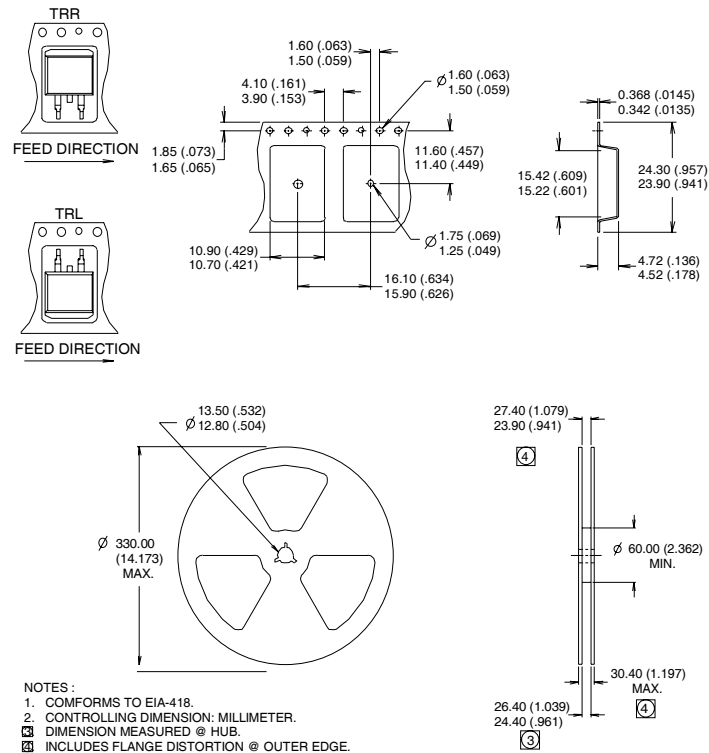


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D²Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.15\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 23\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑤ This is only applied to TO-220AB package.
- ⑥ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑦ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 42A.

TO-220AB package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>