

**Applications**

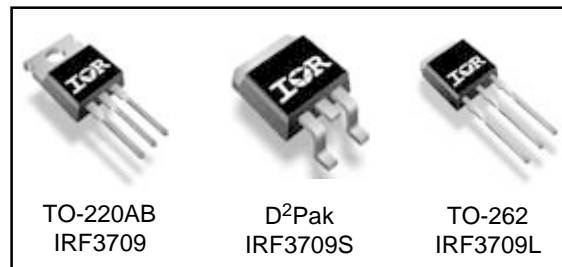
- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use
- High Frequency Buck Converters for Server Processor Power Synchronous FET
- Optimized for Synchronous Buck Converters Including Capacitive Induced Turn-on Immunity

**Benefits**

- Ultra-Low Gate Impedance
- Very Low RDS(on) at 4.5V V<sub>GS</sub>
- Fully Characterized Avalanche Voltage and Current

HEXFET® Power MOSFET

<b>V<sub>DSS</sub></b>	<b>R<sub>DS(on)</sub> max</b>	<b>I<sub>D</sub></b>
<b>30V</b>	<b>9.0mΩ</b>	<b>90A<sup>Ⓔ</sup></b>



**Absolute Maximum Ratings**

Symbol	Parameter	Max.	Units
V <sub>DS</sub>	Drain-Source Voltage	30	V
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	90 <sup>Ⓔ</sup>	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	57	
I <sub>DM</sub>	Pulsed Drain Current <sup>Ⓓ</sup>	360	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation <sup>ⓓ</sup>	120	W
P <sub>D</sub> @ T <sub>A</sub> = 25°C	Maximum Power Dissipation <sup>ⓔ</sup>	3.1	W
	Linear Derating Factor	0.96	mW/°C
T <sub>J</sub> , T <sub>STG</sub>	Junction and Storage Temperature Range	-55 to + 150	°C

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case	—	1.04	°C/W
R <sub>θCS</sub>	Case-to-Sink, Flat, Greased Surface <sup>Ⓓ</sup>	0.50	—	
R <sub>θJA</sub>	Junction-to-Ambient <sup>Ⓓ</sup>	—	62	
R <sub>θJA</sub>	Junction-to-Ambient (PCB mount) <sup>ⓔ</sup>	—	40	

Notes <sup>Ⓓ</sup> through <sup>Ⓔ</sup> are on page 11

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# IRF3709/3709S/3709L

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## Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.029	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	6.4	9.0	mΩ	$V_{GS} = 10V, I_D = 15A$ ③
		—	7.4	10.5		$V_{GS} = 4.5V, I_D = 12A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	3.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 24V, V_{GS} = 0V$
		—	—	100		$V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -16V$

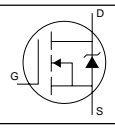
## Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	53	—	—	S	$V_{DS} = 15V, I_D = 30A$
$Q_g$	Total Gate Charge	—	27	41	nC	$I_D = 15A$
$Q_{gs}$	Gate-to-Source Charge	—	6.7	—		$V_{DS} = 16V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	9.7	—		$V_{GS} = 5.0V$ ③
$Q_{oss}$	Output Gate Charge	—	22	—		$V_{GS} = 0V, V_{DS} = 10V$
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	$V_{DD} = 15V$
$t_r$	Rise Time	—	171	—		$I_D = 30A$
$t_{d(off)}$	Turn-Off Delay Time	—	21	—		$R_G = 1.8\Omega$
$t_f$	Fall Time	—	9.2	—		$V_{GS} = 4.5V$ ③
$C_{iss}$	Input Capacitance	—	2672	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	1064	—		$V_{DS} = 16V$
$C_{rss}$	Reverse Transfer Capacitance	—	109	—		$f = 1.0MHz$

## Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy②	—	382	mJ
$I_{AR}$	Avalanche Current①	—	30	A

## Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	90⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	360		
$V_{SD}$	Diode Forward Voltage	—	0.88	1.3	V	$T_J = 25^\circ\text{C}, I_S = 30A, V_{GS} = 0V$ ③
		—	0.82	—		$T_J = 125^\circ\text{C}, I_S = 30A, V_{GS} = 0V$ ③
$t_{rr}$	Reverse Recovery Time	—	48	72	ns	$T_J = 25^\circ\text{C}, I_F = 30A, V_R = 15V$
$Q_{rr}$	Reverse Recovery Charge	—	46	69	nC	$di/dt = 100A/\mu s$ ③
$t_{rr}$	Reverse Recovery Time	—	48	72	ns	$T_J = 125^\circ\text{C}, I_F = 30A, V_R = 15V$
$Q_{rr}$	Reverse Recovery Charge	—	52	78	nC	$di/dt = 100A/\mu s$ ③

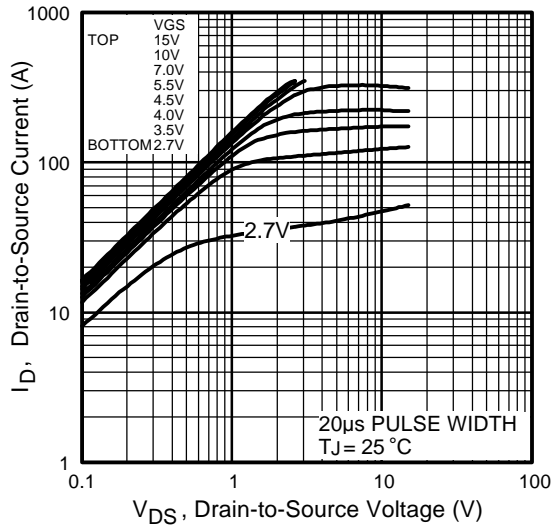


Fig 1. Typical Output Characteristics

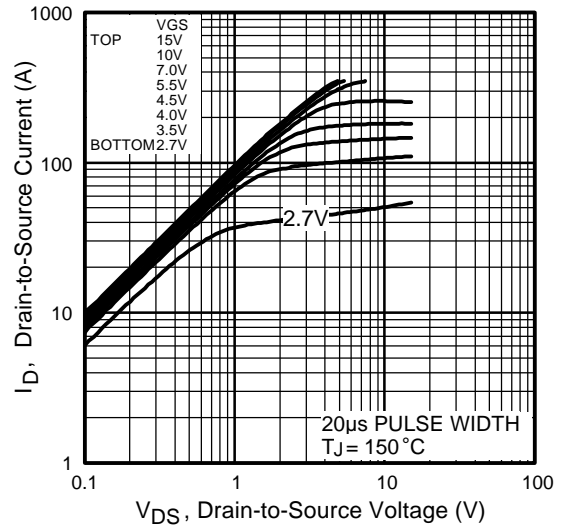


Fig 2. Typical Output Characteristics

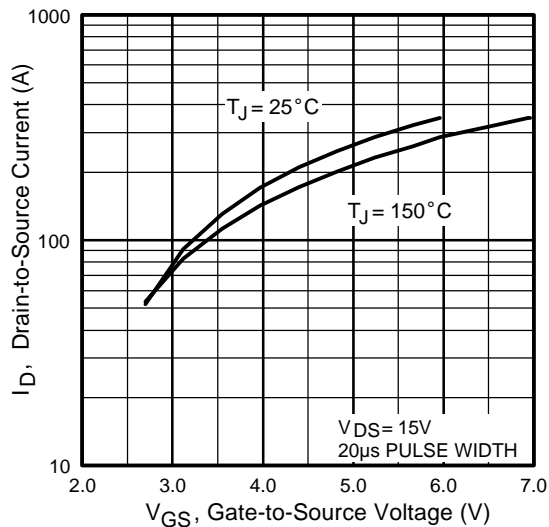


Fig 3. Typical Transfer Characteristics

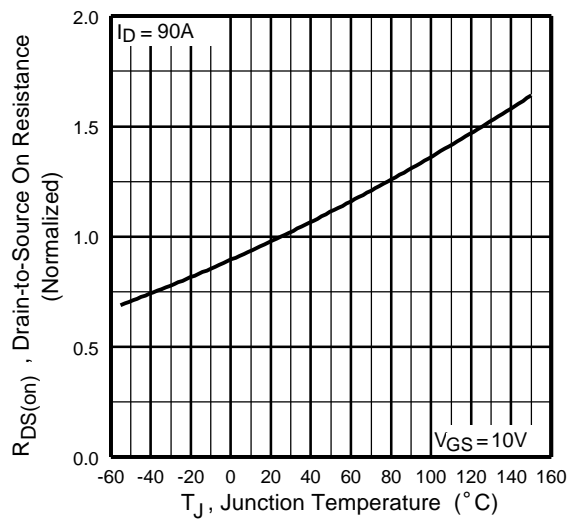
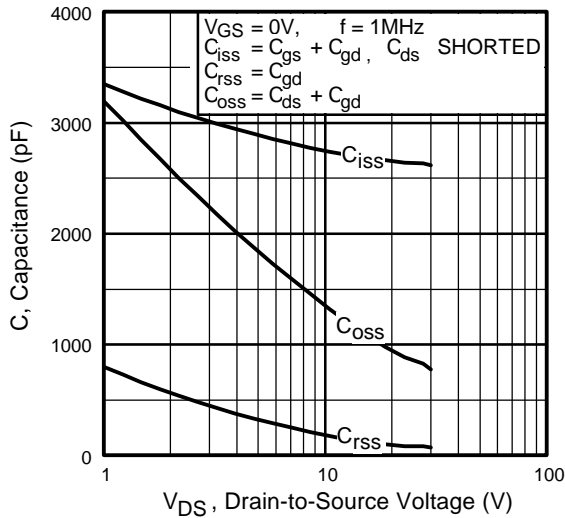
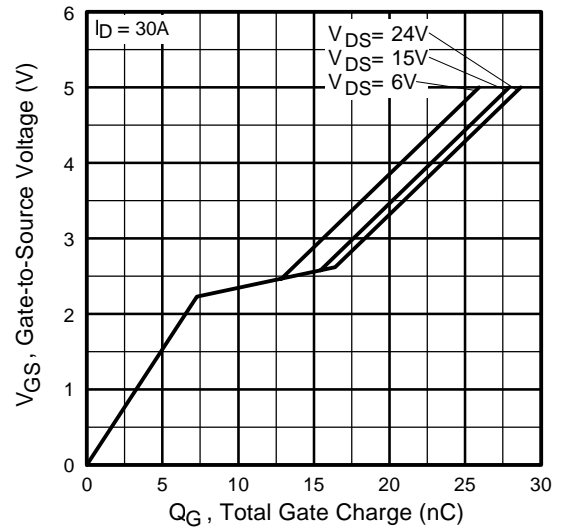


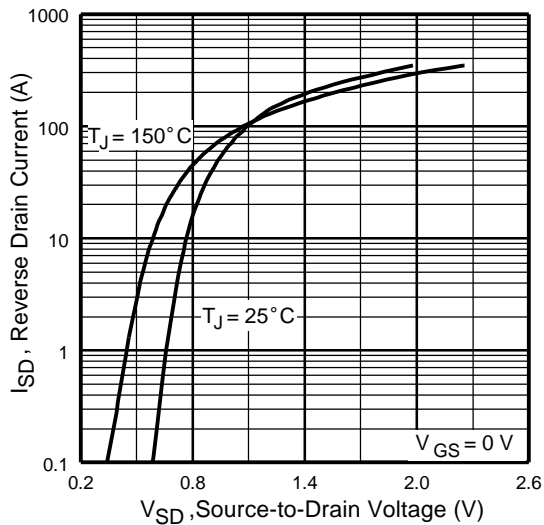
Fig 4. Normalized On-Resistance Vs. Temperature



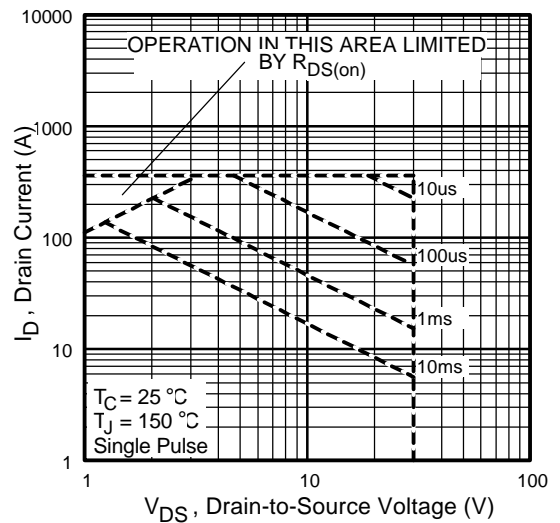
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area

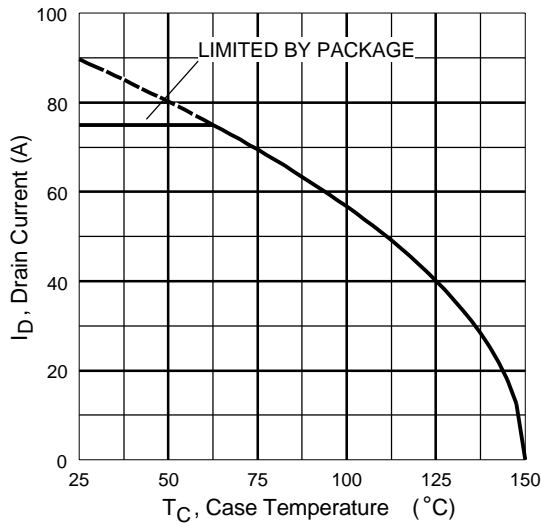


Fig 9. Maximum Drain Current Vs. Case Temperature

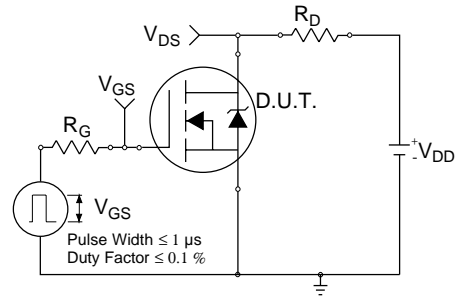


Fig 10a. Switching Time Test Circuit

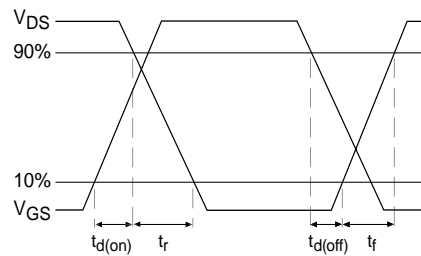


Fig 10b. Switching Time Waveforms

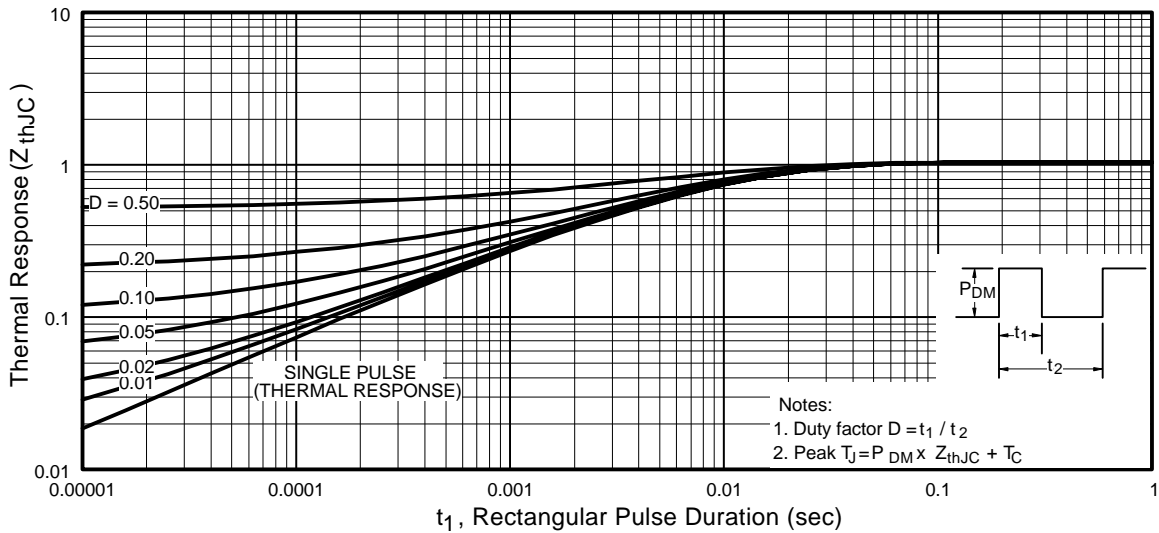
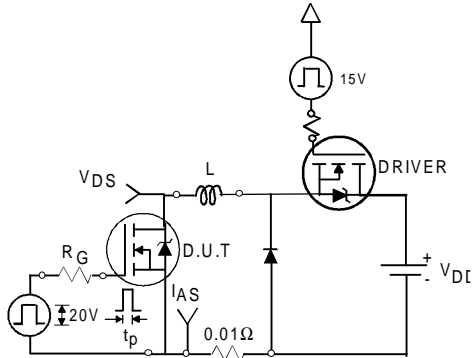


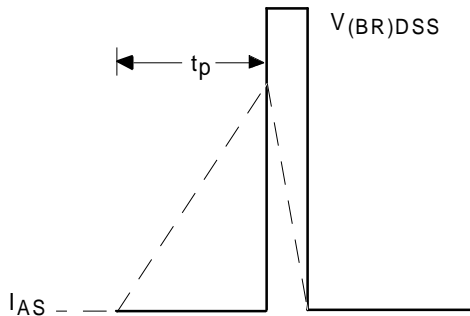
Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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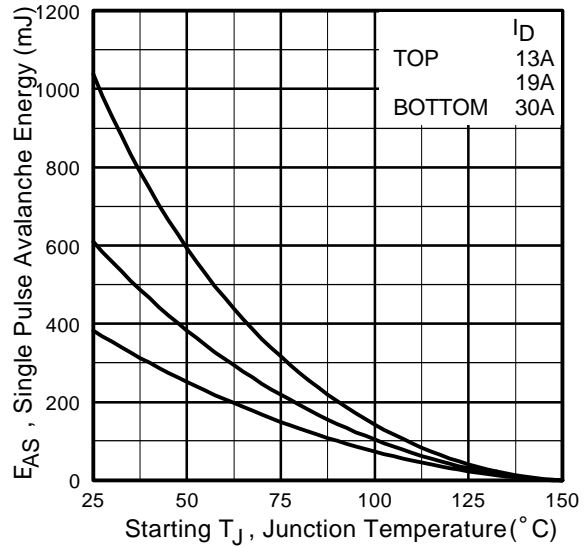
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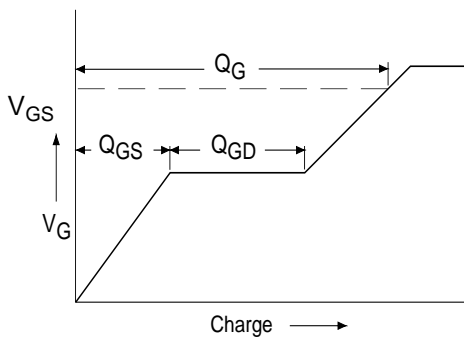
**Fig 12a.** Unclamped Inductive Test Circuit



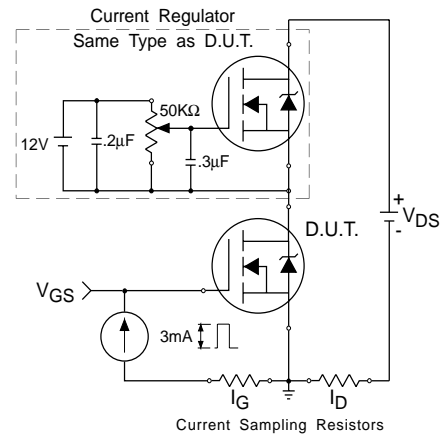
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

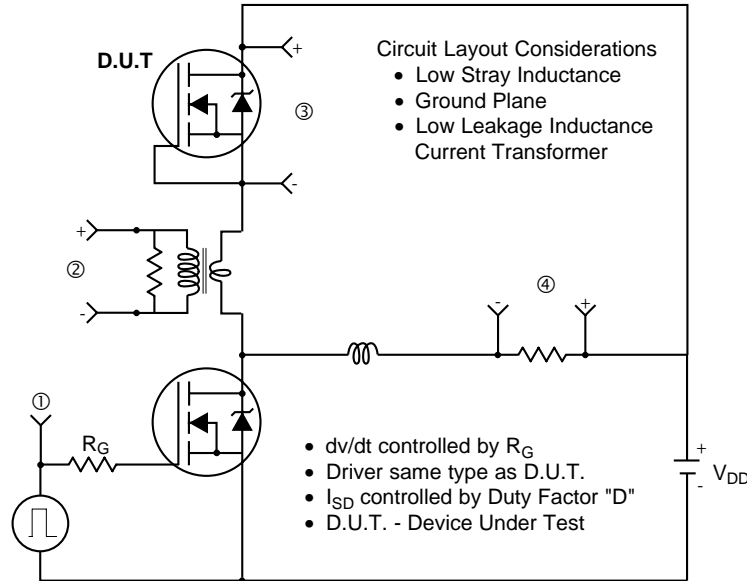


**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

**Peak Diode Recovery dv/dt Test Circuit**



\*  $V_{GS} = 5V$  for Logic Level Devices

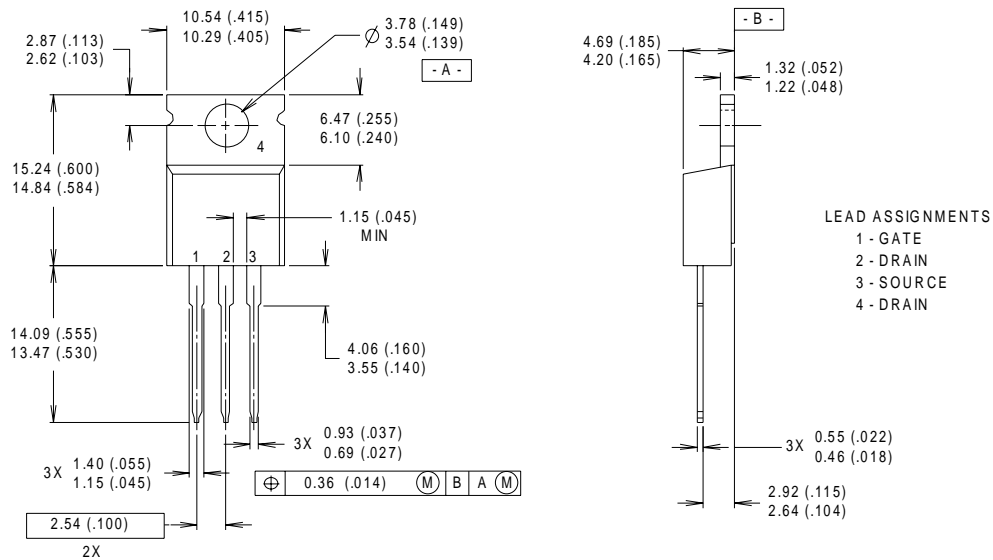
**Fig 14.** For N-Channel HEXFET® Power MOSFETs

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## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

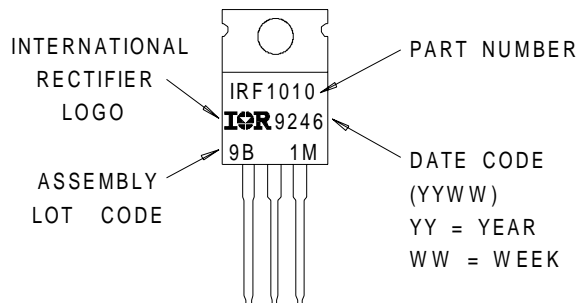


**NOTES:**

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

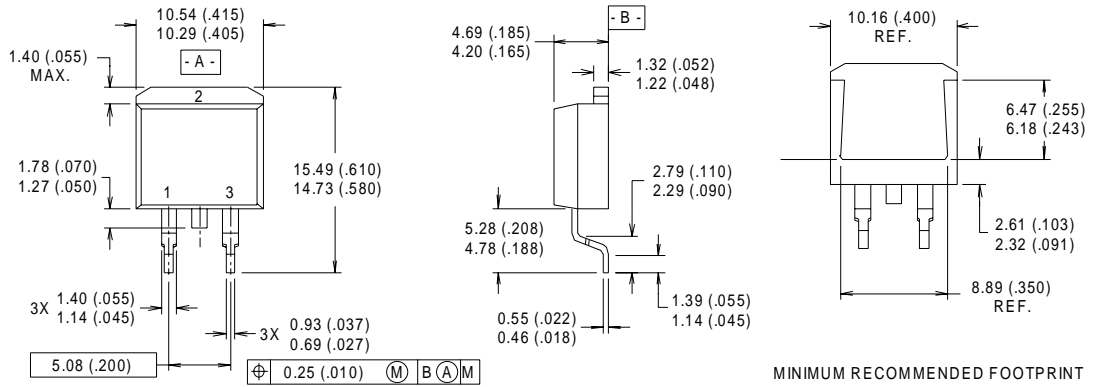
## TO-220AB Part Marking Information

EXAMPLE : THIS IS AN IRF1010  
WITH ASSEMBLY  
LOT CODE 9B1M





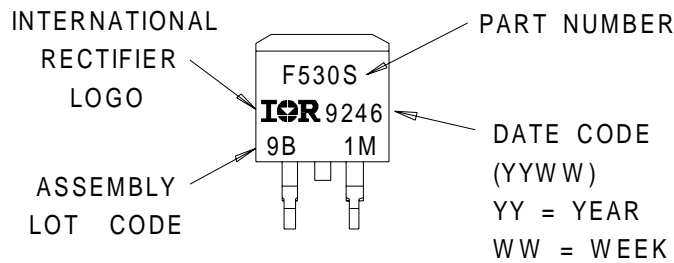
D<sup>2</sup>Pak Package Outline



- NOTES:
- 1 DIMENSIONS AFTER SOLDER DIP.
  - 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
  - 3 CONTROLLING DIMENSION : INCH.
  - 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

- LEAD ASSIGNMENTS
- 1 - GATE
  - 2 - DRAIN
  - 3 - SOURCE

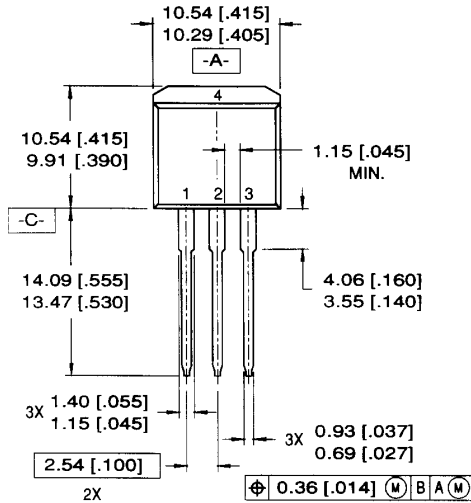
D<sup>2</sup>Pak Part Marking Information



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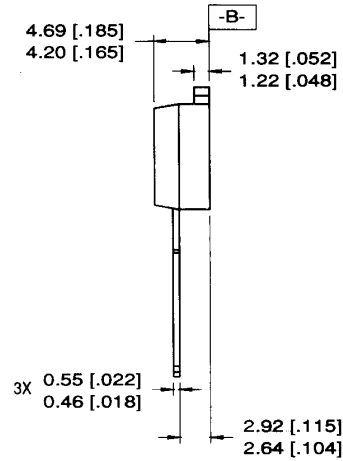
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## TO-262 Package Outline



**LEAD ASSIGNMENTS**

1 = GATE      3 = SOURCE  
2 = DRAIN    4 = DRAIN

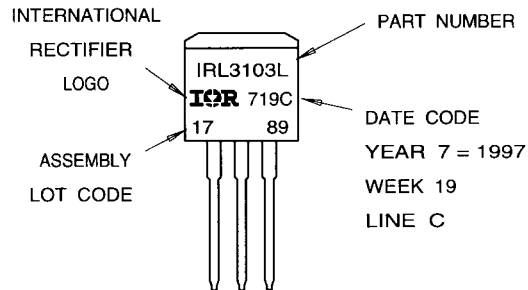


**NOTES:**

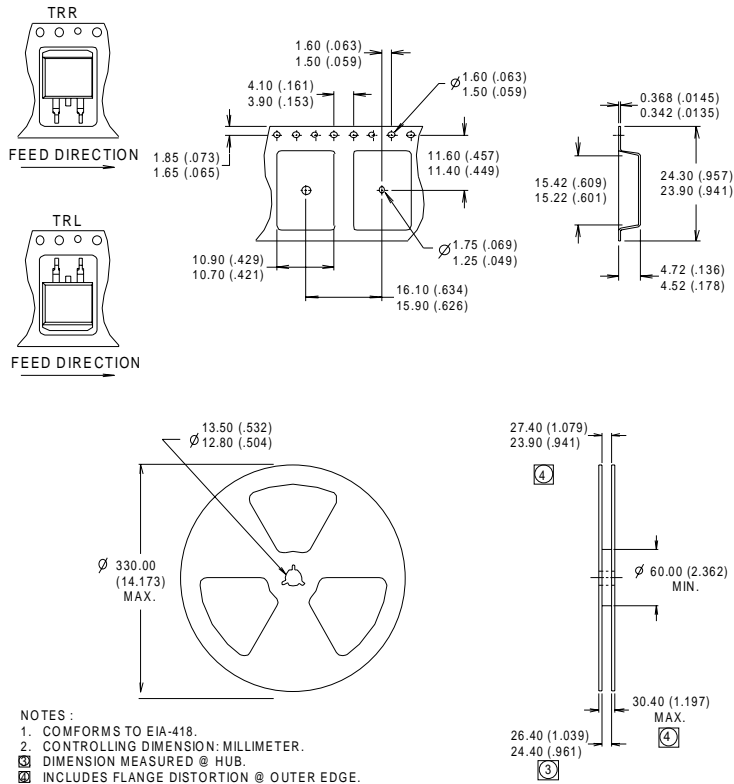
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
LOT CODE 1789  
ASSEMBLED ON WW 19, 1997  
IN THE ASSEMBLY LINE "C"



D<sup>2</sup>Pak Tape & Reel Information



**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.85\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 30\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④ This is only applied to TO-220AB package
- ⑤ This is applied to D<sup>2</sup>Pak, when mounted on 1" square PCB ( FR-4 or G-10 Material ).  
 For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

Data and specifications subject to change without notice.  
 This product has been designed and qualified for the industrial market.  
 Qualification Standards can be found on IR's Web site.

Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>