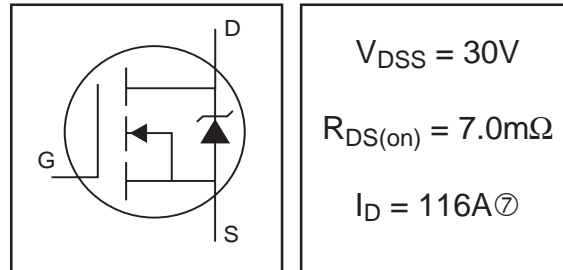


IRL2203NS
IRL2203NL

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- 100% R_G Tested

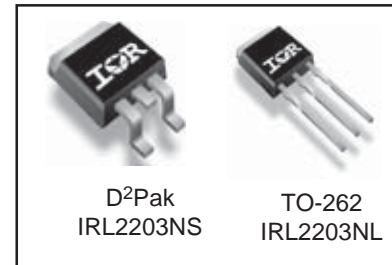
HEXFET[®] Power MOSFET



Description

Advanced HEXFET[®] Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application. The through-hole version (IRL2203NL) is available for low-profile applications.



Absolute Maximum Ratings

Symbol	Parameter	Max	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	116 ⑦	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	82	
I_{DM}	Pulsed Drain Current ①	400	
$P_D @ T_A = 25^\circ C$	Power Dissipation	3.8	W
$P_D @ T_C = 25^\circ C$	Power Dissipation	180	W
	Linear Derating Factor	1.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
I_{AR}	Avalanche Current ①	60	A
E_{AR}	Repetitive Avalanche Energy ①	18	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and Storage Temperature Range	-55 to + 175	°C
T_{STG}	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Junction-to-Case ②	—	0.85	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount, steady state) ②③	—	40	

IRL2203NS/L

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

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Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.029	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	7.0		$V_{GS} = 10V, I_D = 60A$ ④
		—	—	10		$V_{GS} = 4.5V, I_D = 48A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	3.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	73	—	—	S	$V_{DS} = 25V, I_D = 60A$ ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 30V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
Q_g	Total Gate Charge	—	—	60	nC	$I_D = 60A$
Q_{gs}	Gate-to-Source Charge	—	—	14		$V_{DS} = 24V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	33		$V_{GS} = 4.5V$, See Fig. 6 and 13
R_G	Gate Resistance	0.2	—	3.0	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	11	—		$V_{DD} = 15V$
t_r	Rise Time	—	160	—		$I_D = 60A$
$t_{d(off)}$	Turn-Off Delay Time	—	23	—		$R_G = 1.8\Omega$
t_f	Fall Time	—	66	—		$V_{GS} = 4.5V$, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	Nh	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	3290	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1270	—		$V_{DS} = 25V$
C_{riss}	Reverse Transfer Capacitance	—	170	—		$f = 1.0MHz$, See Fig. 5
E_{AS}	Single Pulse Avalanche Energy ②	—	1320 ⑤	290 ⑥	mJ	$I_{AS} = 60A, L = 0.16mH$

Source-Drain Ratings and Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	116 ⑦	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	400		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 60A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	56	84	ns	$T_J = 25^\circ\text{C}, I_F = 60A$
Q_{rr}	Reverse Recovery Charge	—	110	170	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}, L = 0.16mH, R_G = 25\Omega, I_{AS} = 60A, V_{GS} = 10V$ (See Figure 12)
- ③ $I_{SD} \leq 60A, di/dt \leq 110A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.

- ⑤ This is a typical value at device destruction and represents operation outside rated limits.
- ⑥ This is a calculated value limited to $T_J = 175^\circ\text{C}$.
- ⑦ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ R_{θ} is measured at T_J approximately 90°C

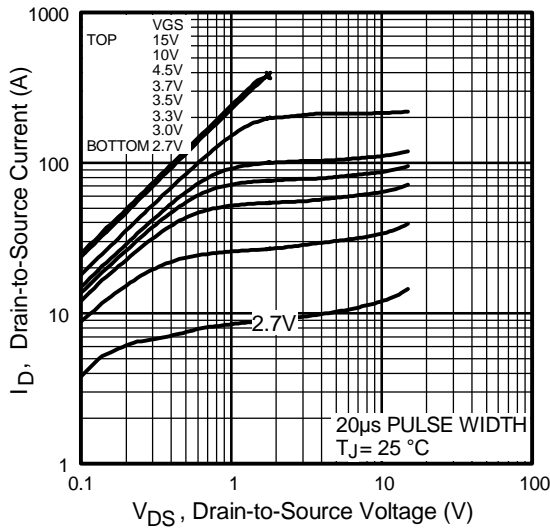


Fig 1. Typical Output Characteristics

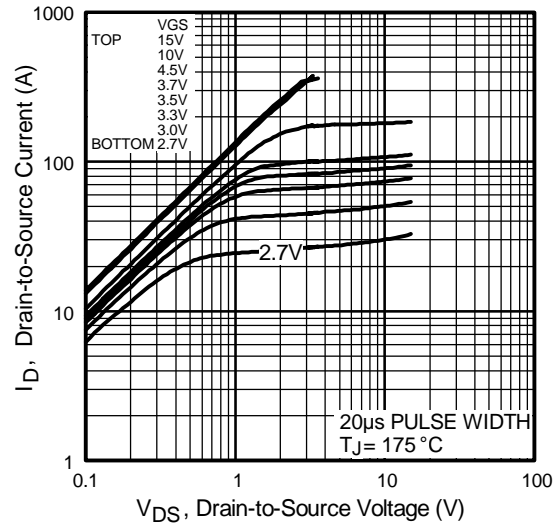


Fig 2. Typical Output Characteristics

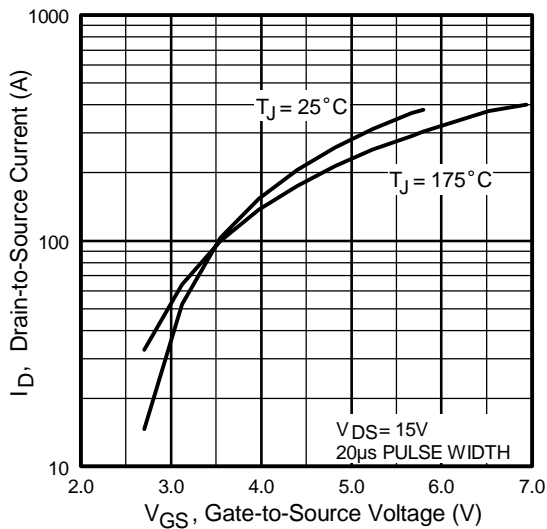


Fig 3. Typical Transfer Characteristics

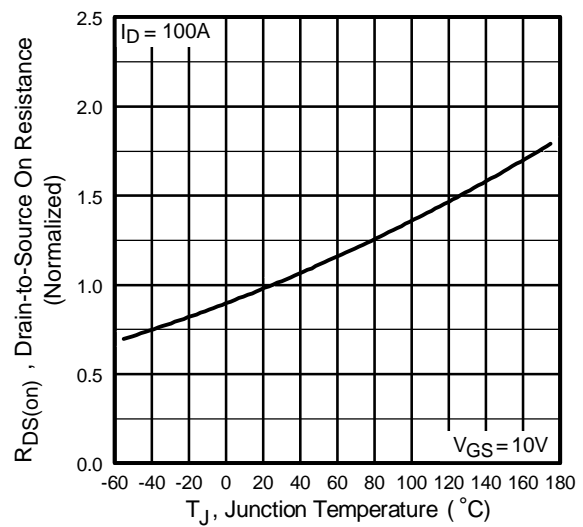


Fig 4. Normalized On-Resistance Vs. Temperature

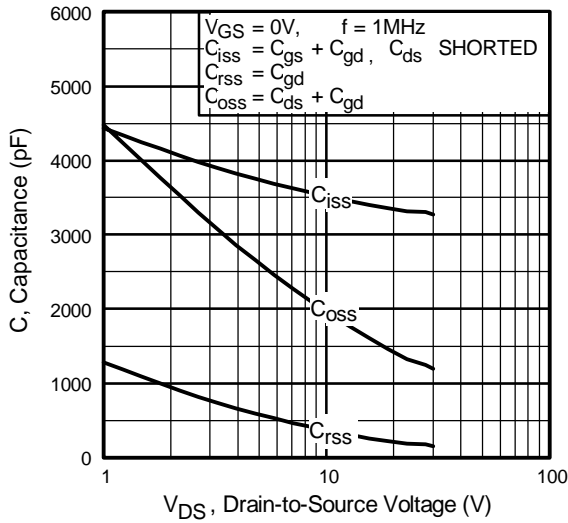


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

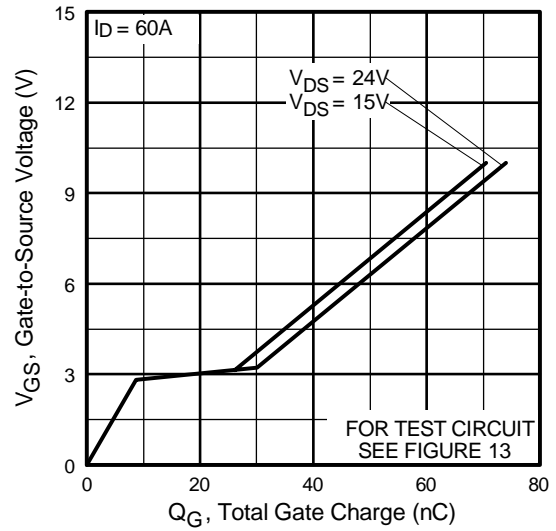


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

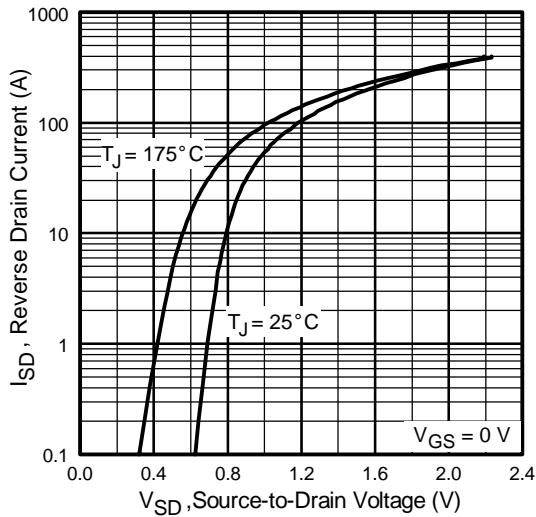


Fig 7. Typical Source-Drain Diode Forward Voltage

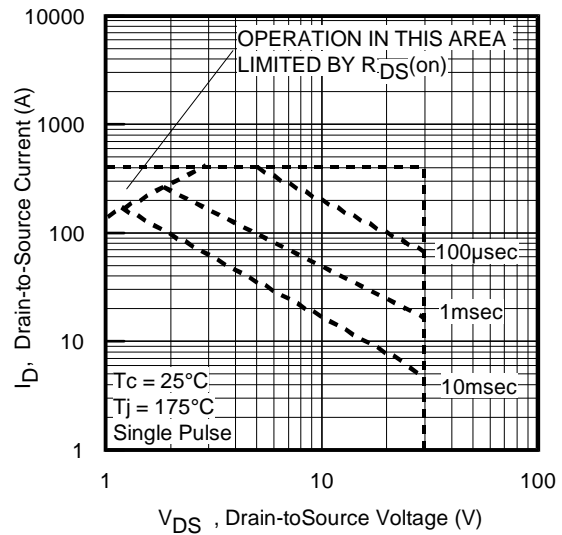


Fig 8. Maximum Safe Operating Area

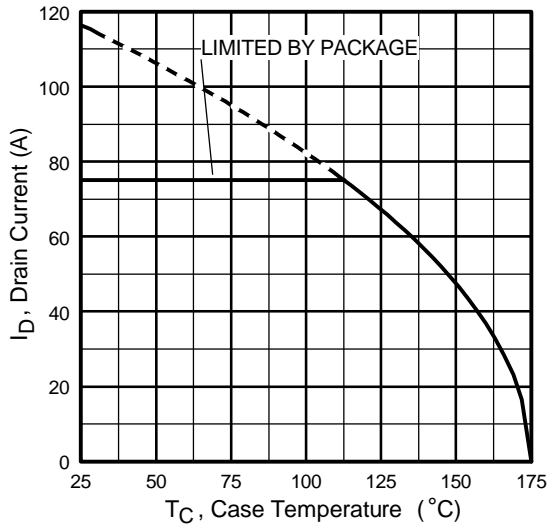


Fig 9. Maximum Drain Current Vs. Case Temperature

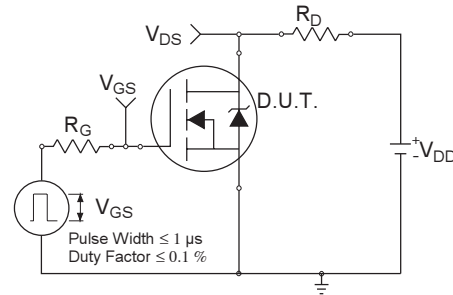


Fig 10a. Switching Time Test Circuit

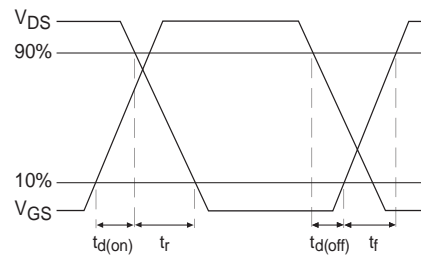


Fig 10b. Switching Time Waveforms

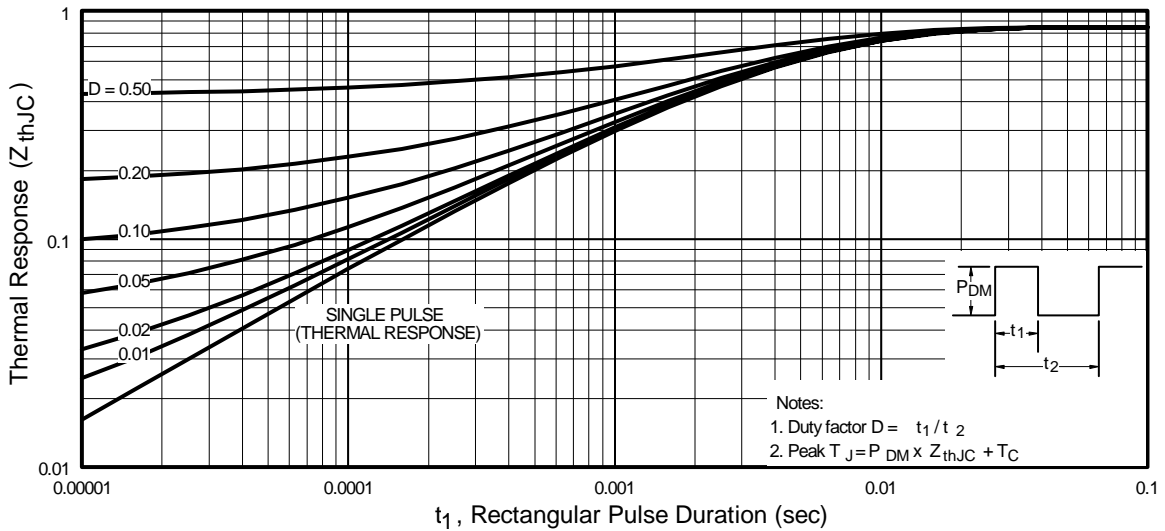


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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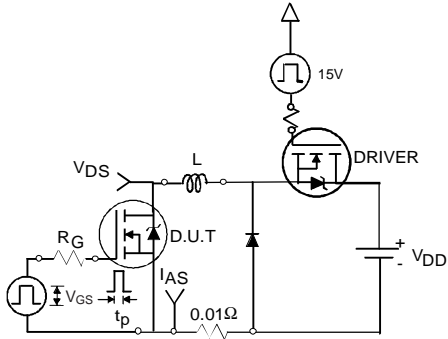


Fig 12a. Unclamped Inductive Test Circuit

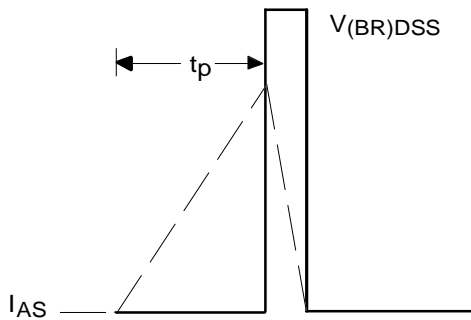


Fig 12b. Unclamped Inductive Waveforms

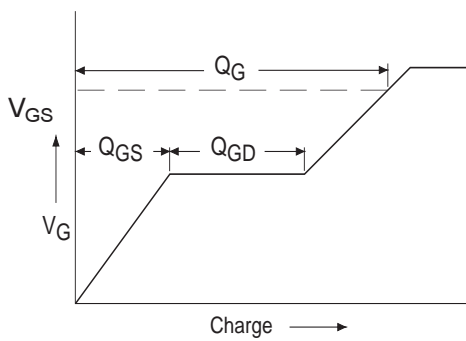


Fig 13a. Basic Gate Charge Waveform

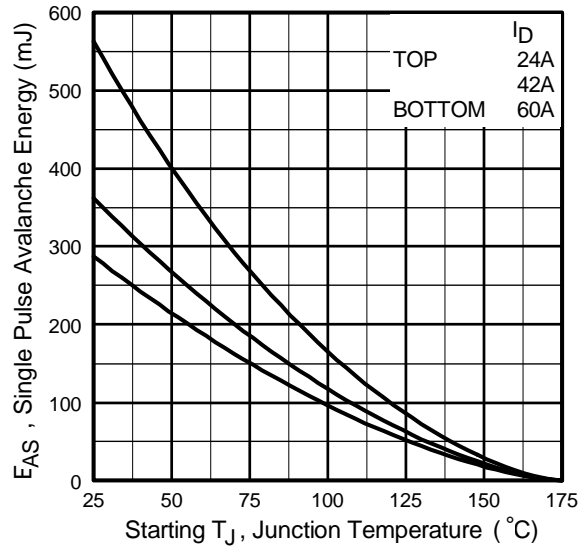


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

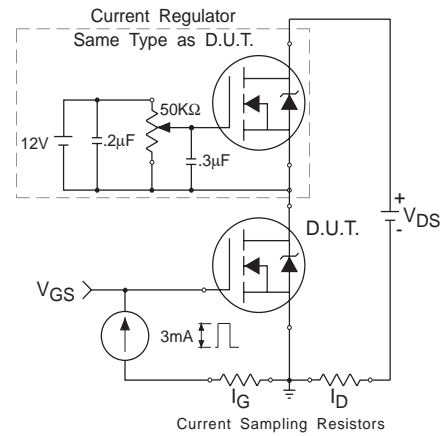
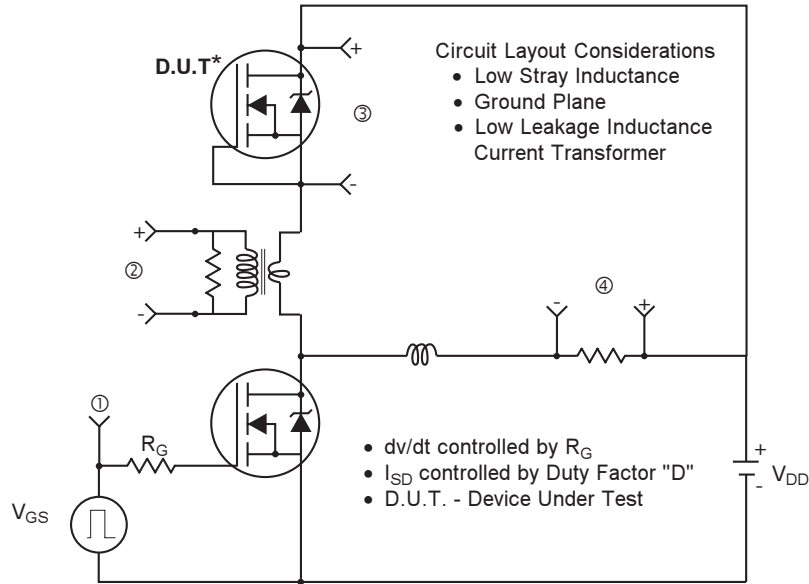
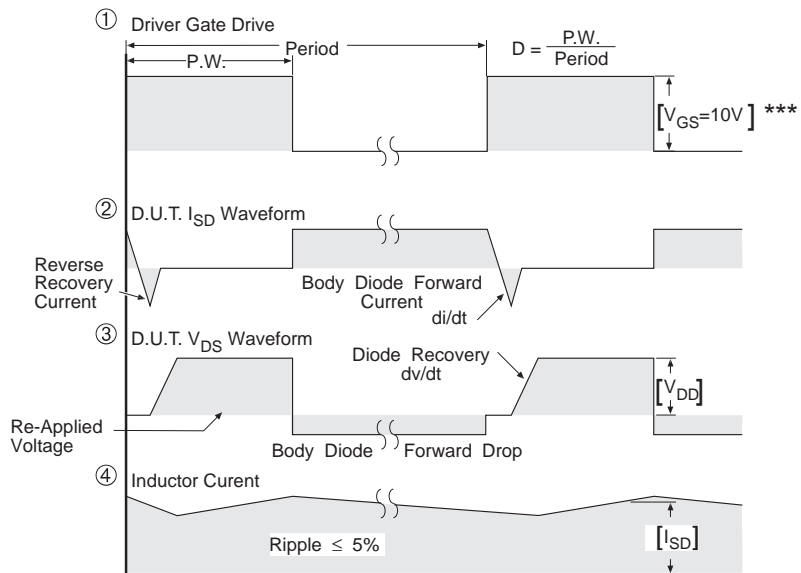


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

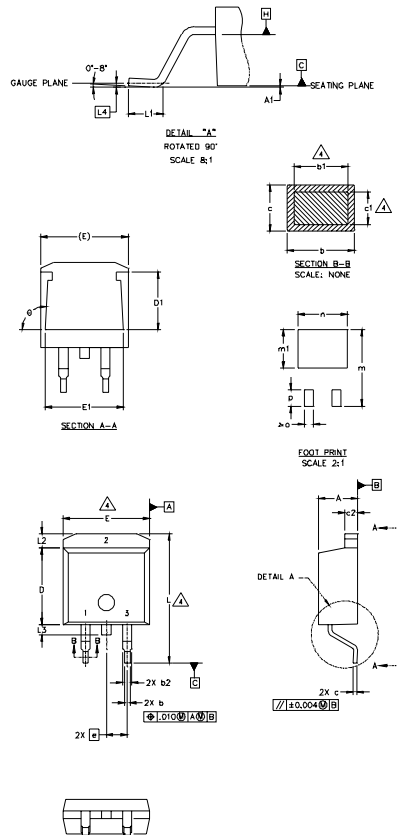
Fig 14. For N-channel HEXFET® power MOSFETs

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D²Pak Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1		0.127		.005	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.43	0.63	.017	.025	
c1	0.38	0.74	.015	.029	3
c2	1.14	1.40	.045	.055	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	
L2		1.65		.065	
L3	1.27	1.78	.050	.070	
L4	0.25 BSC		.010 BSC		
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
θ	90°	93°	90°	93°	

LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK	DIODES
1.- GATE	1.- GATE	1.- ANODE *
2.- DRAIN	2.- COLLECTOR	2.- CATHODE
3.- SOURCE	3.- EMITTER	3.- ANODE

* PART DEPENDENT.

FINISHING AND TOLERANCING PER ASME Y14.5M-1994

ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).

IN D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 (.005")

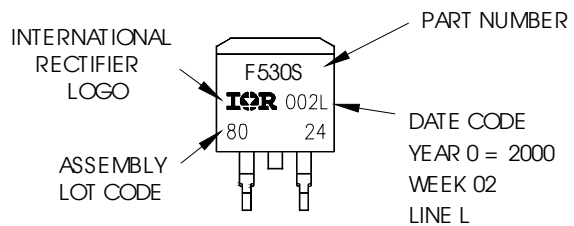
E. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.

IN b1 AND c1 APPLY TO BASE METAL ONLY.

5. CONTROLLING DIMENSION: INCH.

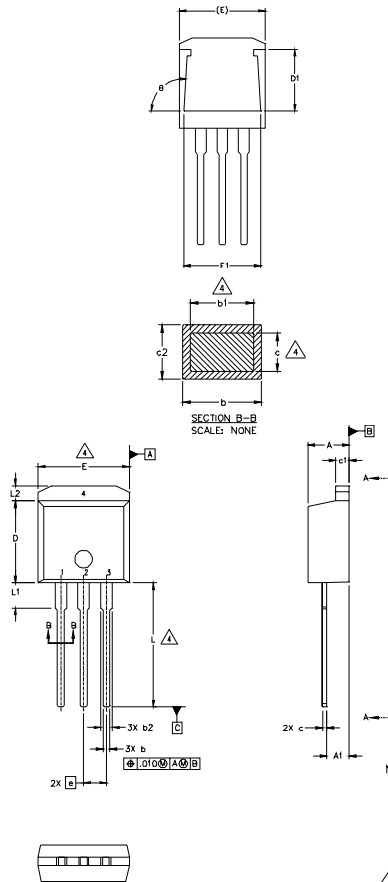
D²Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW02, 2000
IN THE ASSEMBLY LINE "L"



TO-262 Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.38	0.63	.015	.025	
c1	1.14	1.40	.045	.055	3
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

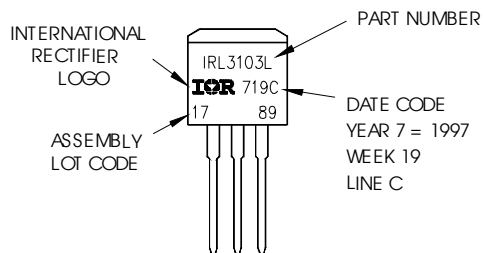
LEAD ASSIGNMENTS

HEXFET	IGBT
1.- GATE	1- GATE
2.- DRAIN	2- COLLECTOR
3.- SOURCE	
4.- DRAIN	

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
 4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
 5. CONTROLLING DIMENSION: INCH.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

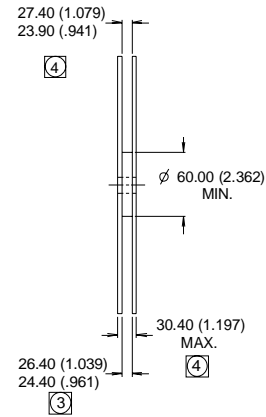
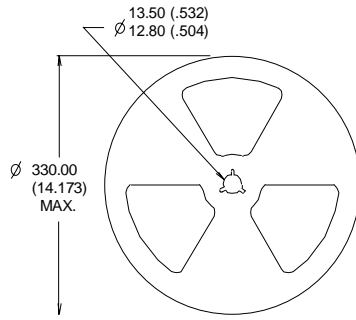
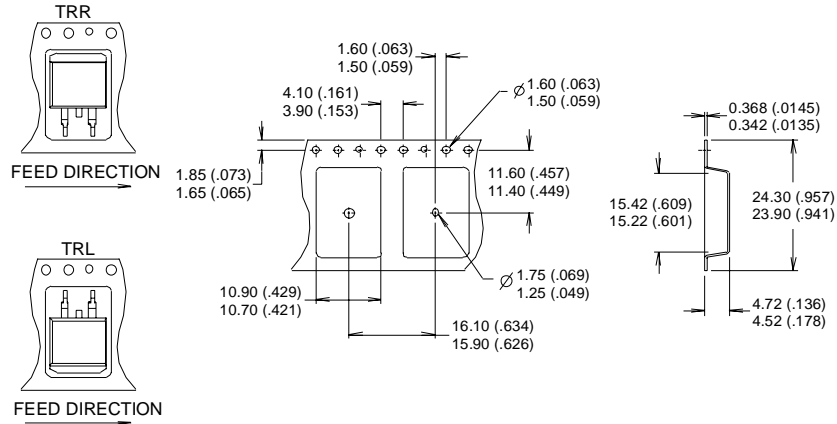


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D²Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES:
1. CONFORMS TO EIA-418.
 2. CONTROLLING DIMENSION: MILLIMETER.
 - ③ DIMENSION MEASURED @ HUB.
 - ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information. 11/03

www.irf.com

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>