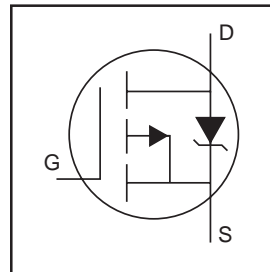


# IRL5602S

HEXFET® Power MOSFET

- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- P-Channel
- Fast Switching
- Fully Avalanche Rated

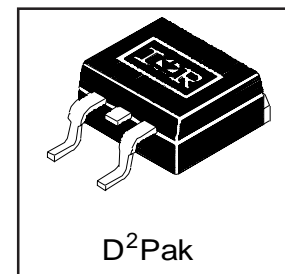


$V_{DSS} = -20V$
$R_{DS(on)} = 0.042\Omega$
$I_D = -24A$

## Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D<sup>2</sup>Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V$	-24	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V$	-17	
$I_{DM}$	Pulsed Drain Current ①	-96	
$P_D @ T_C = 25^\circ C$	Power Dissipation	75	W
	Linear Derating Factor	0.5	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 8.0$	V
$E_{AS}$	Single Pulse Avalanche Energy②	290	mJ
$I_{AR}$	Avalanche Current①	-12	A
$E_{AR}$	Repetitive Avalanche Energy①	7.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-0.81	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

## Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient ( PCB Mounted, steady-state)**	—	40	

## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	-20	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	-0.013	—	V/°C	Reference to 25°C, I <sub>D</sub> = -1mA <sup>⑤</sup>
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.042	Ω	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -12A <sup>④</sup>
		—	—	0.062		V <sub>GS</sub> = -2.7V, I <sub>D</sub> = -10A <sup>④</sup>
		—	—	0.075		V <sub>GS</sub> = -2.5V, I <sub>D</sub> = -10A <sup>④</sup>
V <sub>GS(th)</sub>	Gate Threshold Voltage	-0.7	—	-1.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
g <sub>fs</sub>	Forward Transconductance	12	—	—	S	V <sub>DS</sub> = -15V, I <sub>D</sub> = -12A <sup>⑤</sup>
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	-25	μA	V <sub>DS</sub> = -20V, V <sub>GS</sub> = 0V
		—	—	-250		V <sub>DS</sub> = -16V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	500	nA	V <sub>GS</sub> = -8.0V
	Gate-to-Source Reverse Leakage	—	—	-500		V <sub>GS</sub> = 8.0V
Q <sub>g</sub>	Total Gate Charge	—	—	44	nC	I <sub>D</sub> = -12A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	8.7		V <sub>DS</sub> = -16V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	19		V <sub>GS</sub> = -4.5V, See Fig. 6 and 13 <sup>④⑤</sup>
t <sub>d(on)</sub>	Turn-On Delay Time	—	9.7	—	ns	V <sub>DD</sub> = -10 V
t <sub>r</sub>	Rise Time	—	73	—		I <sub>D</sub> = -12A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	53	—		R <sub>G</sub> = 6.0Ω, V <sub>GS</sub> = 4.5V
t <sub>f</sub>	Fall Time	—	84	—		R <sub>D</sub> = 0.8Ω, See Fig. 10 <sup>④⑤</sup>
L <sub>S</sub>	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C <sub>iss</sub>	Input Capacitance	—	1460	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	790	—		V <sub>DS</sub> = -15V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	370	—		f = 1.0MHz, See Fig. 5 <sup>⑤</sup>

## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	-24	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>①</sup>	—	—	-96		
V <sub>SD</sub>	Diode Forward Voltage	—	—	-1.4	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = -12A, V <sub>GS</sub> = 0V <sup>④</sup>
t <sub>rr</sub>	Reverse Recovery Time	—	58	88	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = -12A
Q <sub>rr</sub>	Reverse Recovery Charge	—	54	81	nC	di/dt = -100A/μs <sup>④</sup>
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

### Notes:

① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )

② Starting T<sub>J</sub> = 25°C, L = 3.0mH  
R<sub>G</sub> = 25Ω, I<sub>AS</sub> = -14A. (See Figure 12)

③ I<sub>SD</sub> ≤ -12A, di/dt ≤ 120A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>,  
T<sub>J</sub> ≤ 175°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

\*\* When mounted on FR-4 board using minimum recommended footprint.  
For recommended footprint and soldering techniques refer to application note #AN-994.

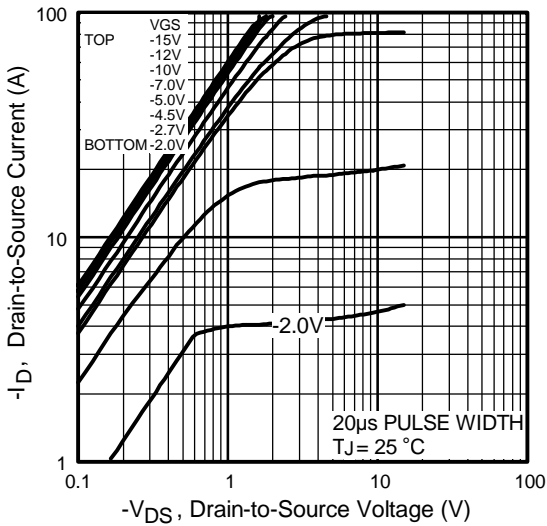


Fig 1. Typical Output Characteristics

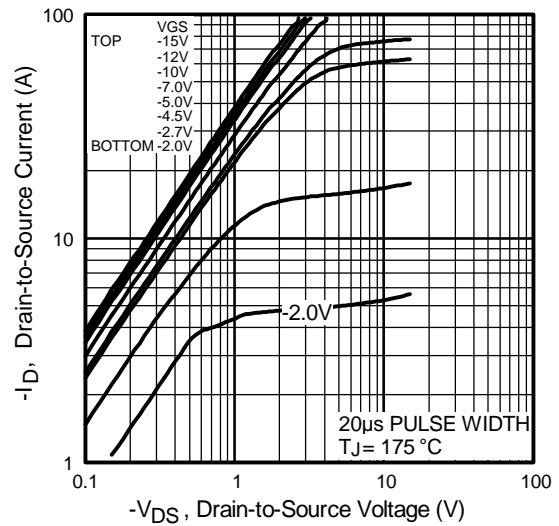


Fig 2. Typical Output Characteristics

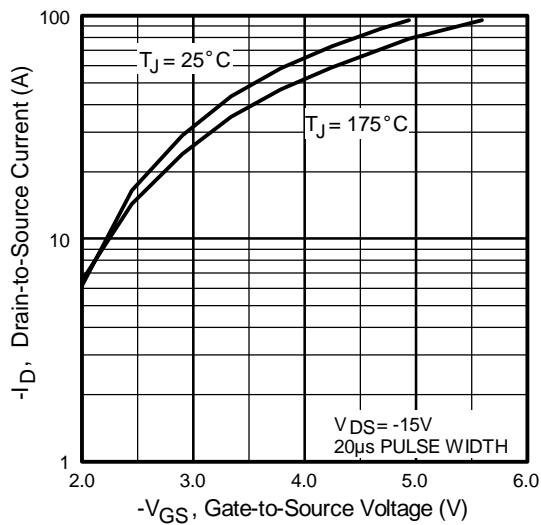


Fig 3. Typical Transfer Characteristics

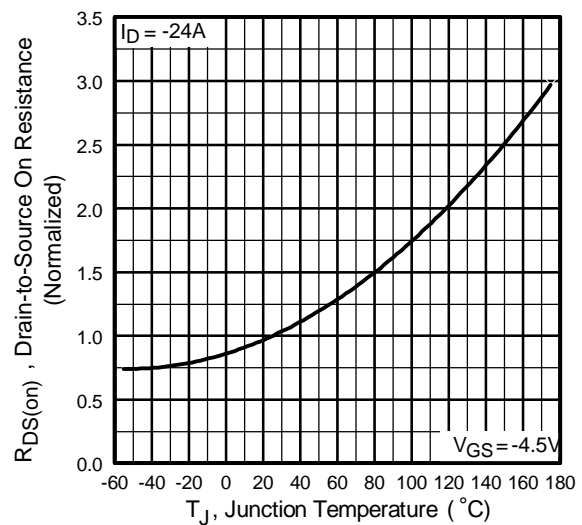
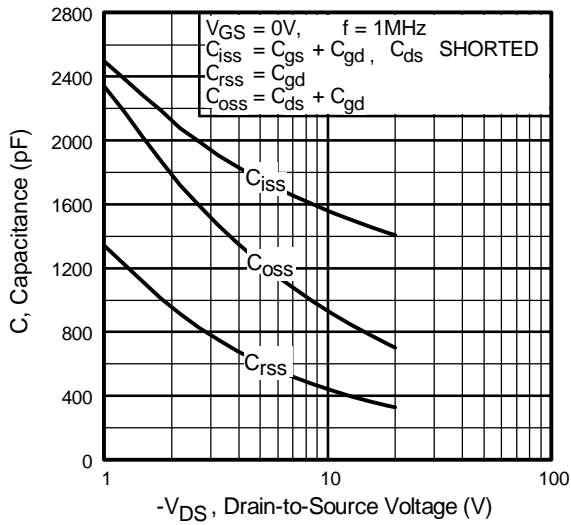
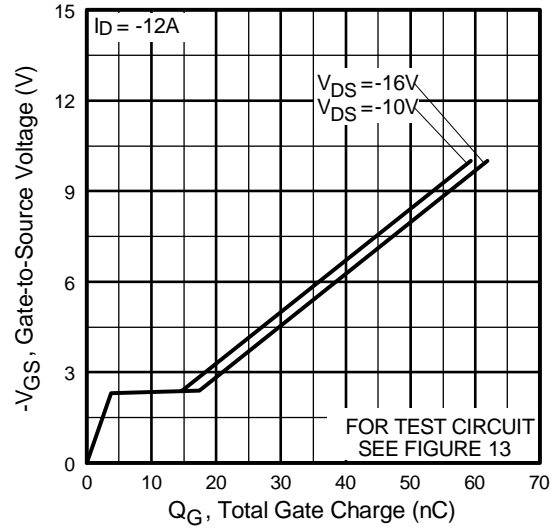


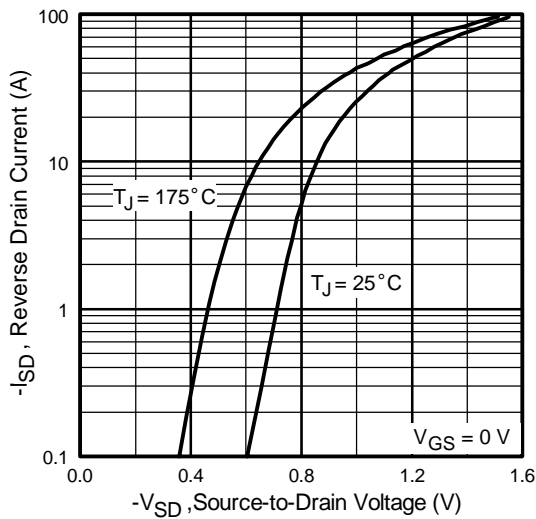
Fig 4. Normalized On-Resistance Vs. Temperature



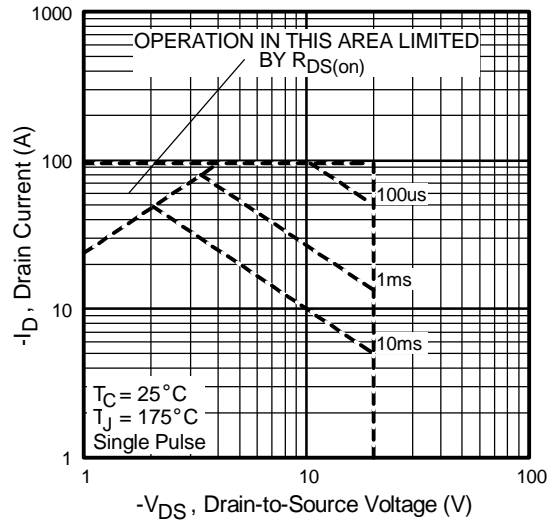
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



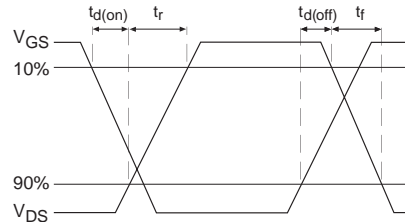
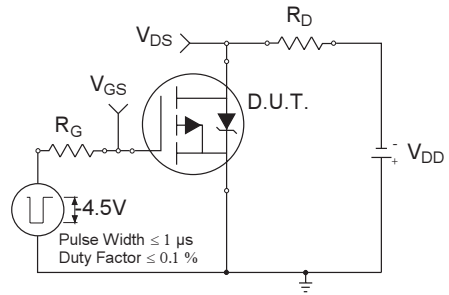
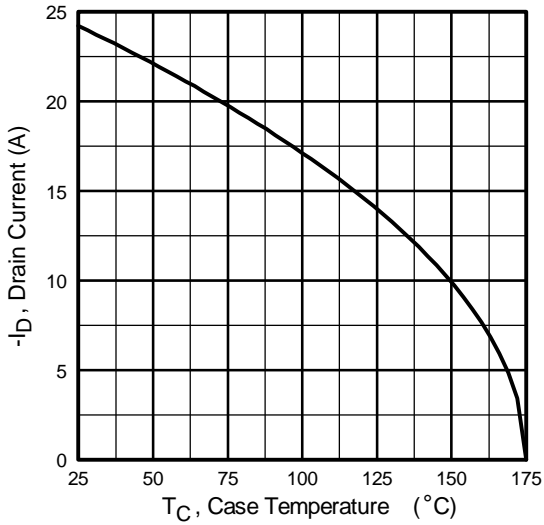
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



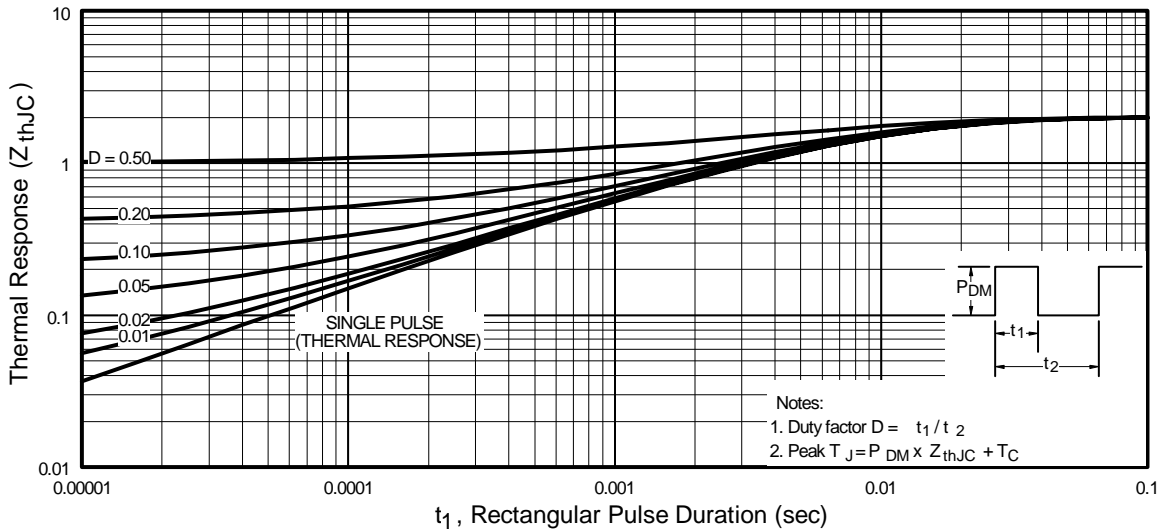
**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area



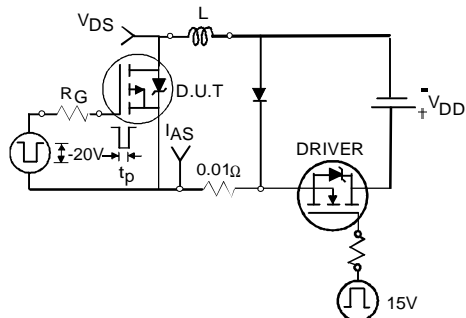
**Fig 9.** Maximum Drain Current Vs. Case Temperature



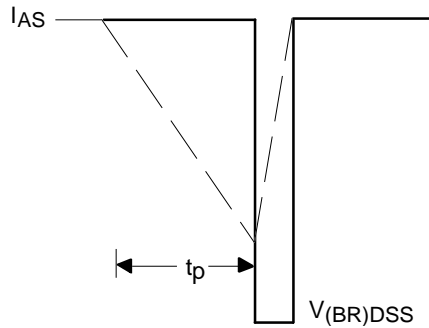
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

# IRL5602S

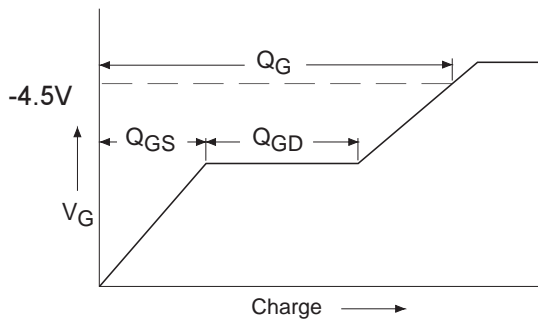
International  
**IR** Rectifier



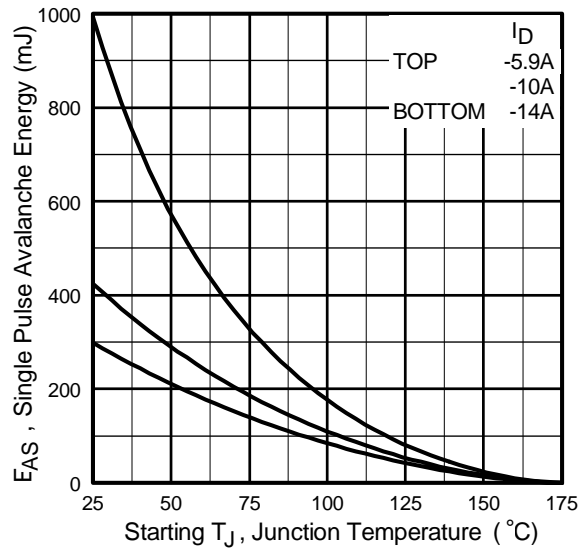
**Fig 12a.** Unclamped Inductive Test Circuit



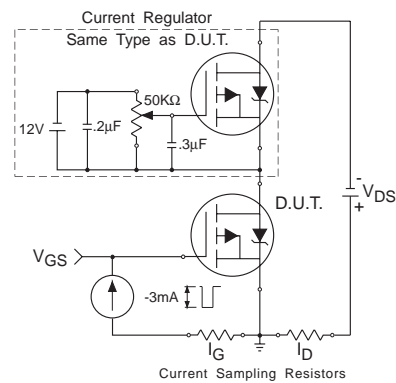
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform

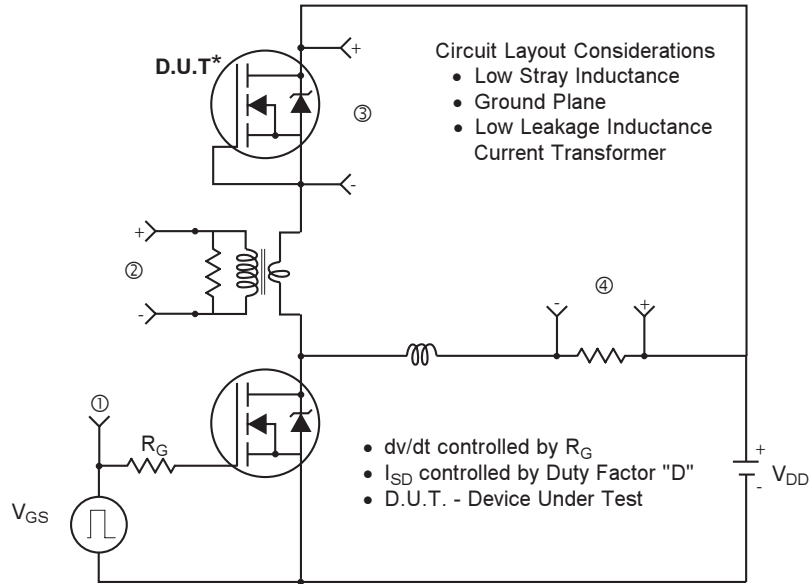


**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

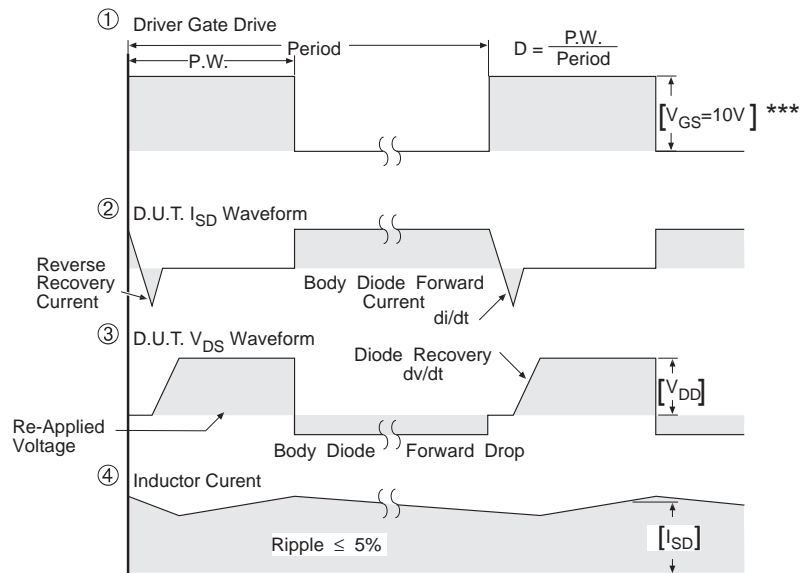


**Fig 13b.** Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity of D.U.T for P-Channel

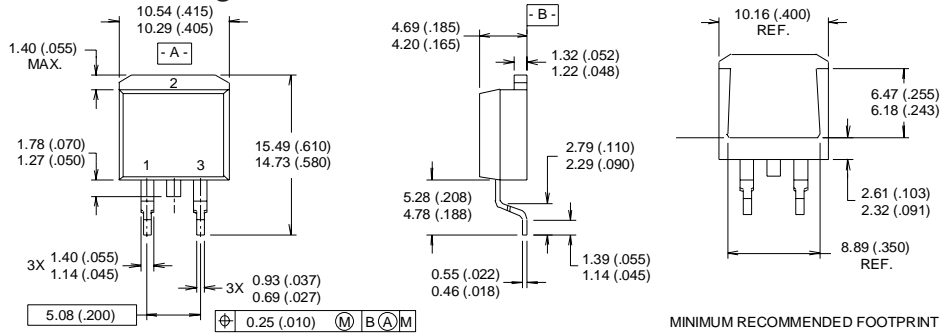


\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

Fig 14. For P-Channel HEXFETS

# IRL5602S TO-263AB Package Details

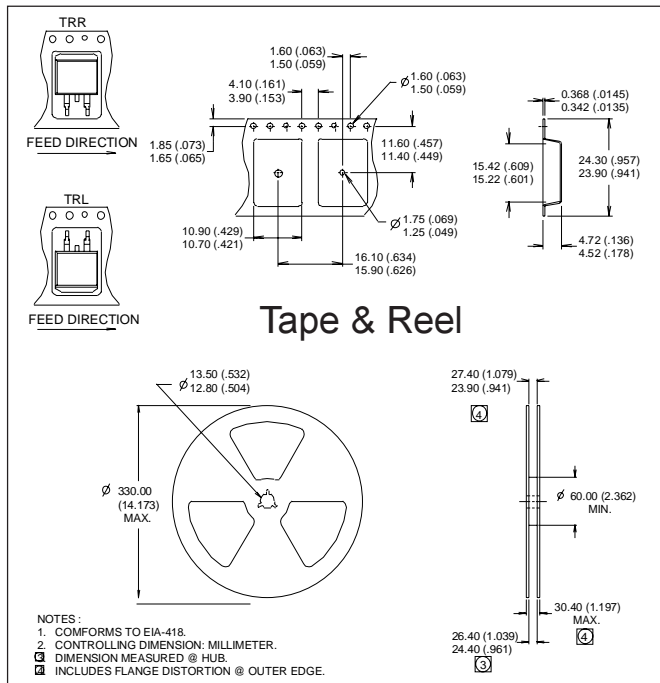
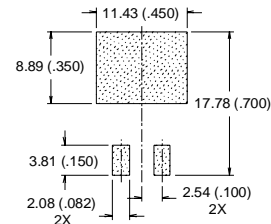
International  
**IR** Rectifier



- NOTES:
- 1 DIMENSIONS AFTER SOLDER DIP.
  - 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
  - 3 CONTROLLING DIMENSION : INCH.
  - 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

- LEAD ASSIGNMENTS
- 1 - GATE
  - 2 - DRAIN
  - 3 - SOURCE

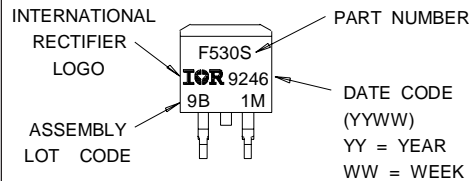
MINIMUM RECOMMENDED FOOTPRINT



- NOTES:
1. CONFORMS TO EIA-418.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION MEASURED @ HUB.
  4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

## Part Marking

(This is an IRF530S with assembly lot code 9B1M)



International  
**IR** Rectifier

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**IR CANADA:** 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200  
**IR GERMANY:** Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590  
**IR ITALY:** Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111  
**IR FAR EAST:** K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086  
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<http://www.irf.com/> Data and specifications subject to change without notice. 5/99



Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>