April 2005

FDS6673AZ
30 Volt P-Channel PowerTrench® MOSFET

Features

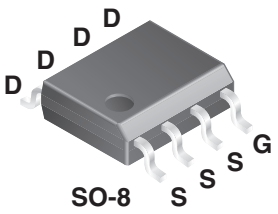
- –14.5 A, –30 V. $R_{DS(ON)}$ = 7.2 mΩ @ V_{GS} = –10 V
  $R_{DS(ON)}$ = 11 mΩ @ V_{GS} = – 4.5 V
- Extended V_{GSS} range (–25V) for battery applications
- ESD protection diode (note 3)
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability

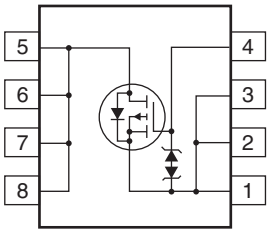
General Description

This P-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers, and battery chargers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(ON)}$ specifications.

The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DSS}	Drain-Source Voltage			–30	V
V_{GSS}	Gate-Source Voltage			±25	V
I_D	Drain Current	– Continuous	(Note 1a)	–14.5	A
		– Pulsed		–50	
P_D	Power Dissipation for Single Operation		(Note 1a)	2.5	W
			(Note 1b)	1.2	
			(Note 1c)	1.0	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			–55 to +175	°C
Thermal Characteristics					
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient		(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case		(Note 1)	25	°C/W

Package Marking and Ordering Information

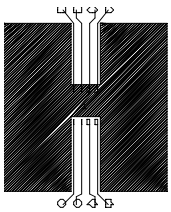
Device Marking	Device	Reel Size	Tape width	Quantity
FDS6673AZ	FDS6673AZ	13”	12mm	2500 units

Electrical Characteristics T_A = 25°C unless otherwise noted

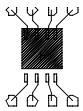
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 µA	–30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C		–25		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –24 V, V_{GS} = 0 V			–1	µA
I_{GSS}	Gate–Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V			±10	µA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 µA	–1	–1.6	–3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C		5.8		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –10 V, I_D = –14.5 A V_{GS} = –4.5 V, I_D = –12 A V_{GS} = –4.5 V, I_D = –14.5A, T_J = 125°C		6.0 8.8 7.8	7.2 11 10.4	mΩ
g_{FS}	Forward Transconductance	V_{DS} = –5 V, I_D = –14.5 A		50		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = –15 V, V_{GS} = 0 V, f = 1.0 MHz		4480		pF
C_{oss}	Output Capacitance			1190		pF
C_{rss}	Reverse Transfer Capacitance			615		pF
R_G	Gate Resistance	V_{GS} = 15 mV, f = 1.0 MHz		3.8		
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –15 V, I_D = –1 A, V_{GS} = –10 V, R_{GEN} = 6 Ω		22	35	ns
t_r	Turn–On Rise Time			8	16	ns
$t_{d(off)}$	Turn–Off Delay Time			134	214	ns
t_f	Turn–Off Fall Time			79	126	ns
Q_g	Total Gate Charge	V_{DS} = –15 V, I_D = –14.5 A, V_{GS} = –10 V		84	118	nC
Q_{gs}	Gate–Source Charge			12		nC
Q_{gd}	Gate–Drain Charge			19		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				–2.1	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –2.1 A (Note 2)		–0.7	–1.2	V
t_{RR}	Reverse Recovery Time	I_F = –14.5 A, d_{iF}/d_t = 100 A/µs (Note 2)		44		ns
Q_{RR}	Reverse Recovery Charge			29		nC

Notes:

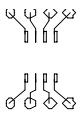
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W (10 sec) 62.5° C/W steady state when mounted on a 1 in^2 pad of 2 oz copper



b) 105°C/W when mounted on a .04 in^2 pad of 2 oz copper



c) 125°/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics

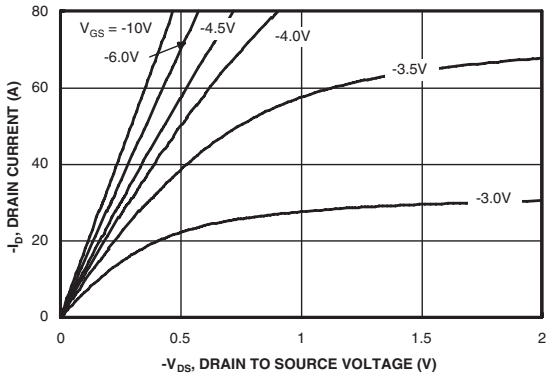


Figure 1. On-Region Characteristics.

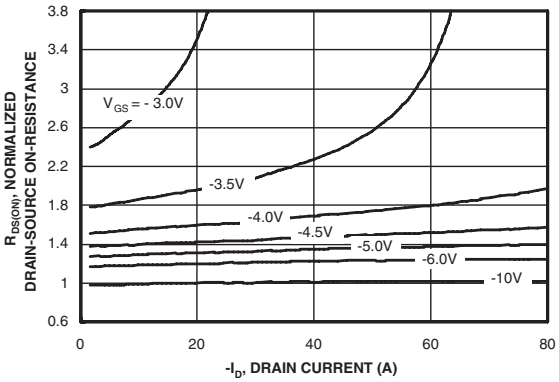


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

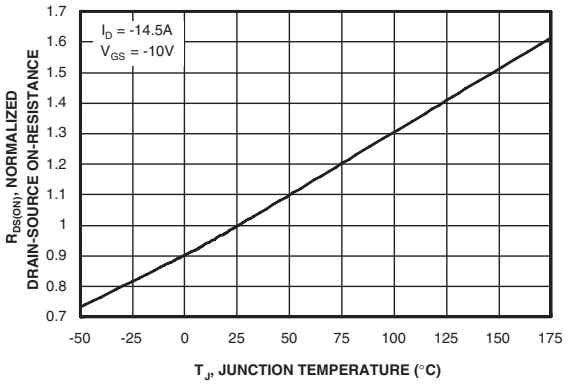


Figure 3. On-Resistance Variation with Temperature.

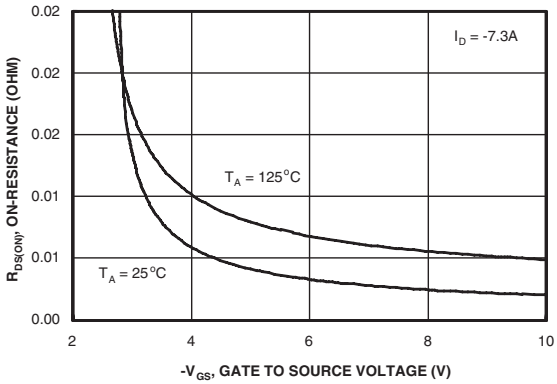


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

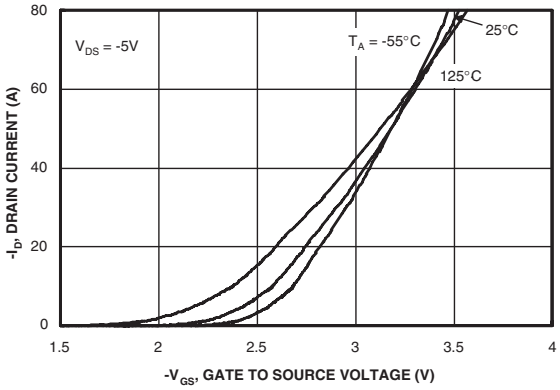


Figure 5. Transfer Characteristics.

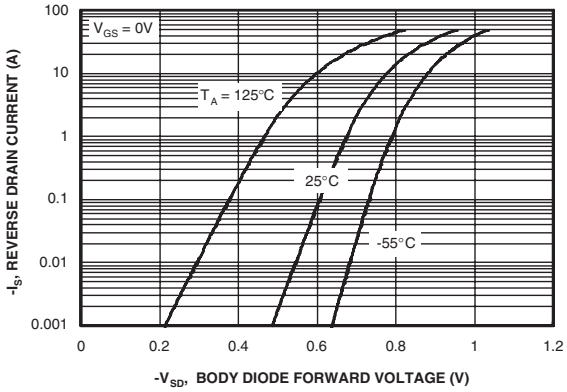


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

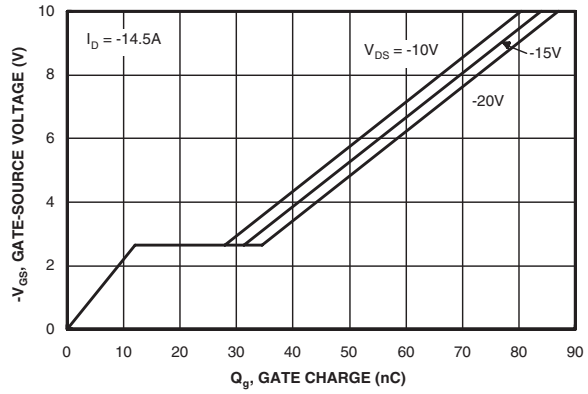


Figure 7. Gate Charge Characteristics.

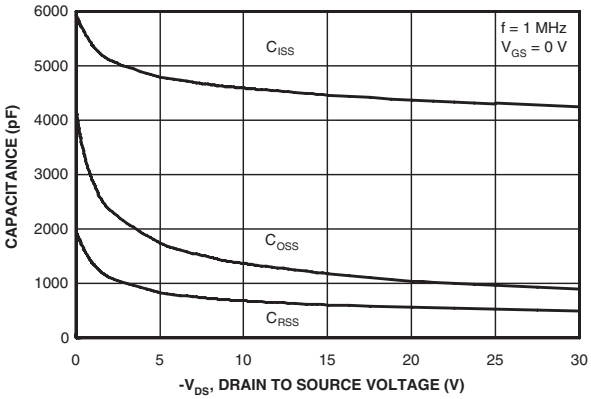


Figure 8. Capacitance Characteristics.

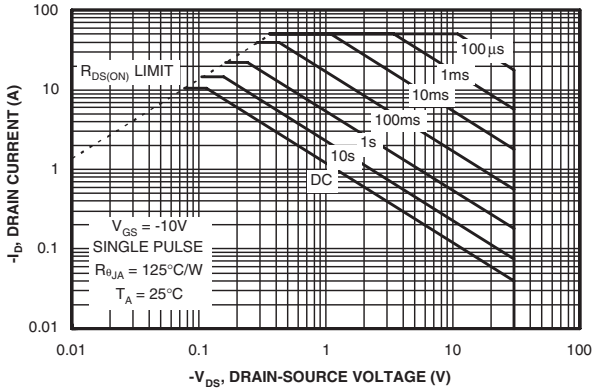


Figure 9. Maximum Safe Operating Area.

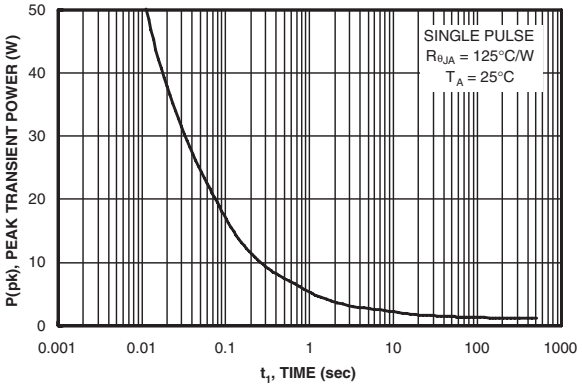


Figure 10. Single Pulse Maximum Power Dissipation.

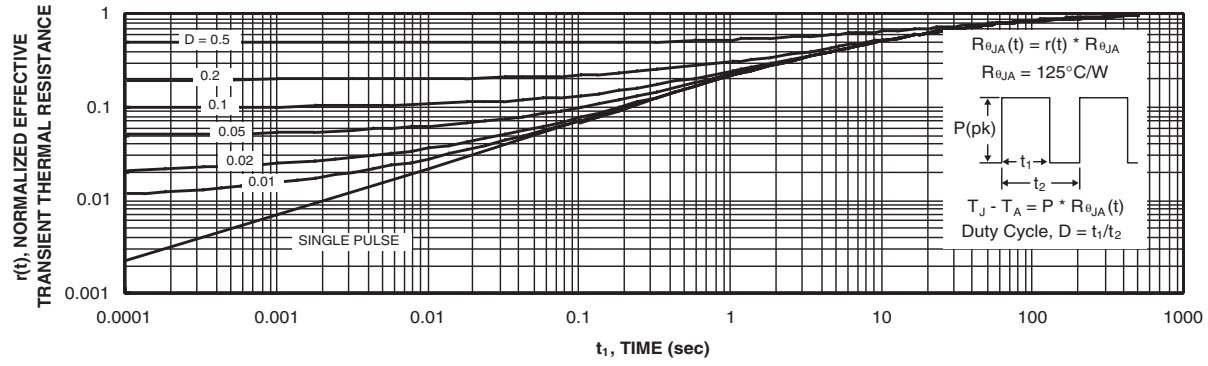


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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