

# FDS4435A

## P-Channel Logic Level PowerTrench® MOSFET

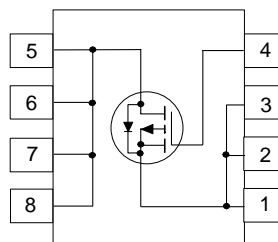
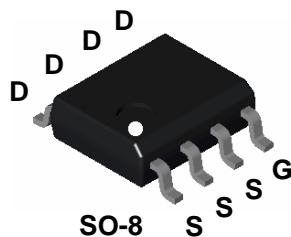
### General Description

This P-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

These devices are well suited for notebook computer applications: load switching and power management, battery charging circuits, and DC/DC conversion.

### Features

- -9 A, -30 V.  $R_{DS(ON)} = 0.017 \Omega @ V_{GS} = -10 \text{ V}$   
 $R_{DS(ON)} = 0.025 \Omega @ V_{GS} = -4.5 \text{ V}$
- Low gate charge (21nC typical).
- High performance trench technology for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.



### Absolute Maximum Ratings T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage	-30	V
V <sub>GSS</sub>	Gate-Source Voltage	± 20	V
I <sub>D</sub>	Drain Current - Continuous (Note 1a) - Pulsed	-9	A
		-50	
P <sub>D</sub>	Power Dissipation for Single Operation (Note 1a) (Note 1b) (Note 1c)	2.5	W
		1.2	
		1	
T <sub>J</sub> , T <sub>stg</sub>	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	25	°C/W

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
FDS4435A	FDS4435A	13"	12mm	2500 units

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-26		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}, V_{GS} = 0$ $T_J = 125^\circ\text{C}$			-1 -10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

## On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-1	-1.7	-2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		4.2		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -9\text{ A}$		0.015	0.017	$\Omega$
		$T_J = 125^\circ\text{C}$		0.021	0.030	
		$V_{GS} = -4.5\text{ V}, I_D = -7\text{ A}$		0.023	0.025	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$	-40			A
$g_{FS}$	Forward Transconductance	$V_{DS} = -10\text{ V}, I_D = -9\text{ A}$		25		S

## Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}$ $f = 1.0\text{ MHz}$		2010		pF
$C_{oss}$	Output Capacitance			590		pF
$C_{rss}$	Reverse Transfer Capacitance			260		pF

## Switching Characteristics (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -15\text{ V}, I_D = -1\text{ A}$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\ \Omega$		12	22	ns
$t_r$	Turn-On Rise Time			15	27	ns
$t_{d(off)}$	Turn-Off Delay Time			100	140	ns
$t_f$	Turn-Off Fall Time			55	80	ns
$Q_g$	Total Gate Charge	$V_{DS} = -15\text{ V}, I_D = -9\text{ A}$ $V_{GS} = -5\text{ V}$		21	30	nC
$Q_{gs}$	Gate-Source Charge			6		nC
$Q_{gd}$	Gate-Drain Charge			8		nC

## Drain-Source Diode Characteristics and Maximum Ratings

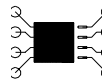
$I_S$	Maximum Continuous Drain-Source Diode Forward Current			-2.1	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -2.1\text{ A}$ (Note 2)		0.75	-1.2	V
$t_{rr}$	Source-Drain Reverse Recovery Time	$I_F = -10\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{S}$		36	80	ns

### Notes:

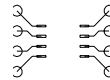
1:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $50^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz. copper.



b)  $105^\circ\text{C/W}$  when mounted on a  $0.04\text{ in}^2$  pad of 2 oz. copper.



c)  $125^\circ\text{C/W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2: Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$

Typical Characteristics

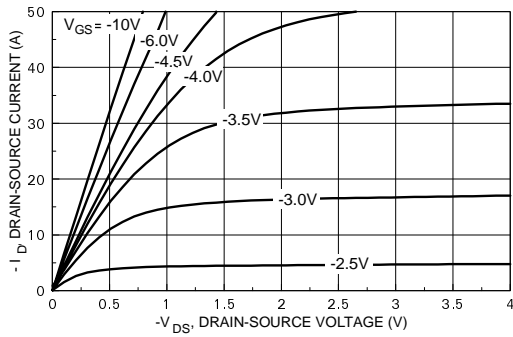


Figure 1. On-Region Characteristics

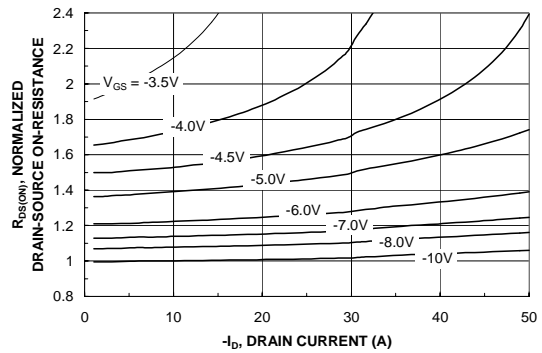


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

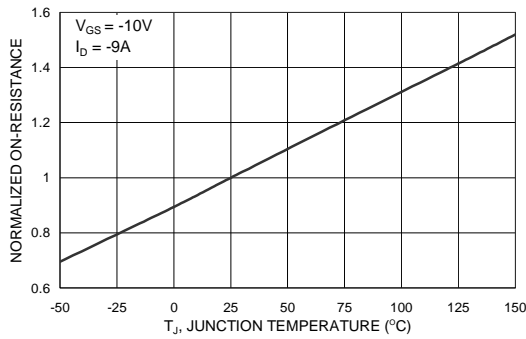


Figure 3. On-Resistance Variation with Temperature

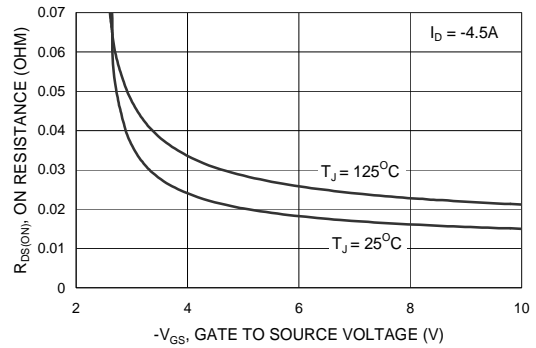


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

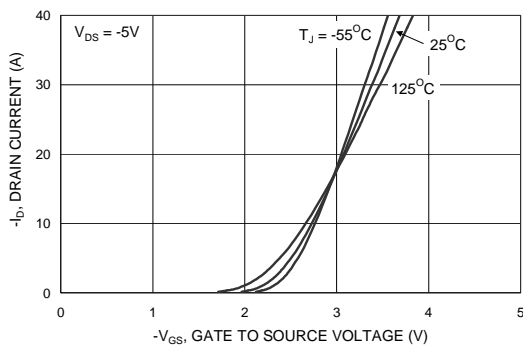


Figure 5. Transfer Characteristics

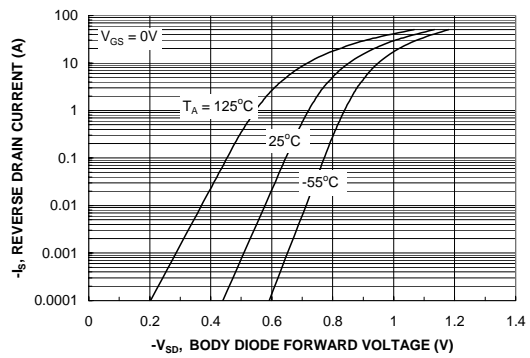
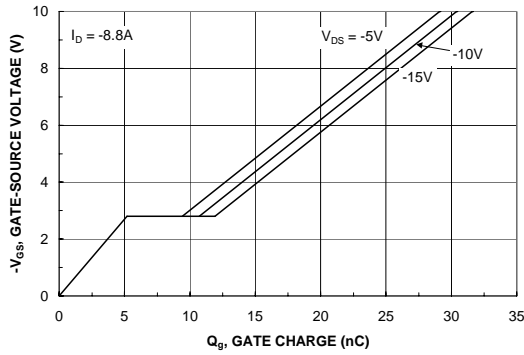
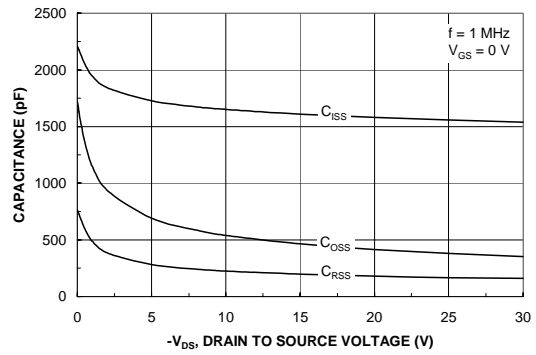


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

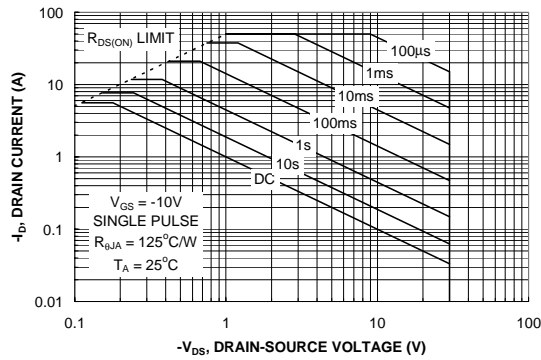
**Typical Characteristics** (continued)



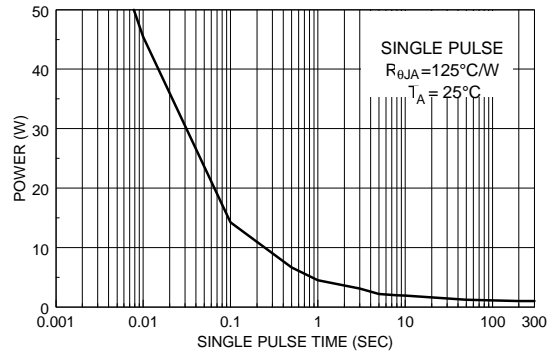
**Figure 7. Gate-Charge Characteristics**



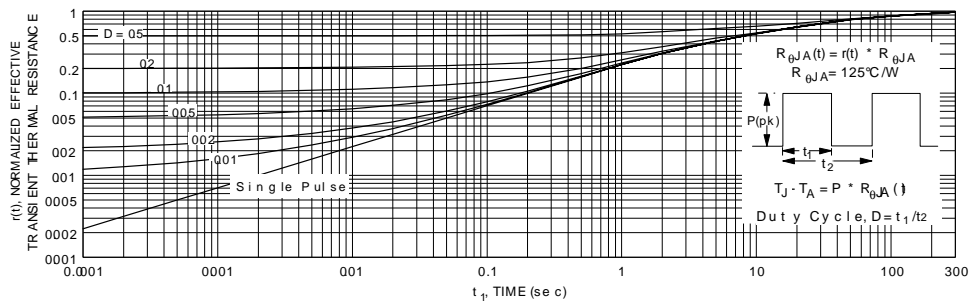
**Figure 8. Capacitance Characteristics**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Single Pulse Maximum Power Dissipation**



**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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