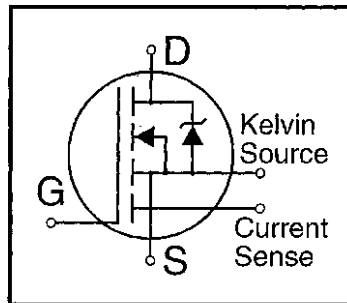


## HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Current Sense
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



$$V_{DSS} = 200V$$

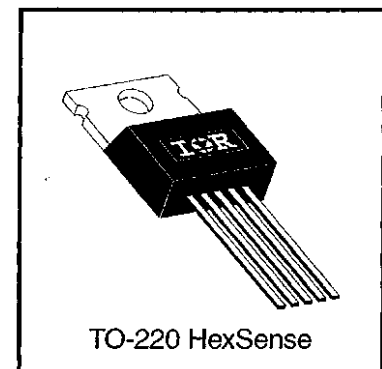
$$R_{DS(on)} = 0.18\Omega$$

$$I_D = 18A$$

### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The HEXSense device provides an accurate fraction of the drain current through the additional two leads to be used for control or protection of the device. These devices exhibit similar electrical and thermal characteristics as their IRF-series equivalent part numbers. The provision of a kelvin source connection effectively eliminates problems of common source inductance when the HEXSense is used as a fast, high-current switch in non current-sensing applications.



TO-220 HexSense

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### Absolute Maximum Ratings

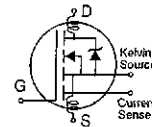
	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	18	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	11	
$I_{DM}$	Pulsed Drain Current ①	72	
$P_D @ T_C = 25^\circ C$	Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	430	mJ
$I_{AR}$	Avalanche Current ①	18	A
$E_{AR}$	Repetitive Avalanche Energy ①	13	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.0	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.29	—	V/°C	Reference to $25^\circ\text{C}$ , $I_D=1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.18	$\Omega$	$V_{GS}=10V, I_D=11A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
$g_{fs}$	Forward Transconductance	6.5	—	—	S	$V_{DS}=50V, I_D=11A$ ④
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS}=200V, V_{GS}=0V$
		—	—	250		$V_{DS}=160V, V_{GS}=0V, T_J=125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS}=20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS}=-20V$
$Q_g$	Total Gate Charge	—	—	70	nC	$I_D=18A$
$Q_{gs}$	Gate-to-Source Charge	—	—	13		$V_{DS}=160V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	39		$V_{GS}=10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	$V_{DD}=100V$
$t_r$	Rise Time	—	51	—		$I_D=18A$
$t_{d(off)}$	Turn-Off Delay Time	—	45	—		$R_G=9.1\Omega$
$t_f$	Fall Time	—	36	—		$R_D=3.2\Omega$ ④
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	1300	—	pF	$V_{GS}=0V$
$C_{oss}$	Output Capacitance	—	430	—		$V_{DS}=25V$
$C_{rss}$	Reverse Transfer Capacitance	—	130	—		$f=1.0\text{MHz}$
$r$	Current Sensing Ratio	2600	—	2880	—	$I_D=18A, V_{GS}=10V$
$C_{oss}$	Output Capacitance of Sensing Cells	—	9.0	—	pF	$V_{GS}=0V, V_{DS}=25V, f=1.0\text{MHz}$



## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	18	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	72		
$V_{SD}$	Diode Forward Voltage	—	—	2.0	V	$T_J=25^\circ\text{C}, I_S=18A, V_{GS}=0V$ ④
$t_{rr}$	Reverse Recovery Time	—	300	610	ns	$T_J=25^\circ\text{C}, I_F=18A$
$Q_{rr}$	Reverse Recovery Charge	—	3.4	7.1	$\mu C$	$di/dt=100A/\mu s$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

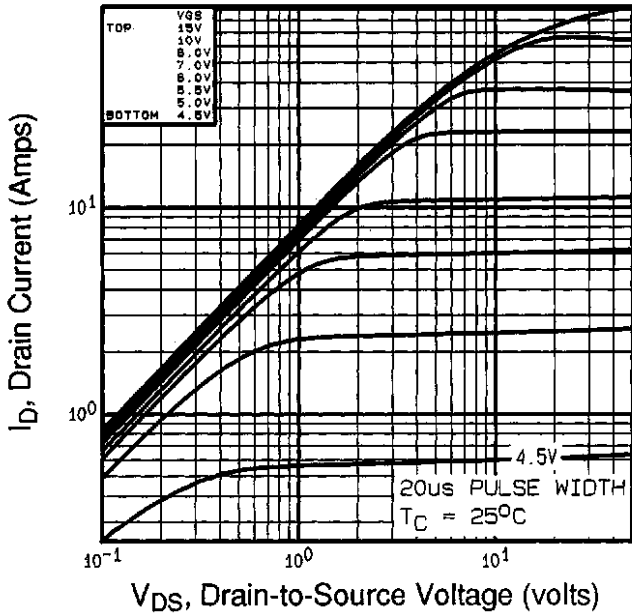
Notes:

① Repetitive rating; pulse width limited by max. junction temperature

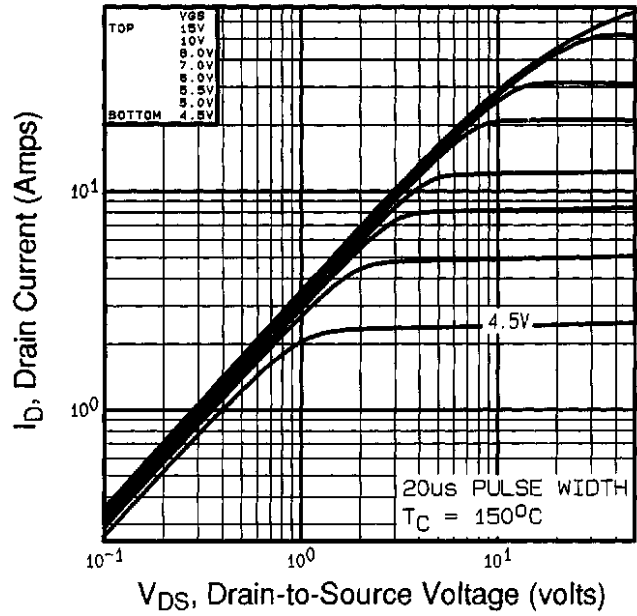
③  $I_{SD} \leq 18A, di/dt \leq 150A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$

②  $V_{DD}=50V, \text{starting } T_J=25^\circ\text{C}, L=2.0\text{mH}, R_G=25\Omega, I_{AS}=18A$

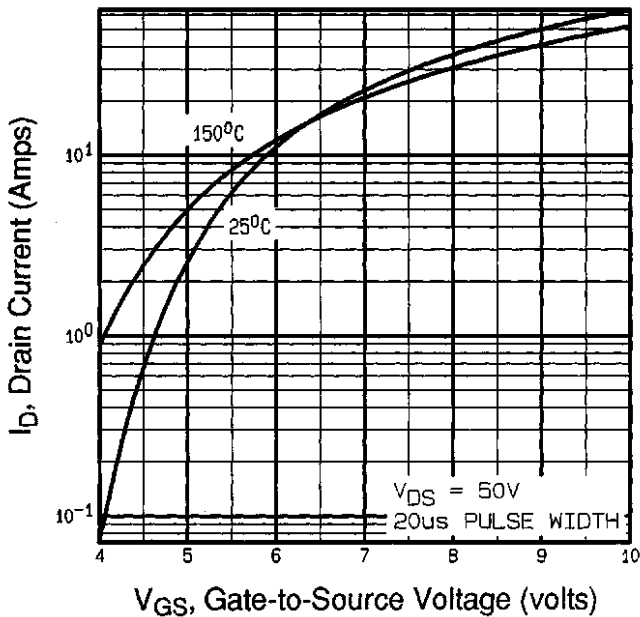
④ Pulse width  $\leq 300 \mu s$ ; duty cycle  $\leq 2\%$ .



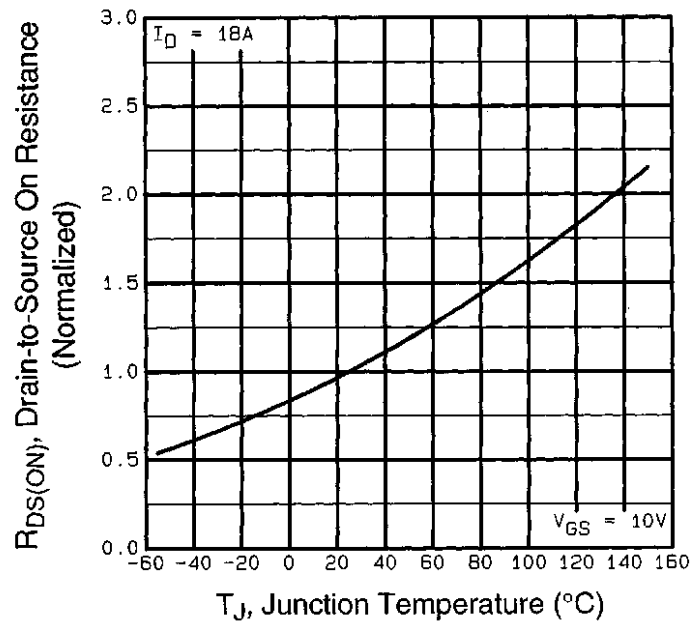
**Fig 1.** Typical Output Characteristics,  $T_C=25^\circ\text{C}$



**Fig 2.** Typical Output Characteristics,  $T_C=150^\circ\text{C}$

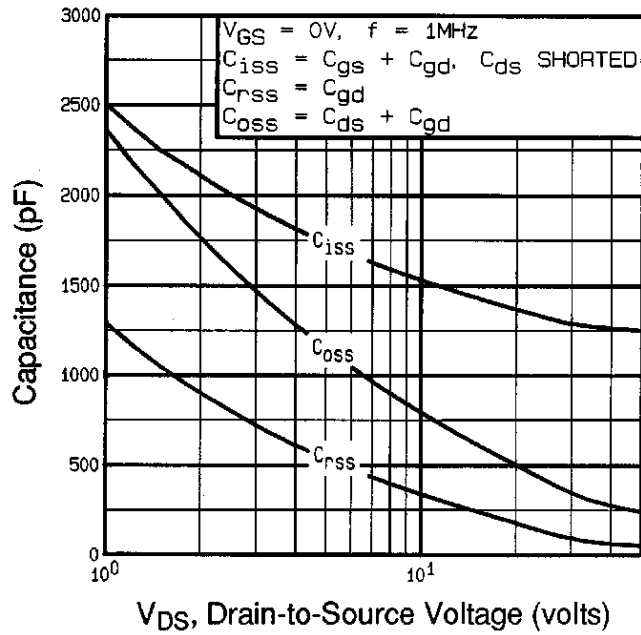


**Fig 3.** Typical Transfer Characteristics

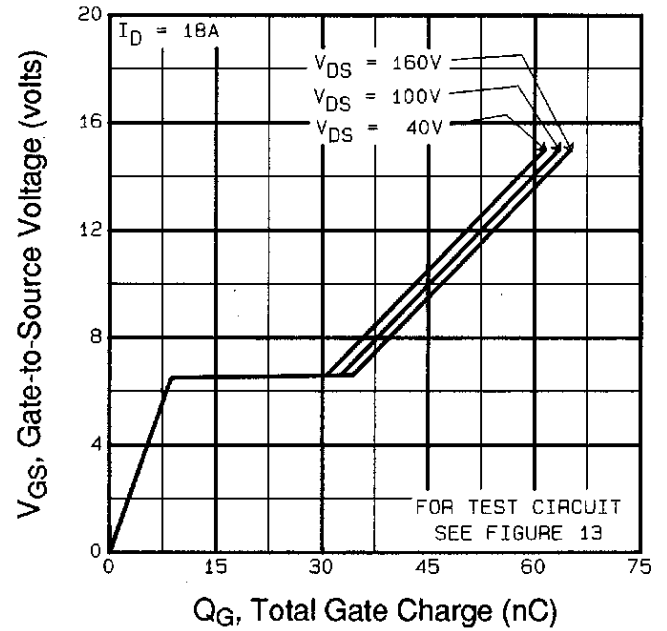


**Fig 4.** Normalized On-Resistance Vs. Temperature

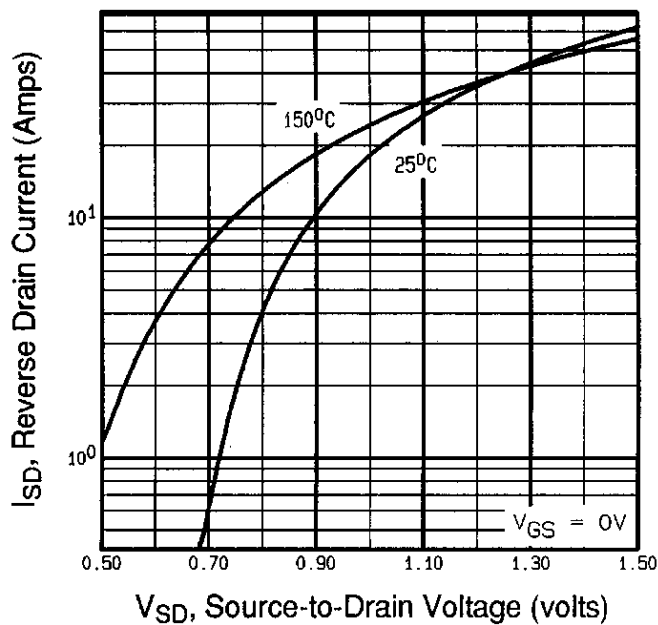
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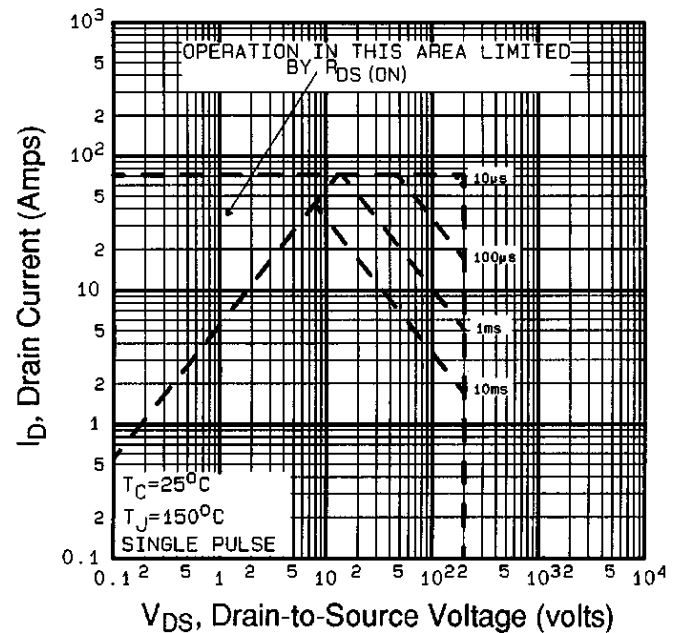
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area

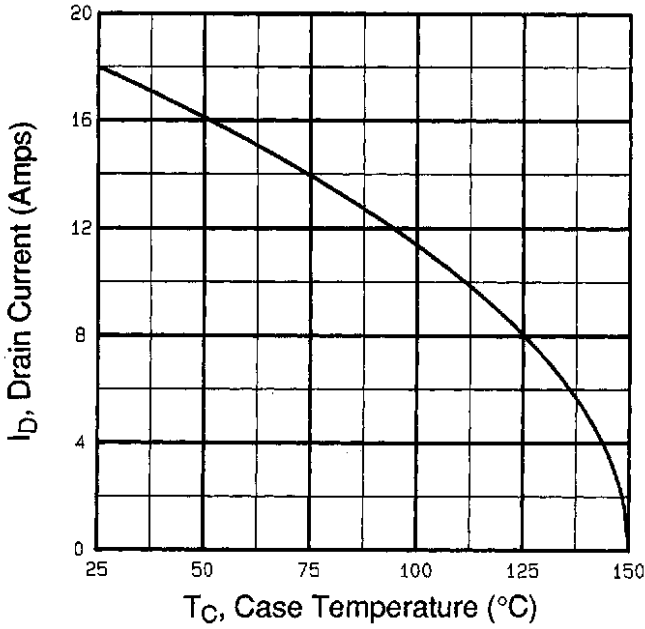


Fig 9. Maximum Drain Current Vs. Case Temperature

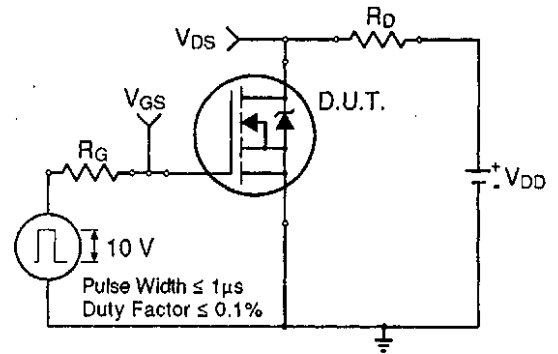


Fig 10a. Switching Time Test Circuit

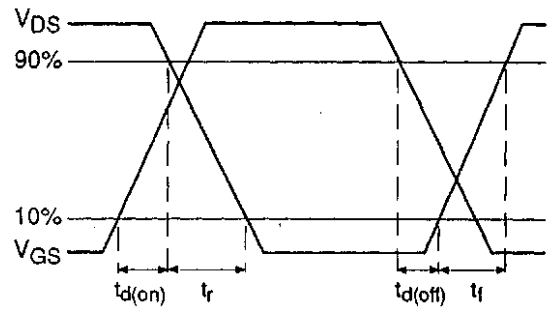


Fig 10b. Switching Time Waveforms

DATA SHEETS

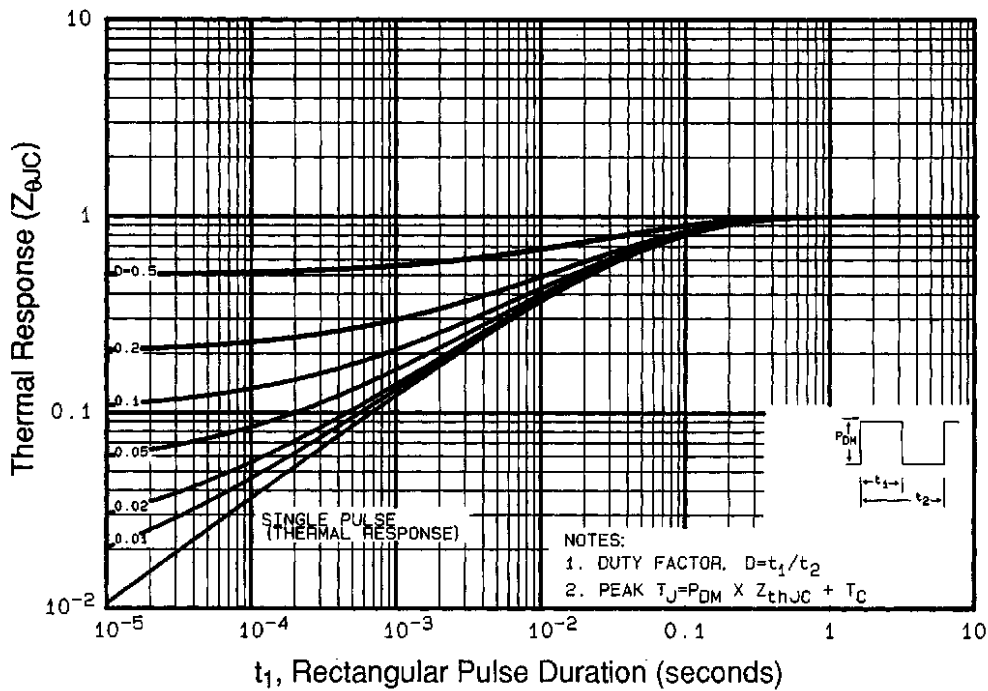
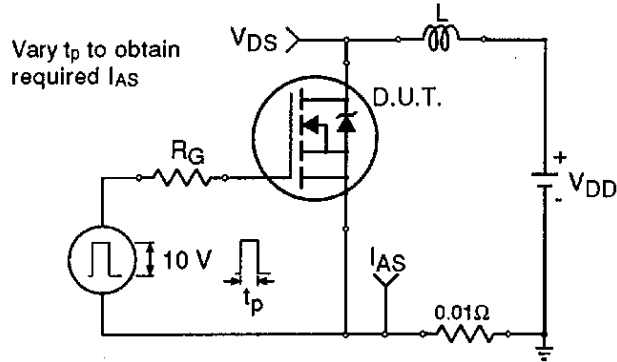
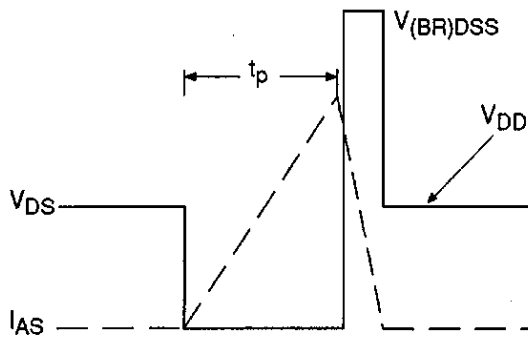


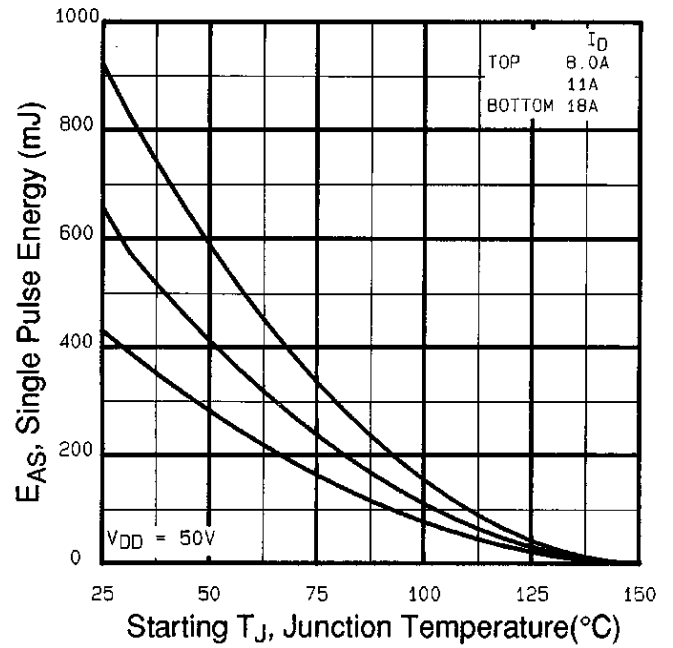
Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case



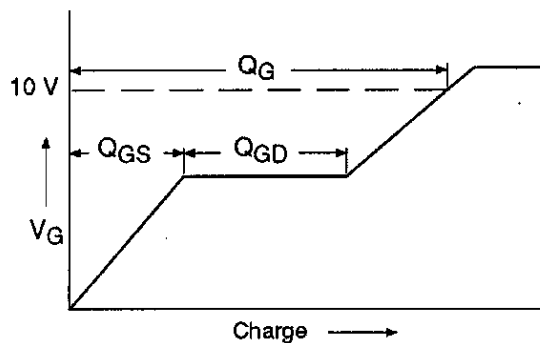
**Fig 12a.** Unclamped Inductive Test Circuit



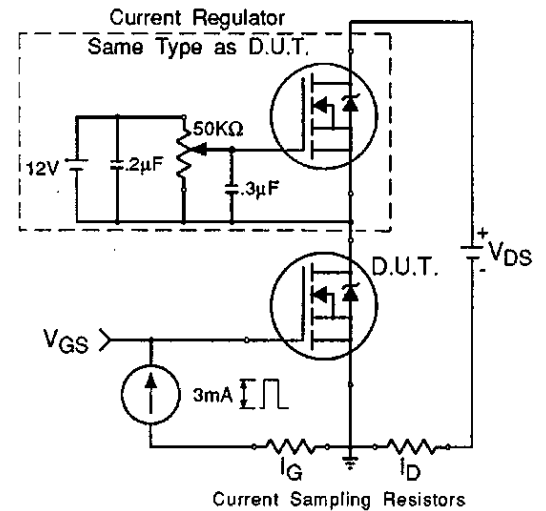
**Fig 12b.** Unclamped Inductive Waveforms



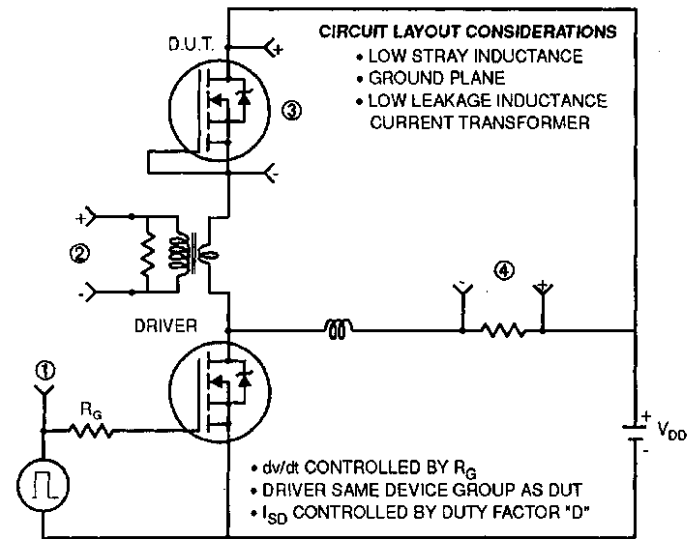
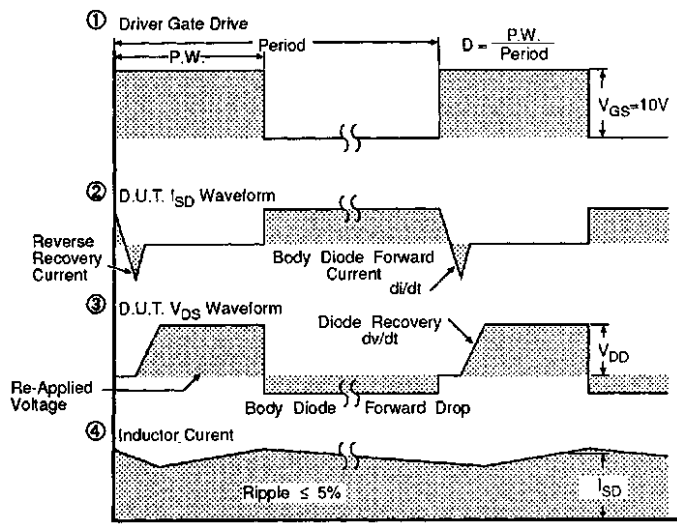
**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit



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Fig 14. Peak Diode Recovery dv/dt Test Circuit

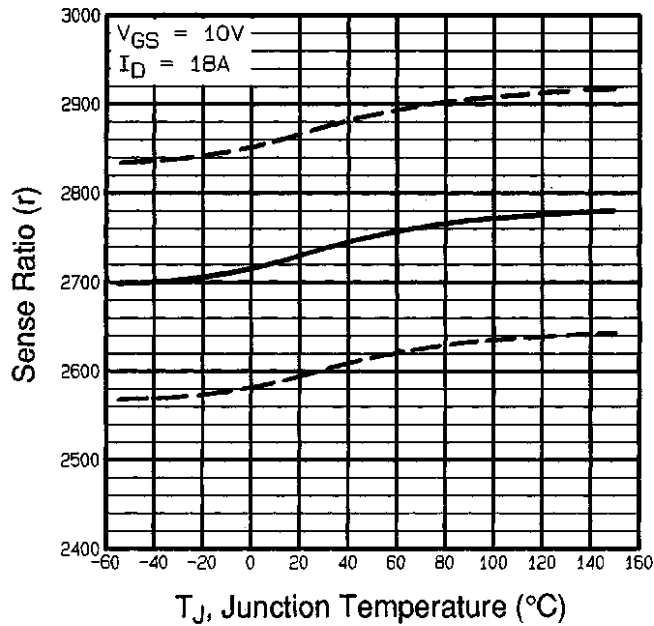


Fig 15. Typical HEXSense Ratio Vs. Junction Temperature

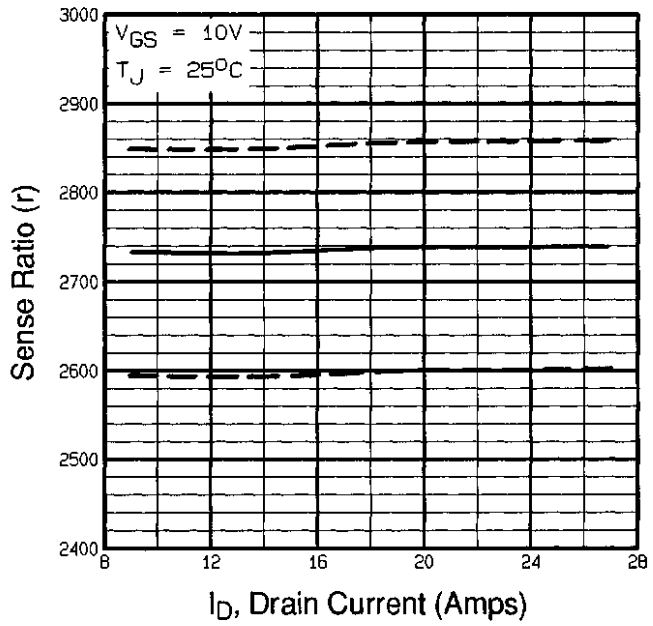
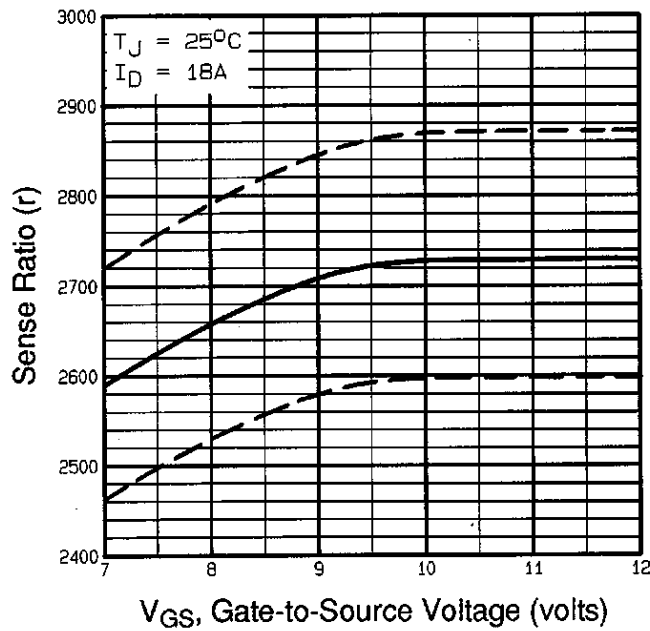
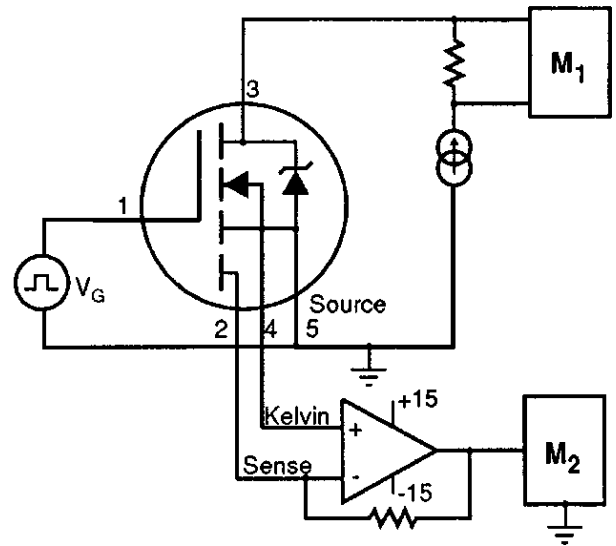


Fig 16. Typical HEXSense Ratio Vs. Drain Current

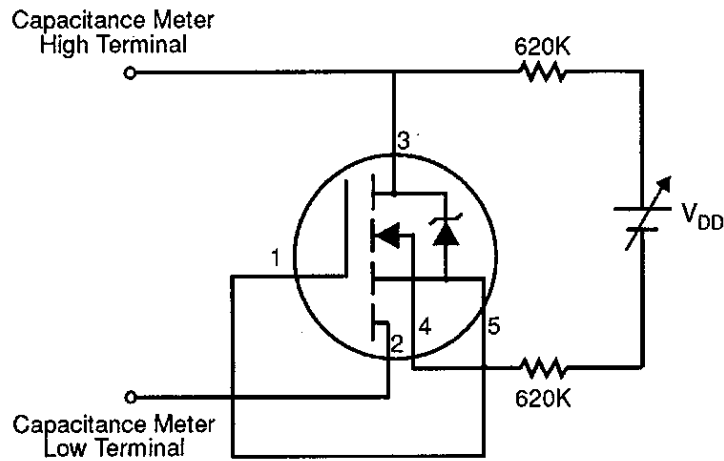


**Fig 17.** Typical HEXSense Ratio Vs. Gate Voltage



M1, M2 = HIGH SPEED DIGITAL VOLTMETERS

**Fig 18.** HEXSense Ratio Test Circuit



**Fig 19.** HEXSense Sensing Cell Output Capacitance Test Circuit

**Appendix B:** Package Outline Mechanical Drawing – See page 1510

**Appendix C:** Part Marking Information – See page 1517