FAIRCHILD
SEMICONDUCTOR®

RFD8P05, RFD8P05SM, RFP8P05

Data Sheet January 2002

8A, 50V, 0.300 Ohm, P-Channel Power MOSFETs

These products are P-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA09832.

Ordering Information

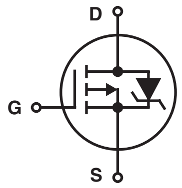
PART NUMBER	PACKAGE	BRAND
RFD8P05	TO-251AA	D8P05
RFD8P05SM	TO-252AA	D8P05
RFP8P05	TO-220AB	RFP8P05

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in tape and reel, i.e., RFD8P05SM9A.

Features

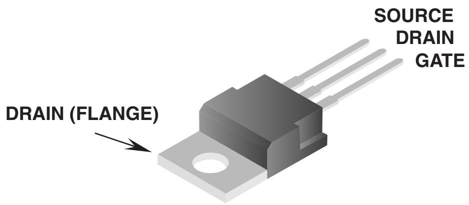
- 8A, 50V
- $r_{DS(ON)} = 0.300\Omega$
- UIS SOA Rating Curve
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

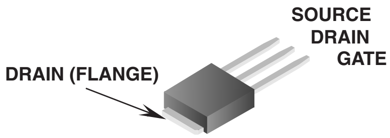


Packaging

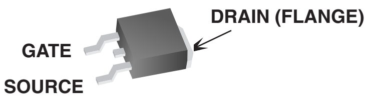
JEDEC TO-220AB



JEDEC TO-251AA



JEDEC TO-252AA



Absolute Maximum Ratings $T_C = 25^oC$ Unless Otherwise Specified

		RFD8P05, RFD8P05SM, RFP8P05	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	-50	V
Drain to Gate Voltage (R_{GS} = 20KΩ) (Note 1)	V_{DGR}	-50	V
Continuous Drain Current	I_D	-8	A
Pulsed Drain Current (Note 3)	I_{DM}	-20	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	48	W
Dissipation Derating Factor		0.27	W/^{o}C
Single Pulse Avalanche Energy Rating	E_{AS}	See Figure 6	
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^{o}C
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^{o}C
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$ Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 9)	-50	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA (Figure 8)	-2	-	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, T_J = 150^{o}C	-	-	25	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 8A, V_{GS} = -10V (Figure 7)	-	-	0.300	Ω
Turn-On Time	t_{ON}	V_{DD} = -25V, I_D ≈ 4A, R_G = 9.1Ω, R_L = 6.25Ω, V_{GS} = -10V	-	-	60	ns
Turn-On Delay Time	$t_{d(ON)}$		-	16	-	ns
Rise Time	t_r		-	30	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	42	-	ns
Fall Time	t_f		-	20	-	ns
Turn-Off Time	t_{OFF}		-	-	100	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0 to -20V V_{DD} = -40V, I_D = 8A,R_L = 5Ω, $I_{G(REF)}$ = -0.3mA	-	-	80	nC
Gate Charge at -5V	$Q_{g(-10)}$	V_{GS} = 0 to -10V	-	-	40	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0 to -2V	-	-	2	nC
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	3.125	^{o}C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-251AA, TO-252AA	-	-	100	^{o}C/W
		TO-220AB			62.5	^{o}C/W

Source to Drain Diode Specifications $T_C = 25^oC$ Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = -8A	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = -8A, dI_{SD}/dt = 100A/μs	-	-	125	ns

NOTE:

2. Pulse test: pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: pulse width is limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

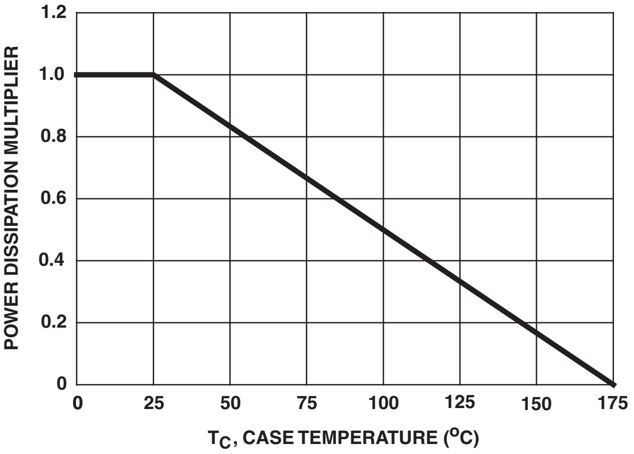


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

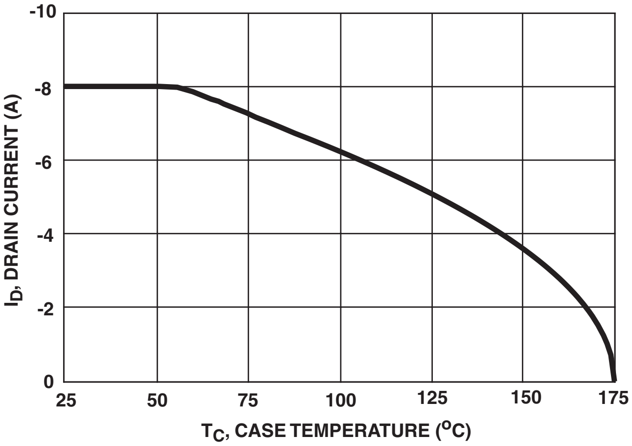


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

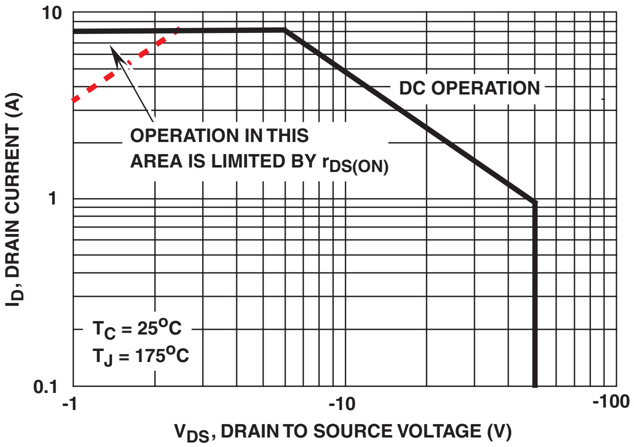


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

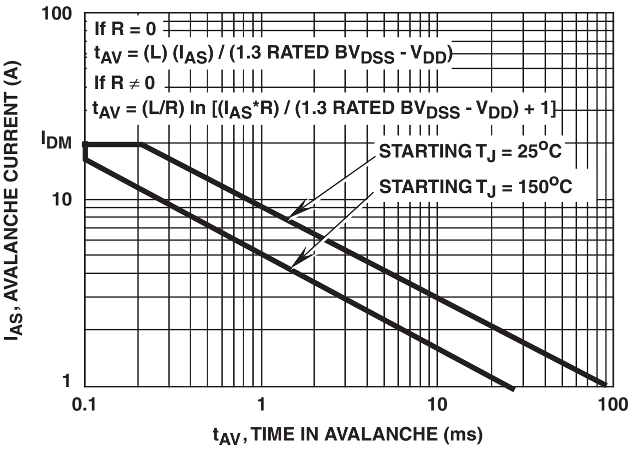


FIGURE 4. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

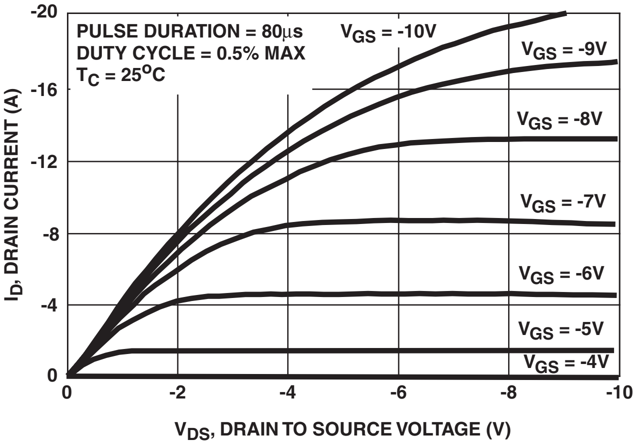


FIGURE 5. SATURATION CHARACTERISTICS

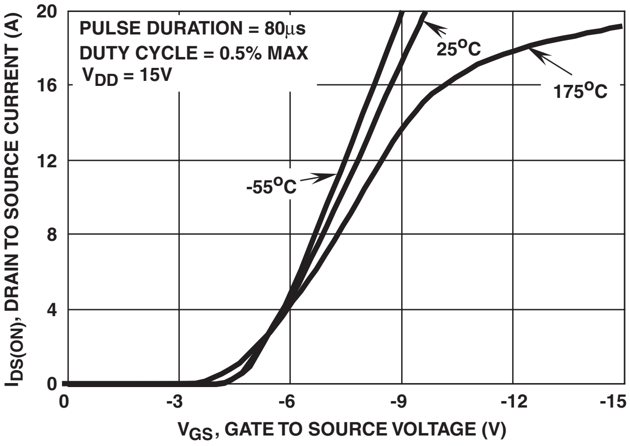


FIGURE 6. TRANSFER CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified

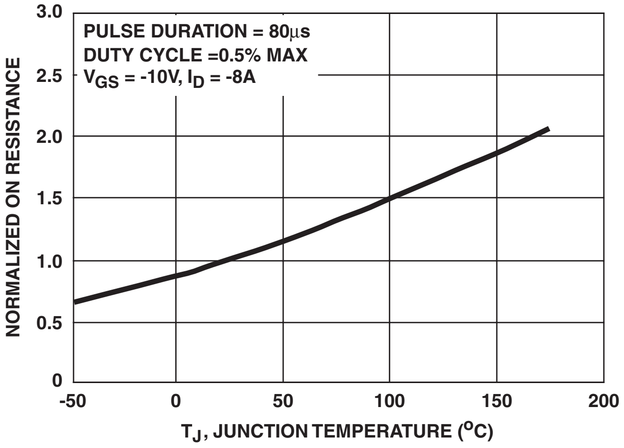


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

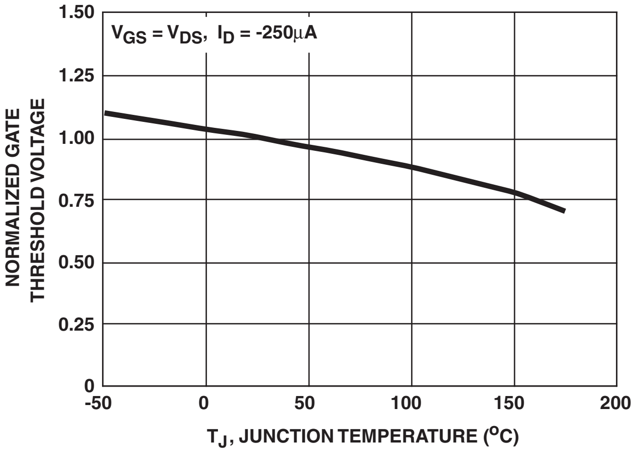


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

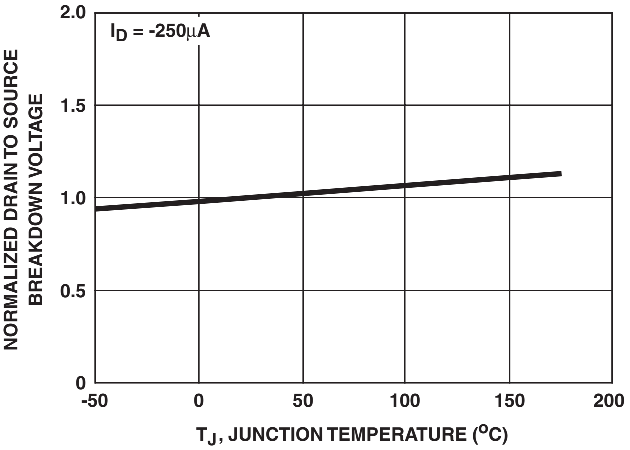


FIGURE 9. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

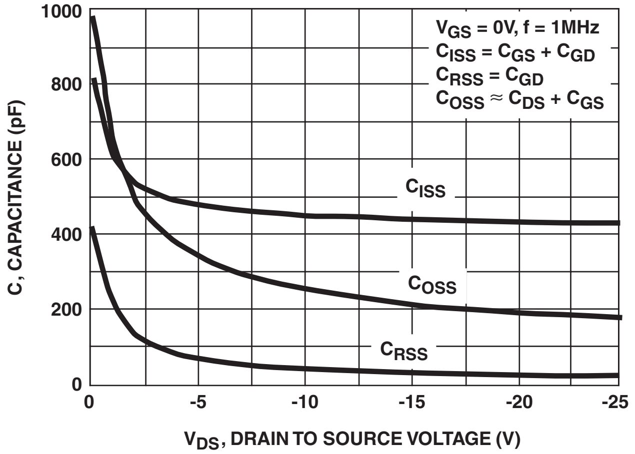
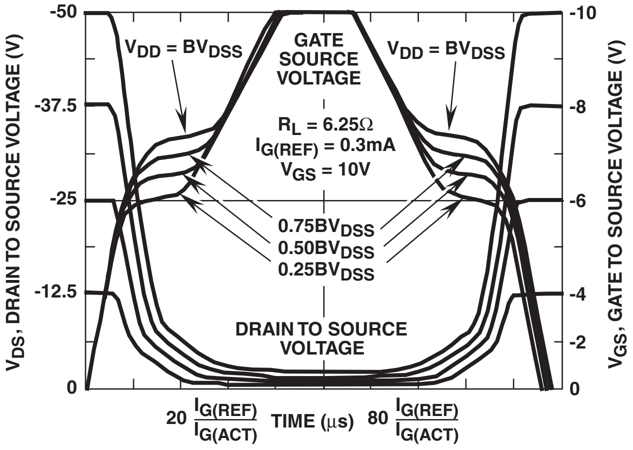


FIGURE 10. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Application Notes AN7254 and AN7260.

FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

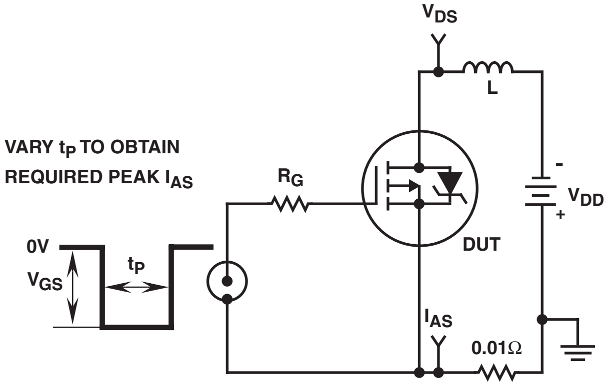


FIGURE 12. UNCLAMPED ENERGY TEST CIRCUIT

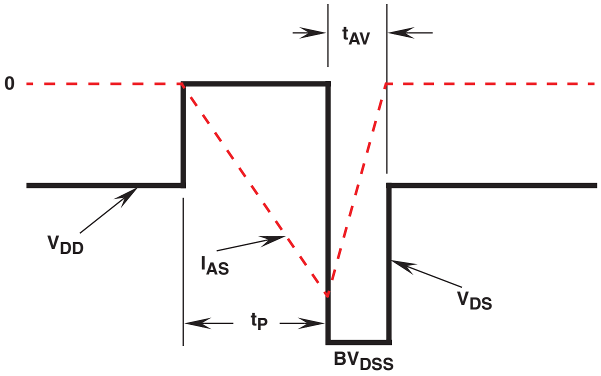


FIGURE 13. UNCLAMPED ENERGY WAVEFORMS

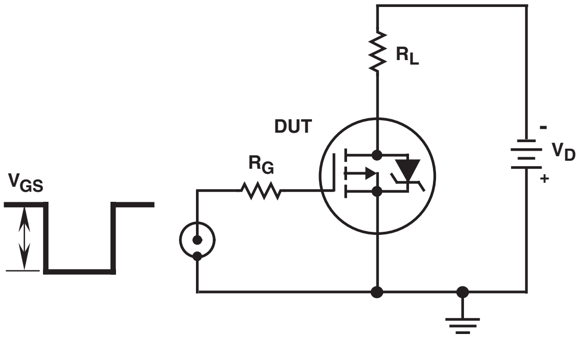


FIGURE 14. SWITCHING TIME TEST CIRCUIT

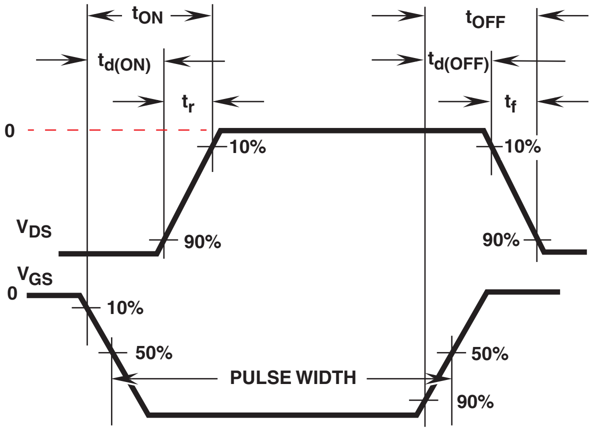


FIGURE 15. RESISTIVE SWITCHING WAVEFORMS

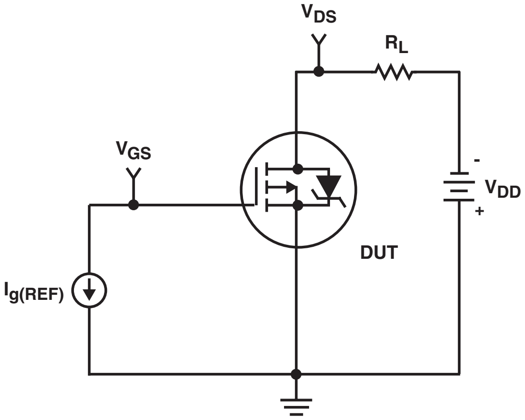


FIGURE 16. GATE CHARGE TEST CIRCUIT

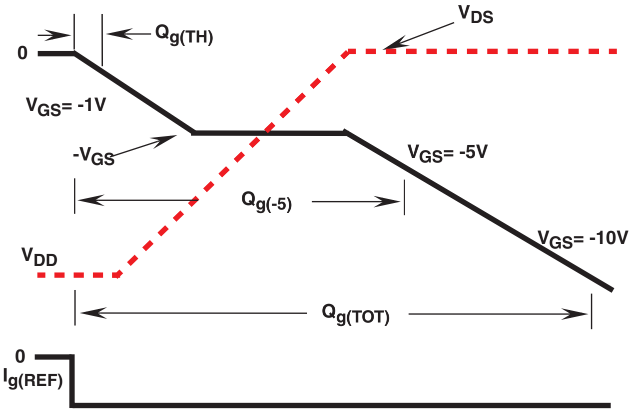


FIGURE 17. GATE CHARGE WAVEFORMS

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