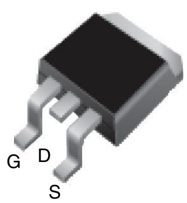
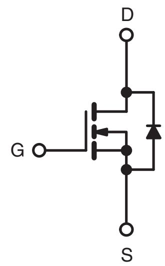
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	100	
$R_{DS(on)}$ (Ω)	V_{GS} = 5.0 V	0.16
Q_g (Max.) (nC)	28	
Q_{gs} (nC)	3.8	
Q_{gd} (nC)	14	
Configuration	Single	

D²PAK (TO-263)





N-Channel MOSFET

FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Logic Level Gate Drive
- $R_{DS(on)}$ Specified at V_{GS} = 4 V and 5 V
- 175 °C Operating Temperature
- Compliant to RoHS Directive 2002/95/EC

Pb Available
RoHS* COMPLIANT
HALOGEN FREE Available

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK (TO-263) is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on resistance in any existing surface mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

ORDERING INFORMATION		
Package	D²PAK (TO-263)	D²PAK (TO-263)
Lead (Pb)-free and Halogen-free	-	SiHL530STRR-GE3[a]
Lead (Pb)-free	-	IRL530STRRPbF[a]
	-	SiHL530STR-E3[a]
SnPb	IRL530S	-
	SiHL530S	-

Note
a. See device orientation.

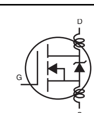
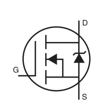
ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage			V_{DS}	100	V
Gate-Source Voltage			V_{GS}	± 10	
Continuous Drain Current	V_{GS} at 5 V	T_C = 25 °C	I_D	15	A
		T_C = 100 °C		11	
Pulsed Drain Current[a]			I_{DM}	60	
Linear Derating Factor				0.59	W/°C
Linear Derating Factor (PCB Mount)[e]				0.025	
Single Pulse Avalanche Energy[b]			E_{AS}	290	mJ
Repetitive Avalanche Current[a]			I_{AR}	15	A
Repetitive Avalanche Energy[a]			E_{AR}	8.8	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	88	W
Maximum Power Dissipation (PCB Mount)[e]	T_A = 25 °C			3.7	
Peak Diode Recovery dV/dt[c]			dV/dt	5.5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = 25 V, starting T_J = 25 °C, L = 1.9 mH, R_g = 25 Ω, I_{AS} = 15 A (see fig. 12).
c. $I_{SD} \le 15$ A, dI/dt ≤ 140 A/μs, $V_{DD} \le V_{DS}$, $T_J \le 175$ °C.
d. 1.6 mm from case.
e. When mounted on 1" square PCB (FR-4 or G-10 material).

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to Ambient (PCB	R_{thJA}	-	40	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.7	

Note
a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	100	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.14	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.0	-	2.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 10 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	-	-	25	μA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 150 °C	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 5.0 V, I_D = 9.0 A[b]	-	-	0.16	Ω
		V_{GS} = 4.0 V, I_D = 7.5 A[b]	-	-	0.22	
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 9.0 A[b]	6.4	-	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	930	-	pF
Output Capacitance	C_{oss}		-	250	-	
Reverse Transfer Capacitance	C_{rss}		-	57	-	
Total Gate Charge	Q_g	V_{GS} = 5.0 V, I_D = 15 A, V_{DS} = 80 V, see fig. 6 and 13[b]	-	-	28	nC
Gate-Source Charge	Q_{gs}		-	-	3.8	
Gate-Drain Charge	Q_{gd}		-	-	14	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50 V, I_D = 15 A, R_g = 12 Ω, R_D = 32 Ω, see fig. 10[b]	-	4.7	-	ns
Rise Time	t_r		-	100	-	
Turn-Off Delay Time	$t_{d(off)}$		-	22	-	
Fall Time	t_f		-	48	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	15	A
Pulsed Diode Forward Current[a]	I_{SM}		-	-	60	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 15 A, V_{GS} = 0 V[b]	-	-	2.5	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 15 A, dI/dt = 100 A/μs[b]	-	150	200	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	0.93	1.4	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

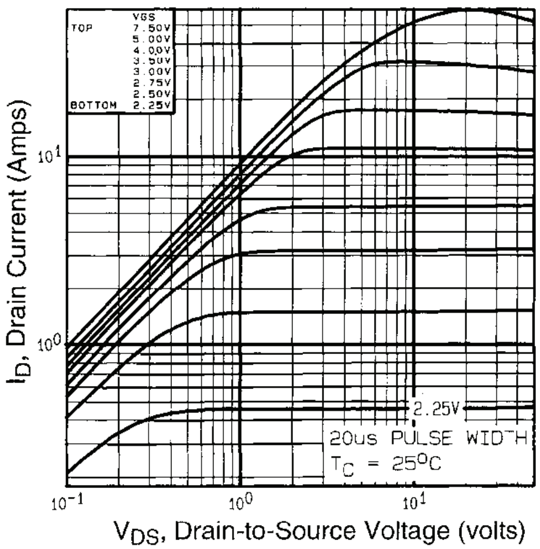


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

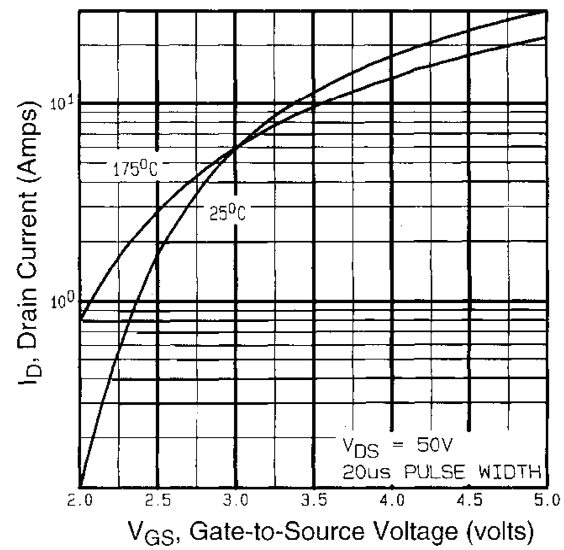


Fig. 3 - Typical Transfer Characteristics

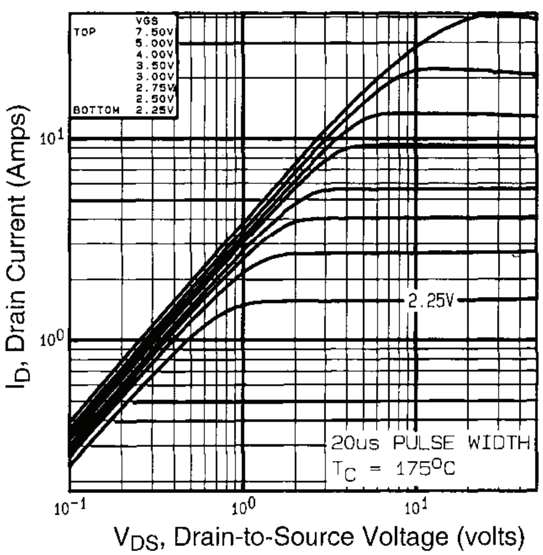


Fig. 2 - Typical Output Characteristics, T_C = 175 °C

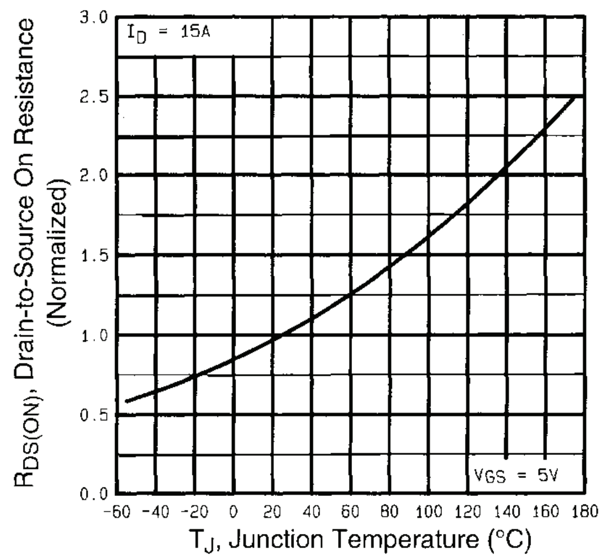


Fig. 4 - Normalized On-Resistance vs. Temperature

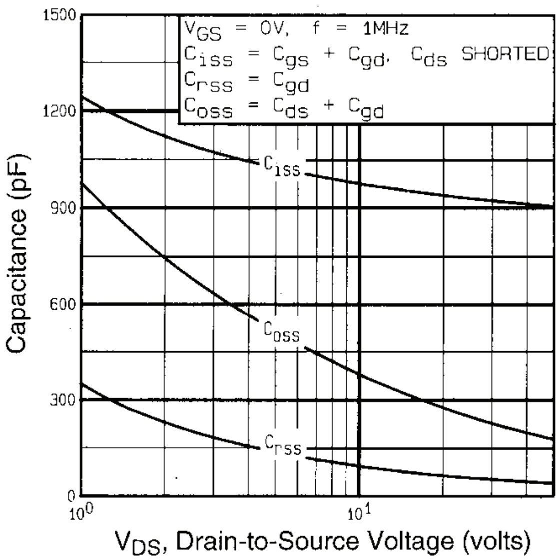


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

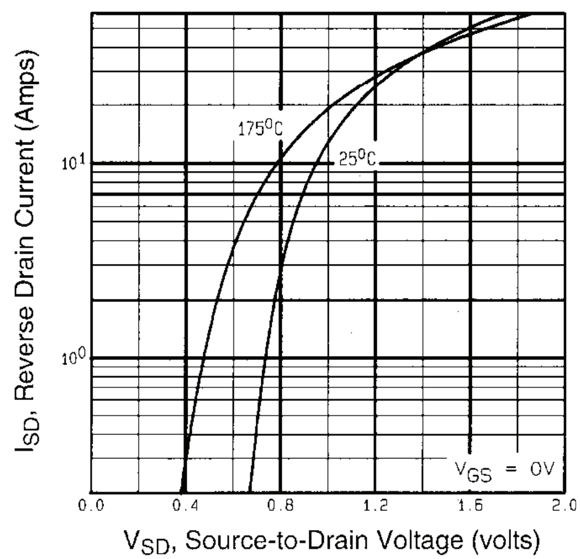


Fig. 7 - Typical Source-Drain Diode Forward Voltage

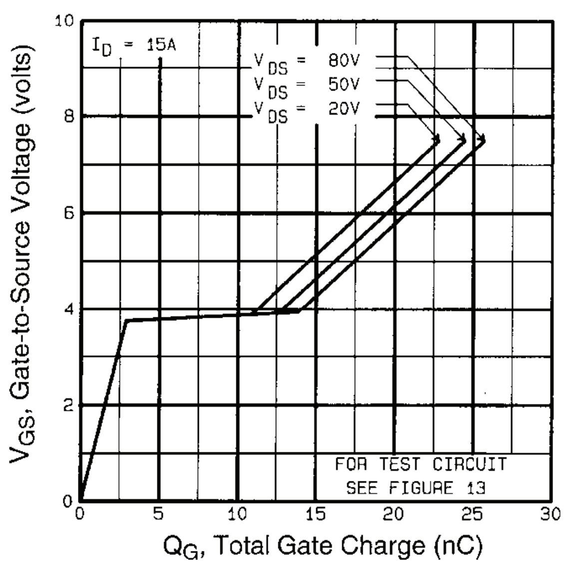


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

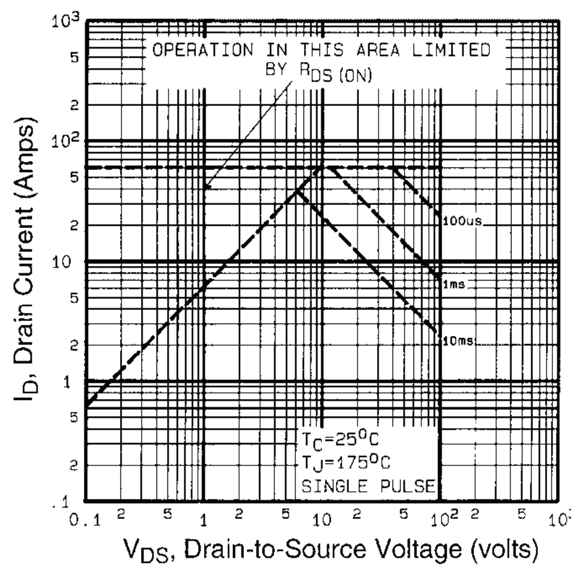


Fig. 8 - Maximum Safe Operating Area

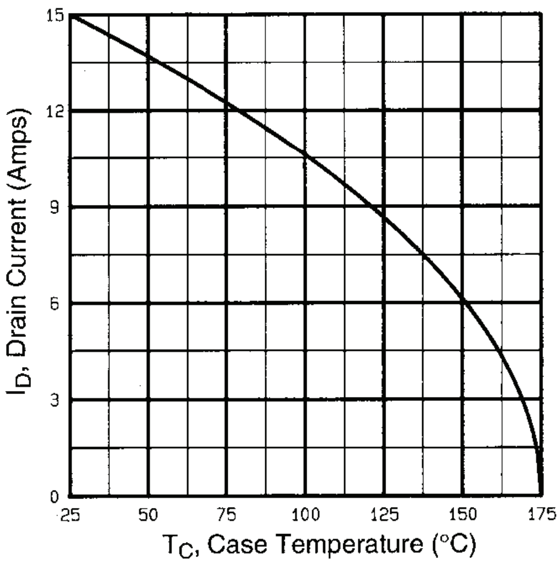


Fig. 9 - Maximum Drain Current vs. Case Temperature

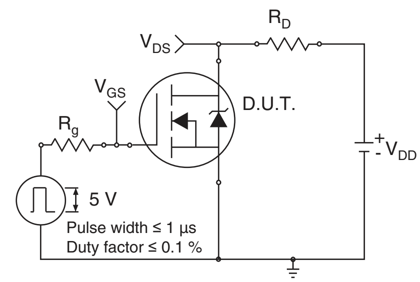


Fig. 10a - Switching Time Test Circuit

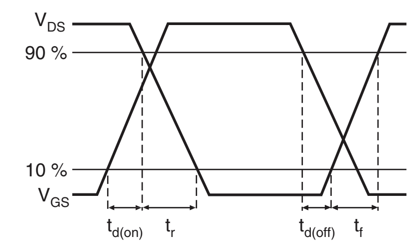


Fig. 10b - Switching Time Waveforms

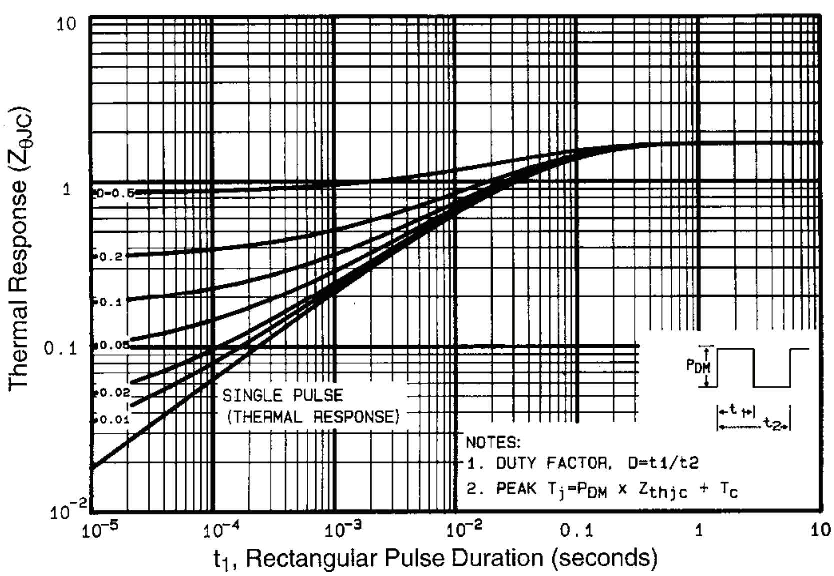


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

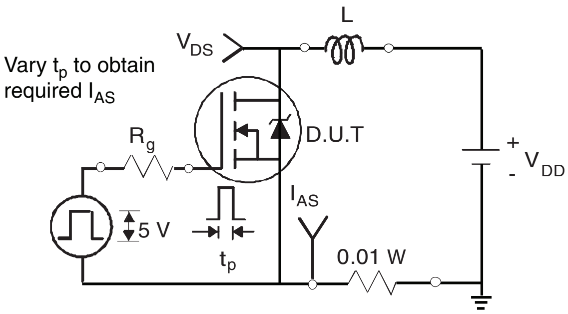


Fig. 12a - Unclamped Inductive Test Circuit

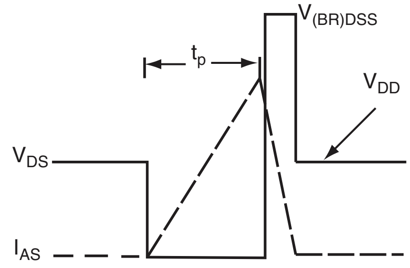


Fig. 12b - Unclamped Inductive Waveforms

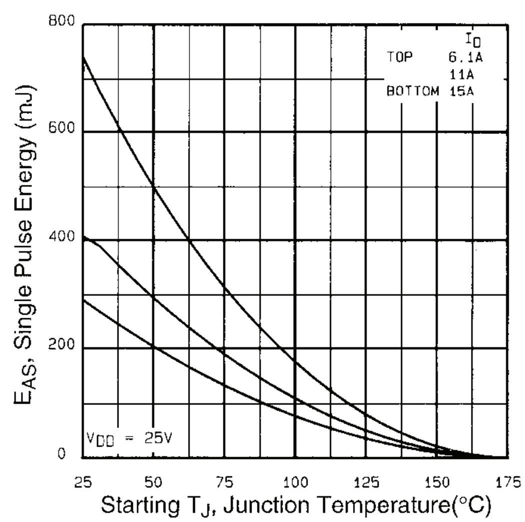


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

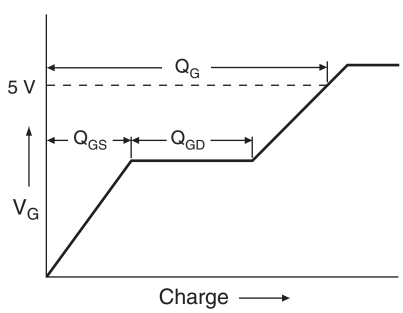


Fig. 13a - Basic Gate Charge Waveform

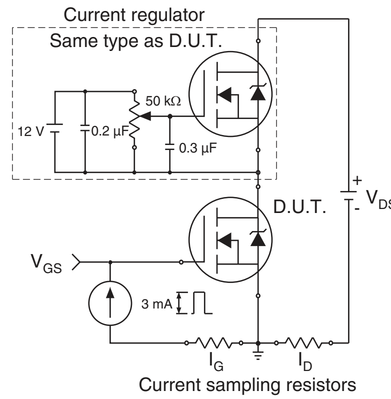
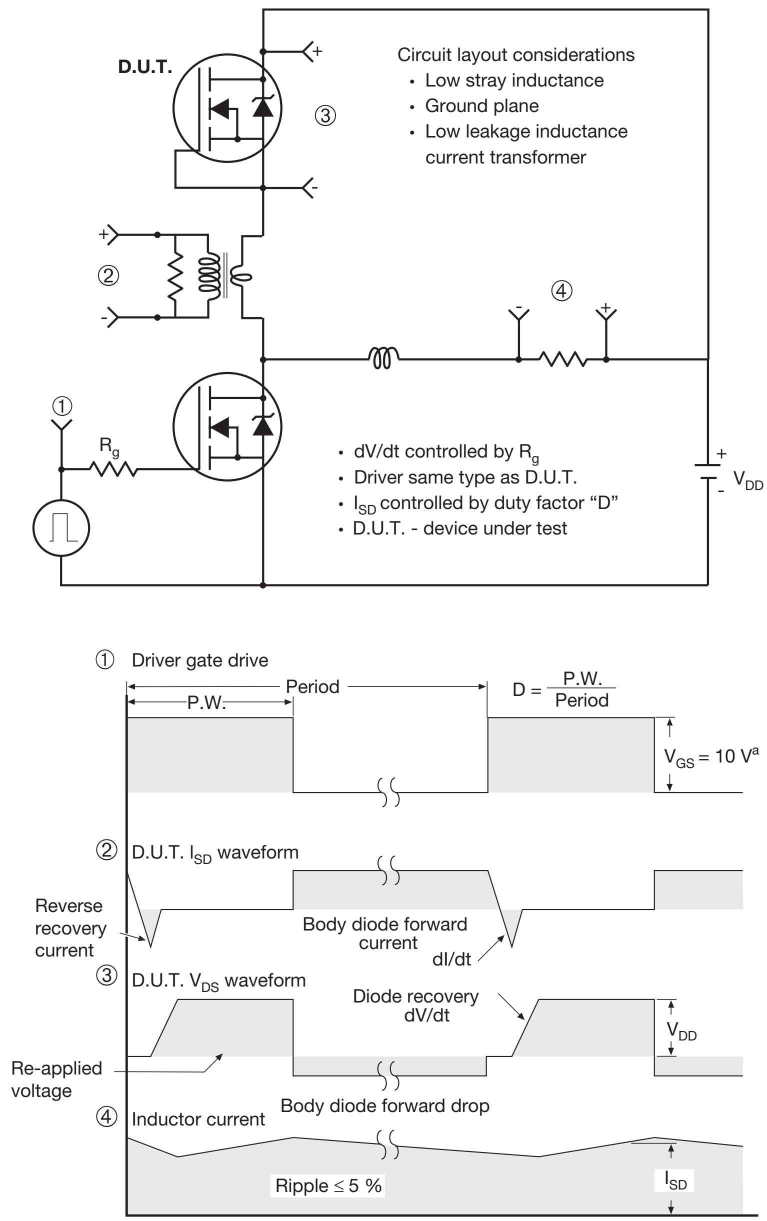


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

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