

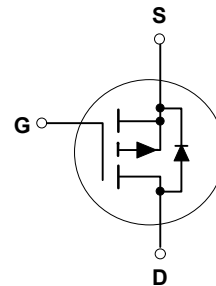
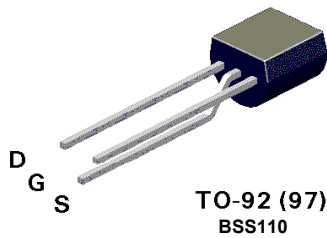
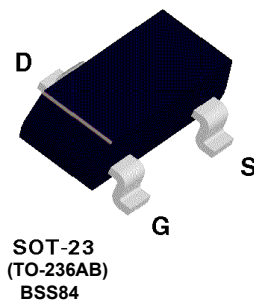
BSS84 / BSS110 P-Channel Enhancement Mode Field Effect Transistor

General Description

These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is designed to minimize on-state resistance, provide rugged and reliable performance and fast switching. They can be used, with a minimum of effort, in most applications requiring up to 0.17A DC and can deliver pulsed currents up to 0.68A. This product is particularly suited to low voltage applications requiring a low current high side switch.

Features

- BSS84: -0.13A, -50V. $R_{DS(ON)} = 10\Omega @ V_{GS} = -5V$.
BSS110: -0.17A, -50V. $R_{DS(ON)} = 10\Omega @ V_{GS} = -10V$
- Voltage controlled p-channel small signal switch.
- High density cell design for low $R_{DS(ON)}$.
- High saturation current.



Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	BSS84	BSS110	Units
V_{DSS}	Drain-Source Voltage		-50	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 20\text{ K}\Omega$)		-50	V
V_{GSS}	Gate-Source Voltage - Continuous		± 20	V
I_D	Drain Current - Continuous @ $T_A = 30/35^\circ\text{C}$	-0.13	-0.17	A
	- Pulsed @ $T_A = 25^\circ\text{C}$	-0.52	-0.68	
P_D	Maximum Power Dissipation $T_A = 25^\circ\text{C}$	0.36	0.63	W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/16" from case for 10 seconds		300	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Symbol	Parameter	BSS84	BSS110	Units
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	350	200	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	All	-50			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -50\text{ V},$ $V_{GS} = 0\text{ V}$	All			-15	μA
						-60	μA
		$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V}$			-0.1	μA	
I_{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	All			-10	nA
ON CHARACTERISTICS (Note 1)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -1\text{ mA}$	All	-0.8	-1.75	-2	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -5\text{ V}, I_D = -0.10\text{ A}$	BSS84		3.2	10	Ω
		$V_{GS} = -10\text{ V}, I_D = -0.17\text{ A}$	BSS110		2.2	10	
g_{FS}	Forward Transconductance	$V_{DS} = -25\text{ V}, I_D = -0.10\text{ A}$	BSS84	0.05	0.27		S
		$V_{DS} = -10\text{ V}, I_D = -0.17\text{ A}$	BSS110	0.05	0.29		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	BSS84		37	45	pF
			BSS110		37	40	
C_{oss}	Output Capacitance		All		16	25	pF
C_{rss}	Reverse Transfer Capacitance		All		5	12	pF
SWITCHING CHARACTERISTICS (Note 1)							
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = -30\text{ V}, I_D = -0.27\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 50\ \Omega$	All			12	nS
t_r	Turn - On Rise Time		All			50	nS
$t_{D(off)}$	Turn - Off Delay Time		All			10	nS
t_f	Turn - Off Fall Time		All			25	nS
DRAIN-SOURCE DIODE CHARACTERISTICS							
I_S	Continuous Source Diode Current		BSS84			-0.13	A
			BSS110			-0.17	
I_{SM}	Maximum Pulsed Source Diode Current (Note 1)		BSS84			-0.52	A
			BSS110			-0.68	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -0.26\text{ A}$ (Note 1)	BSS84		-0.95	-1.2	V
		$V_{GS} = 0\text{ V}, I_S = -0.34\text{ A}$ (Note 1)	BSS110		-1	-1.2	

Note:

 1. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Typical Electrical Characteristics

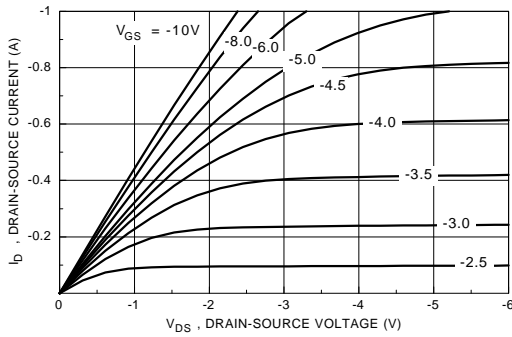


Figure 1. On-Region Characteristics

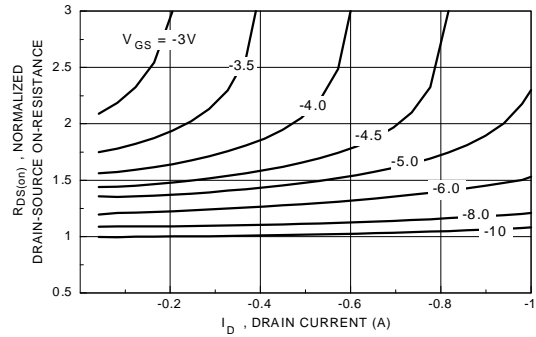


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

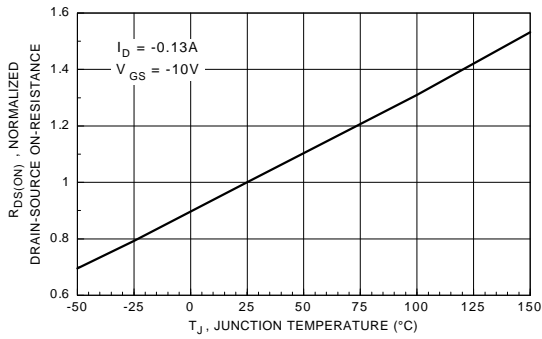


Figure 3. On-Resistance Variation with Temperature

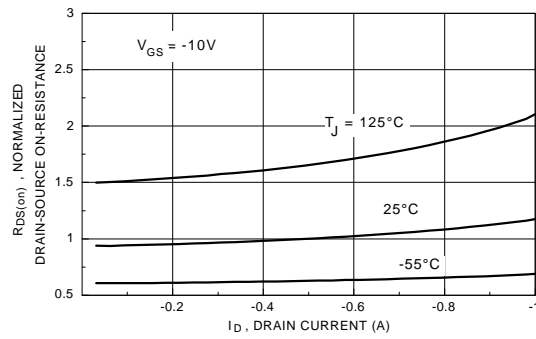


Figure 4. On-Resistance Variation with Drain Current and Temperature

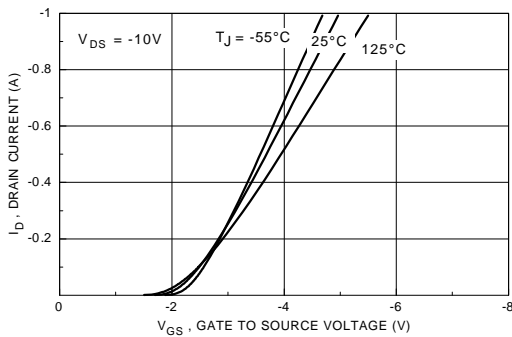


Figure 5. Transfer Characteristics

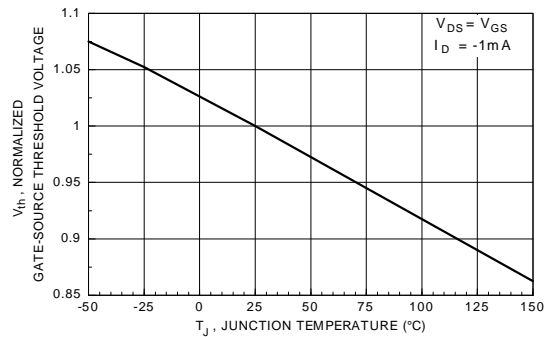


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

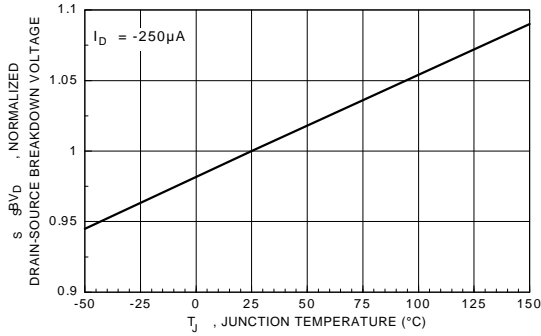


Figure 7. Breakdown Voltage Variation with Temperature

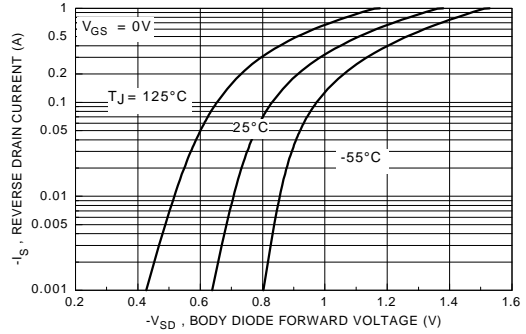


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

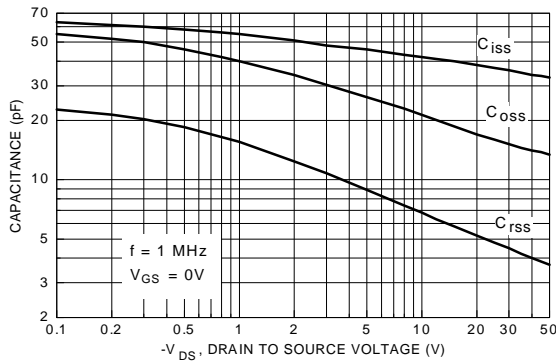


Figure 9. Capacitance Characteristics

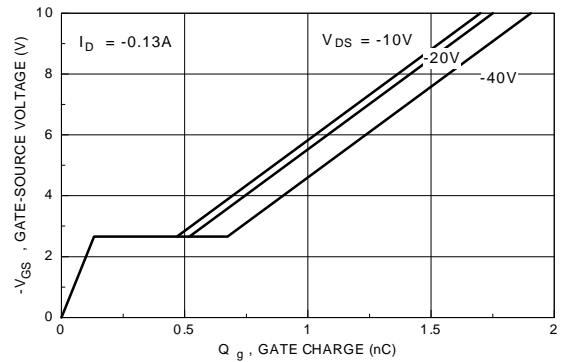


Figure 10. Gate Charge Characteristics

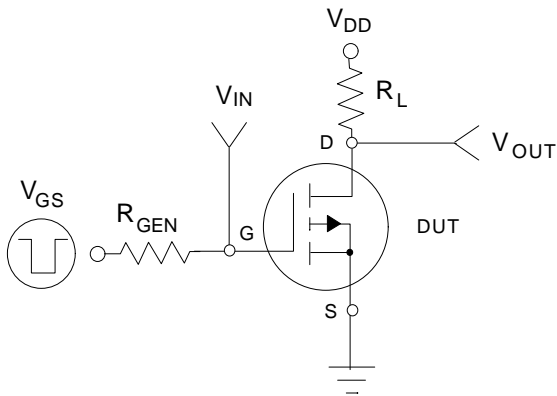


Figure 11. Switching Test Circuit

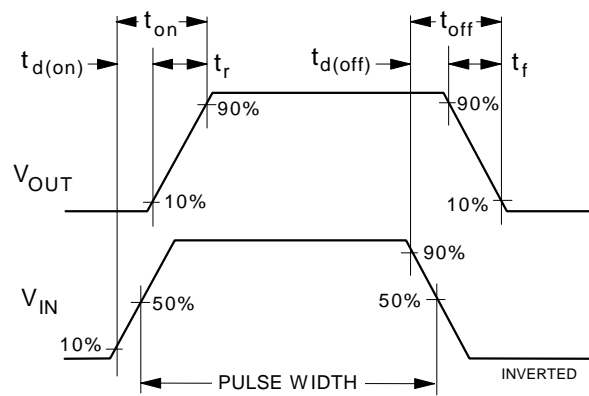


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

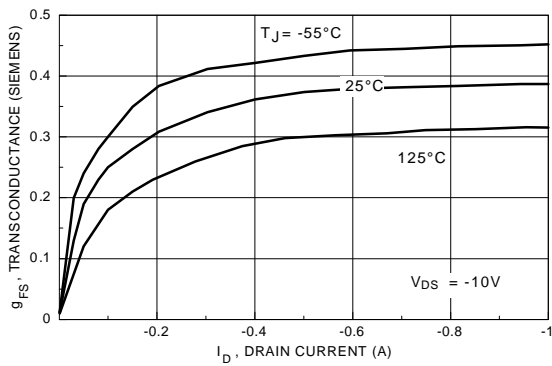


Figure 13. Transconductance Variation with Drain Current and Temperature

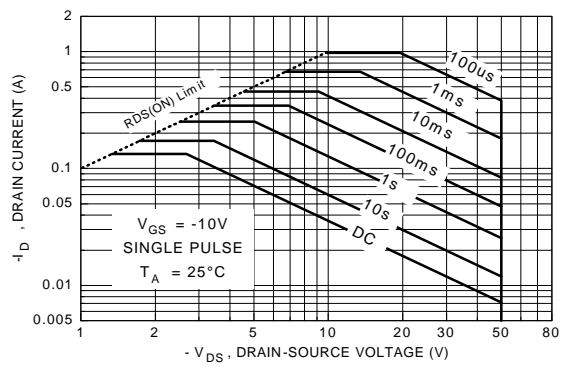


Figure 14. Maximum Safe Operating Area

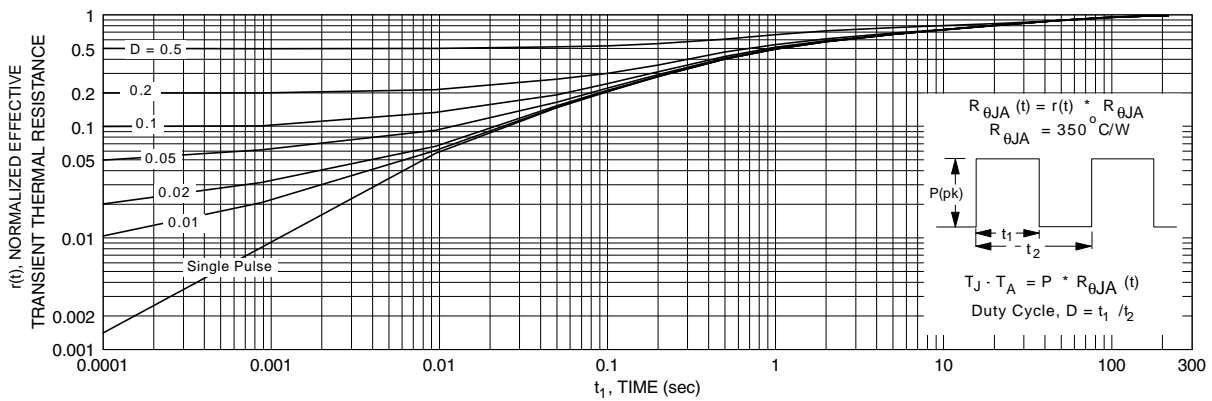


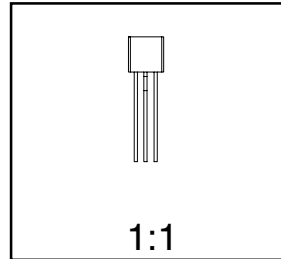
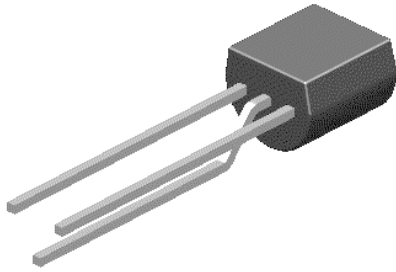
Figure 15. Transient Thermal Response Curve

Note : Characterization performed using a circuit board with 175°C/W typical case-to-ambient thermal resistance.

TO-92 Package Dimensions



TO-92; TO-18 Reverse Lead Form (J35Z Option) (FS PKG Code 92, 94, 96)

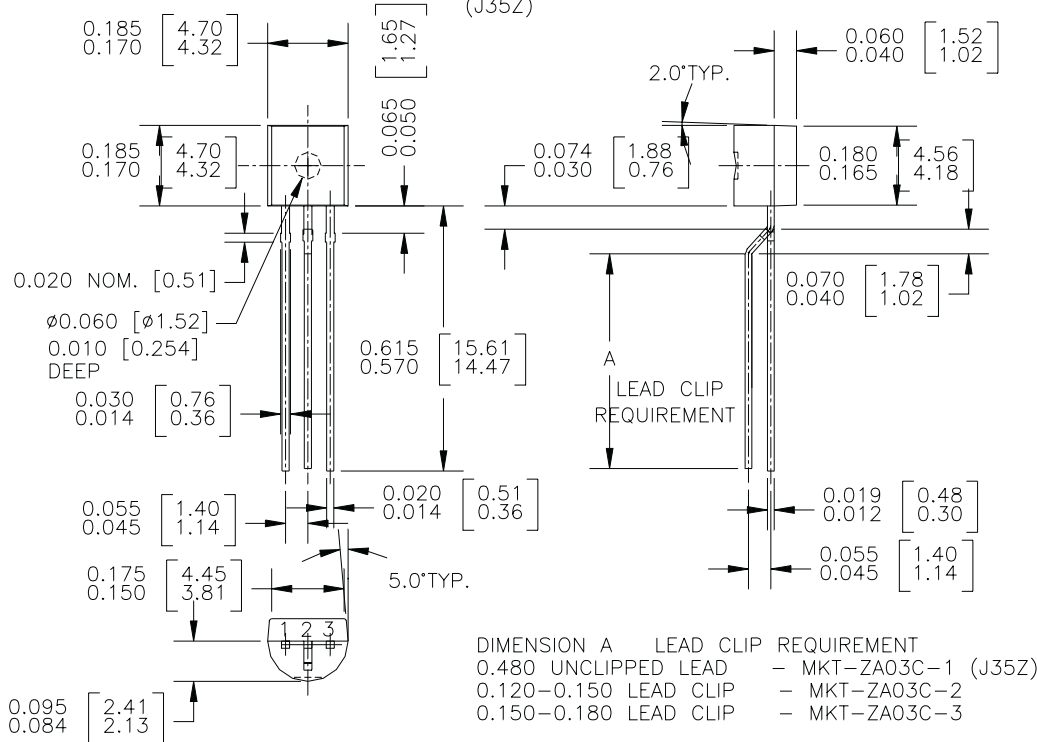


Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.22

TO-92(92,94,96,97*,98*);
TO-18 REVERSE LEADFORM
(J35Z)



Note: All package 97 or 98 transistors are leadformed to this configuration prior to bulk shipment. Order L34Z option if in-line leads are preferred on package 97 or 98.

* Standard Option on 97 & 98 package code

January 2000, Rev. B

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