

# NTD3055-150

## Power MOSFET

### 9.0 A, 60 V, N-Channel DPAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

#### Features

- Pb-Free Packages are Available

#### Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit		
Drain-to-Source Voltage	$V_{DSS}$	60	Vdc		
Drain-to-Gate Voltage ( $R_{GS} = 10\text{ M}\Omega$ )	$V_{DGR}$	60	Vdc		
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	Vdc		
– Continuous		$\pm 30$			
– Non-repetitive ( $t_p \leq 10\text{ ms}$ )					
Drain Current	$I_D$	9.0	Adc		
– Continuous @ $T_A = 25^\circ\text{C}$		3.0			
– Continuous @ $T_A = 100^\circ\text{C}$		27	Apk		
– Single Pulse ( $t_p \leq 10\text{ }\mu\text{s}$ )					
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	28.8	W		
Derate above $25^\circ\text{C}$		0.19	W/ $^\circ\text{C}$		
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1)		2.1	W		
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 2)		1.5	W		
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$		
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$	$E_{AS}$	30	mJ		
( $V_{DD} = 25\text{ Vdc}$ , $V_{GS} = 10\text{ Vdc}$ , $L = 1.0\text{ mH}$ , $I_L(pk) = 7.75\text{ A}$ , $V_{DS} = 60\text{ Vdc}$ )					
Thermal Resistance		$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$		5.2	$^\circ\text{C/W}$
– Junction-to-Case				71.4	
– Junction-to-Ambient (Note 1)	100				
– Junction-to-Ambient (Note 2)					
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	$T_L$	260	$^\circ\text{C}$		

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted to an FR4 board using 0.5 sq in pad size.
2. When surface mounted to an FR4 board using minimum recommended pad size.

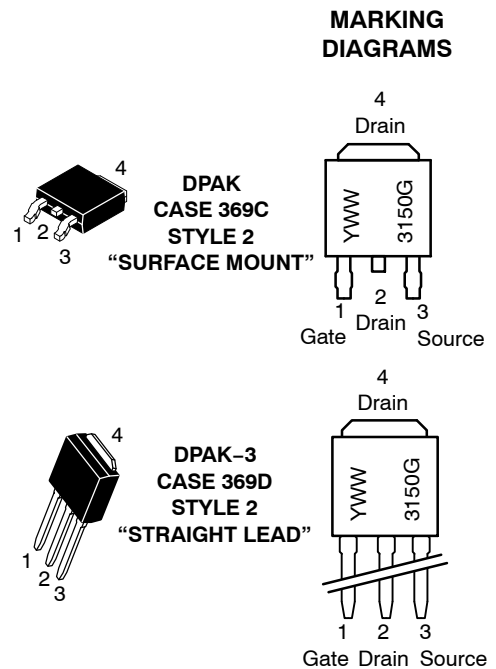
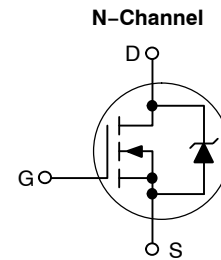


**ON Semiconductor®**

<http://onsemi.com>

**9.0 AMPERES, 60 VOLTS**

**$R_{DS(on)} = 122\text{ m}\Omega$  (Typ)**



3150 = Device Code  
Y = Year  
WW = Work Week  
G = Pb-Free Package

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NTD3055-150

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain-to-Source Breakdown Voltage (Note 3) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	60 -	- 70.2	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	I <sub>DSS</sub>	- -	- -	1.0 10	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	-	-	±100	nAdc

## ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	2.0 -	3.0 6.4	4.0 -	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 4.5 Adc)	R <sub>DS(on)</sub>	-	122	150	mΩ
Static Drain-to-Source On-Voltage (Note 3) (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 9.0 Adc) (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 4.5 Adc, T <sub>J</sub> = 150°C)	V <sub>DS(on)</sub>	- -	1.4 1.1	1.9 -	Vdc
Forward Transconductance (Note 3) (V <sub>DS</sub> = 7.0 Vdc, I <sub>D</sub> = 6.0 Adc)	g <sub>FS</sub>	-	5.4	-	mhos

## DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	-	200	280	pF
Output Capacitance		C <sub>oss</sub>	-	70	100	
Transfer Capacitance		C <sub>rss</sub>	-	26	40	

## SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V <sub>DD</sub> = 48 Vdc, I <sub>D</sub> = 9.0 Adc, V <sub>GS</sub> = 10 Vdc, R <sub>G</sub> = 9.1 Ω) (Note 3)	t <sub>d(on)</sub>	-	11.2	25	ns
Rise Time		t <sub>r</sub>	-	37.1	80	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	12.2	25	
Fall Time		t <sub>f</sub>	-	23	50	
Gate Charge	(V <sub>DS</sub> = 48 Vdc, I <sub>D</sub> = 9.0 Adc, V <sub>GS</sub> = 10 Vdc) (Note 3)	Q <sub>T</sub>	-	7.1	15	nC
		Q <sub>1</sub>	-	1.7	-	
		Q <sub>2</sub>	-	3.5	-	

## SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I <sub>S</sub> = 9.0 Adc, V <sub>GS</sub> = 0 Vdc) (Note 3) (I <sub>S</sub> = 19 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	V <sub>SD</sub>	- -	0.98 0.86	1.20 -	Vdc
Reverse Recovery Time	(I <sub>S</sub> = 9.0 Adc, V <sub>GS</sub> = 0 Vdc, di <sub>S</sub> /dt = 100 A/μs) (Note 3)	t <sub>rr</sub>	-	28.9	-	ns
		t <sub>a</sub>	-	21.6	-	
		t <sub>b</sub>	-	7.3	-	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	-	0.036	-	μC

- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- Switching characteristics are independent of operating junction temperatures.

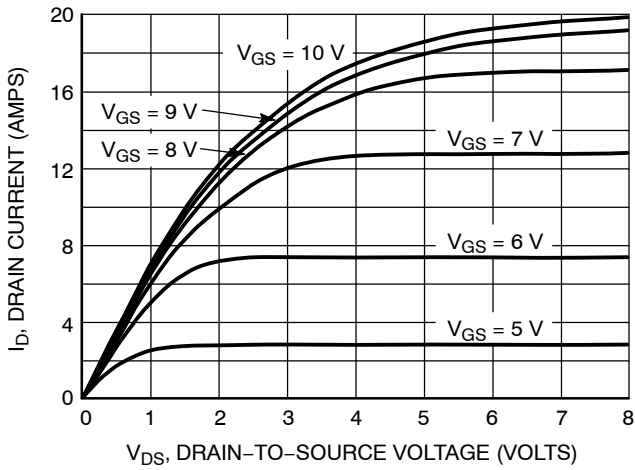


Figure 1. On-Region Characteristics

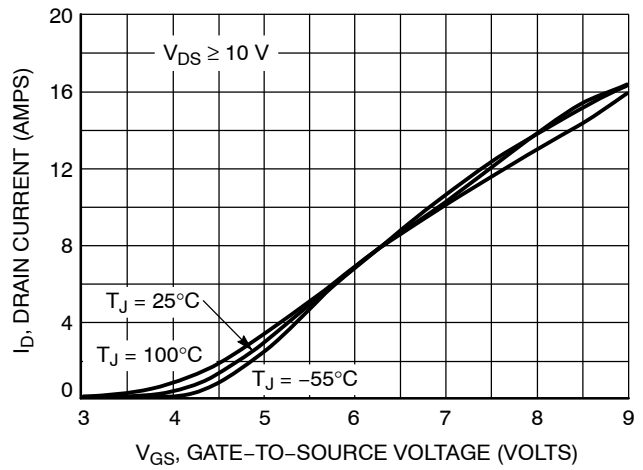


Figure 2. Transfer Characteristics

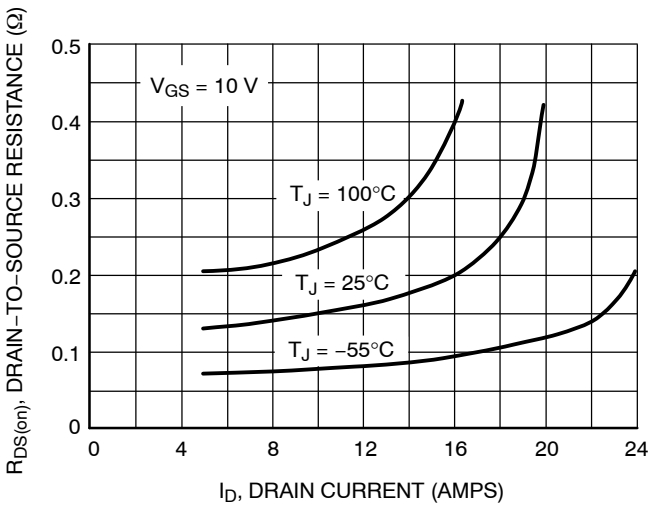


Figure 3. On-Resistance versus Gate-to-Source Voltage

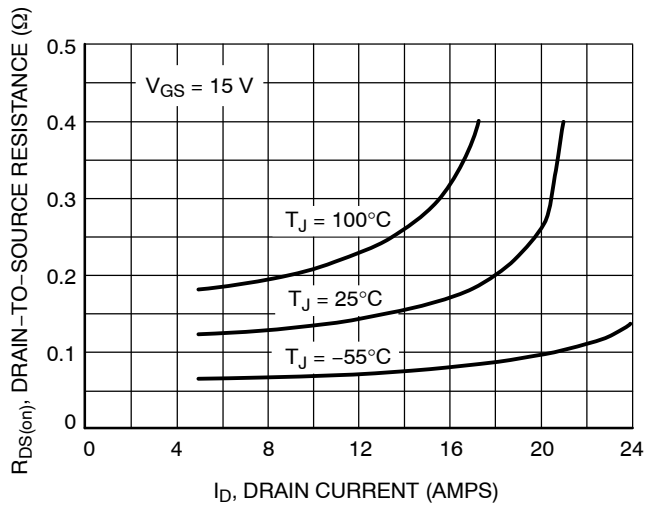


Figure 4. On-Resistance versus Drain Current and Gate Voltage

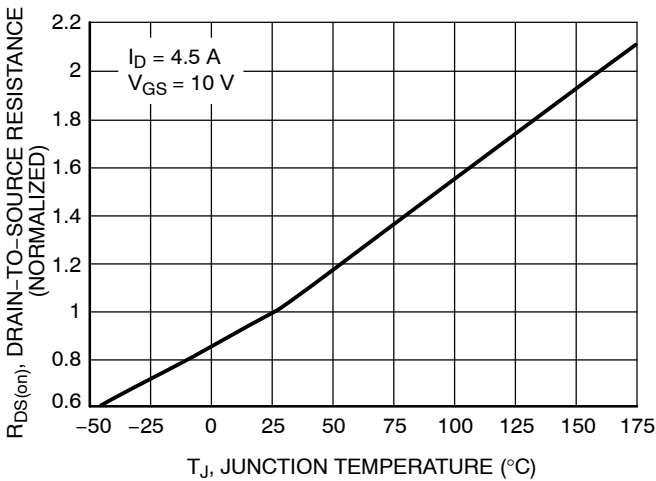


Figure 5. On-Resistance Variation with Temperature

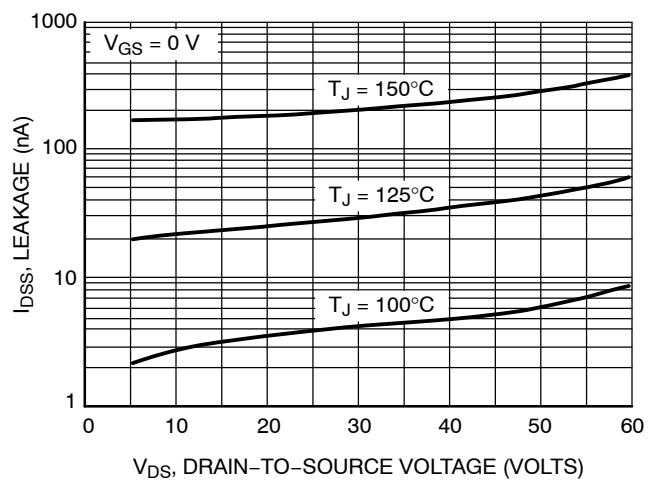


Figure 6. Drain-to-Source Leakage Current versus Voltage

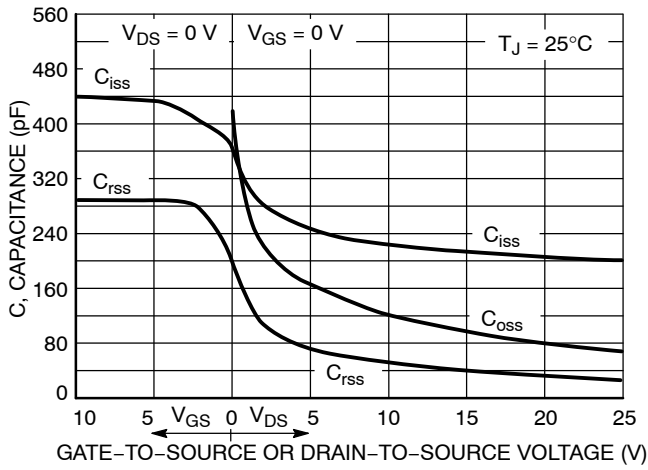


Figure 7. Capacitance Variation

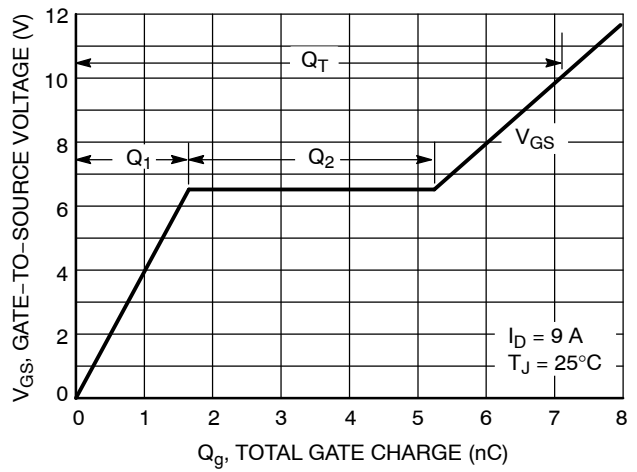


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

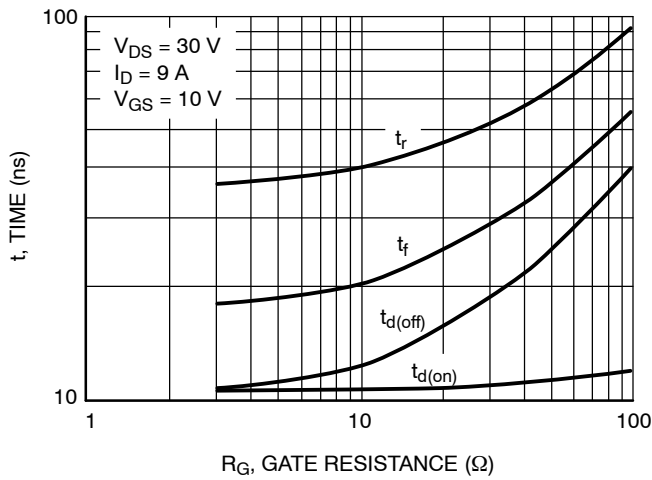


Figure 9. Resistive Switching Time Variation versus Gate Resistance

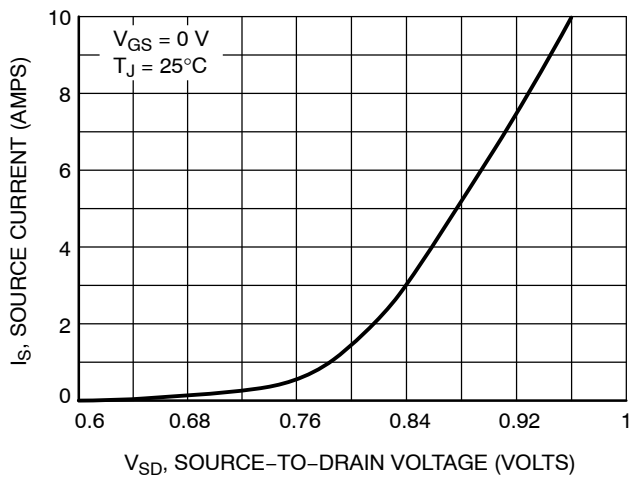


Figure 10. Diode Forward Voltage versus Current

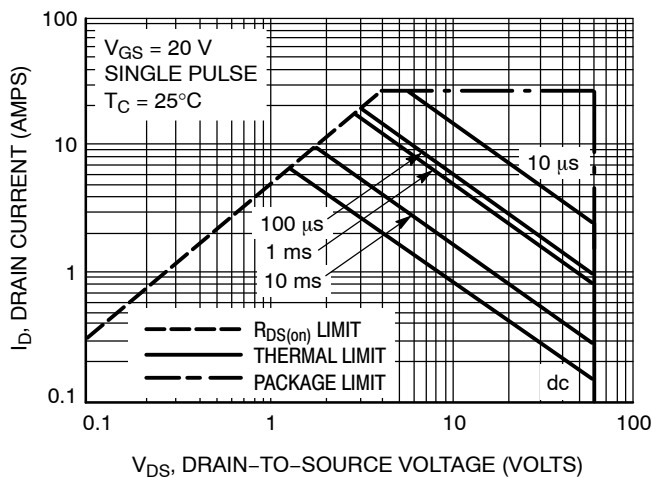


Figure 11. Maximum Rated Forward Biased Safe Operating Area

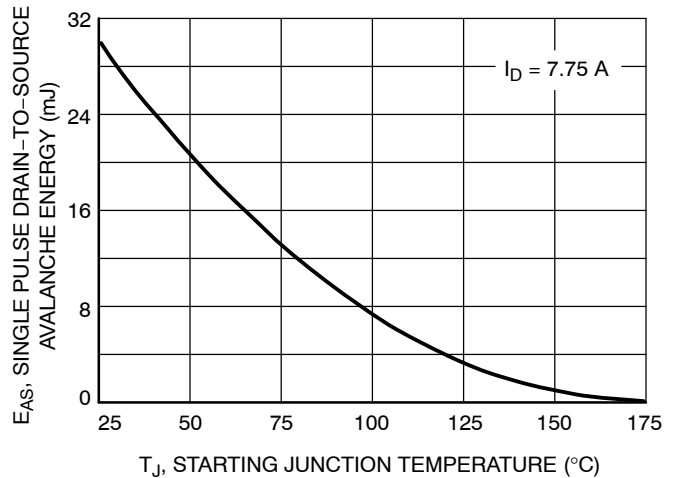


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

# NTD3055-150

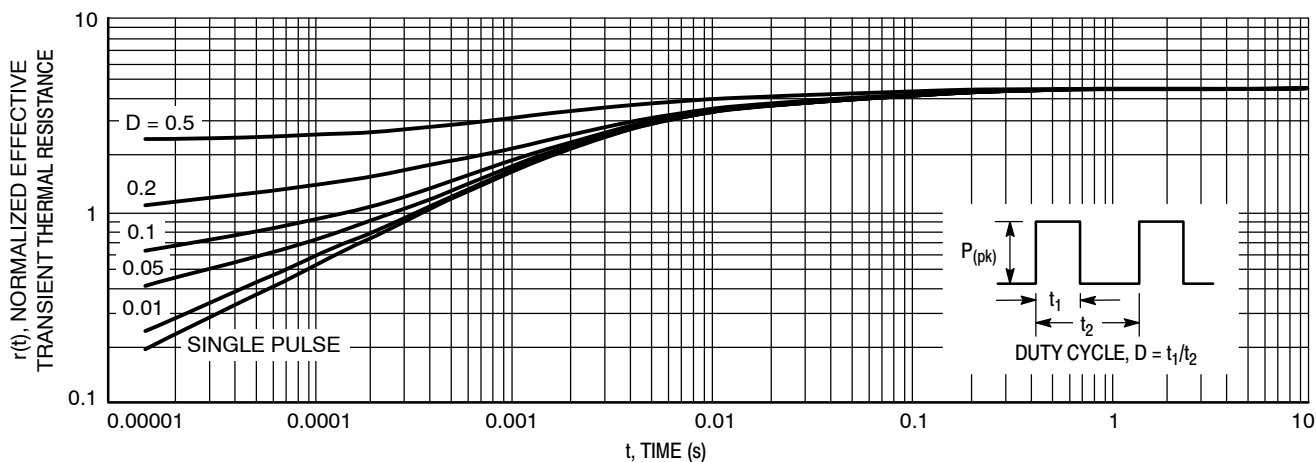


Figure 13. Thermal Response

## ORDERING INFORMATION

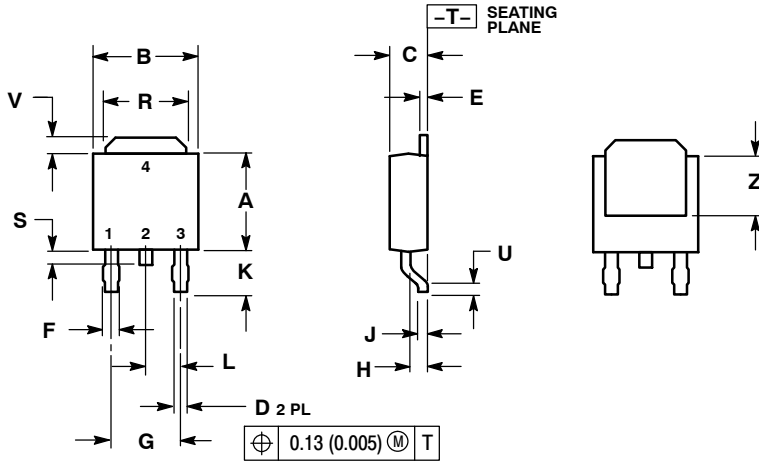
Device	Package	Shipping <sup>†</sup>
NTD3055-150	DPAK	75 Units/Rail
NTD3055-150G	DPAK (Pb-Free)	75 Units/Rail
NTD3055-150-1	DPAK-3	75 Units/Rail
NTD3055-150-1G	DPAK-3 (Pb-Free)	75 Units/Rail
NTD3055-150T4	DPAK	2500 Tape & Reel
NTD3055-150T4G	DPAK (Pb-Free)	2500 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTD3055-150

## PACKAGE DIMENSIONS

DPAK  
CASE 369C-01  
ISSUE C

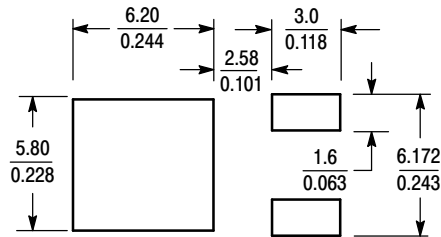


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 2:
1. GATE
  2. DRAIN
  3. SOURCE
  4. DRAIN

### SOLDERING FOOTPRINT\*



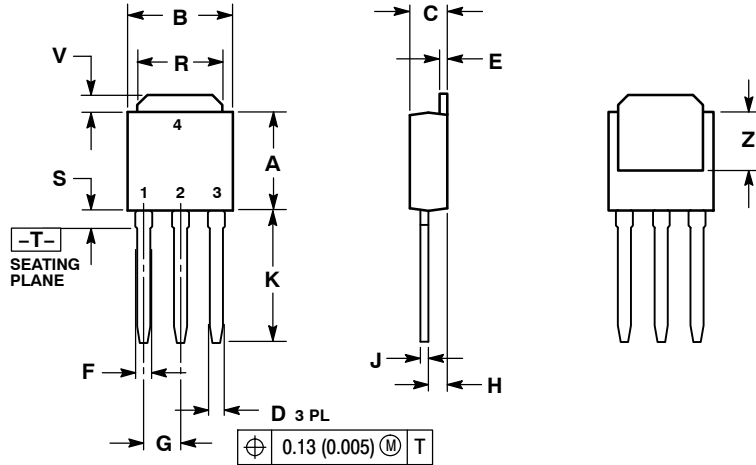
SCALE 3:1  $\left(\frac{\text{mm}}{\text{inches}}\right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NTD3055-150

## PACKAGE DIMENSIONS

### DPAK-3 CASE 369D-01 ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:

- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

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