



**AO4406**

**N-Channel Enhancement Mode Field Effect Transistor**



**General Description**

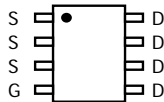
The AO4406/L uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 2.5V. This device makes an excellent high side switch for notebook CPU core DC-DC conversion. *AO4406 and AO4406L are electrically identical.*

- RoHS Compliant
- AO4406L is Halogen Free

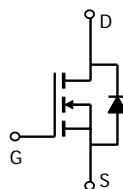
**Features**

- $V_{DS}$  (V) = 30V
- $I_D$  = 11.5A ( $V_{GS}$  = 10V)
- $R_{DS(ON)} < 14m\Omega$  ( $V_{GS}$  = 10V)
- $R_{DS(ON)} < 16.5m\Omega$  ( $V_{GS}$  = 4.5V)
- $R_{DS(ON)} < 26m\Omega$  ( $V_{GS}$  = 2.5V)

**UIS TESTED!**  
**Rg,Ciss,Coss,Crss Tested**



**SOIC-8**



**Absolute Maximum Ratings  $T_A=25^\circ\text{C}$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Continuous Drain Current <sup>AF</sup>	$I_D$	11.5	A
		$T_A=25^\circ\text{C}$	
	$T_A=70^\circ\text{C}$	9.6	
Pulsed Drain Current <sup>B</sup>	$I_{DM}$	80	
Avalanche Current <sup>B</sup>	$I_{AV}$	25	A
Repetitive Avalanche Energy <sup>B</sup> $L=0.3\text{mH}$	$E_{AV}$	94	mJ
Power Dissipation	$P_D$	$T_A=25^\circ\text{C}$	3
		$T_A=70^\circ\text{C}$	2.1
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>AF</sup>	$R_{\theta JA}$	$t \leq 10\text{s}$	23	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A</sup>		Steady-State	48	$^\circ\text{C/W}$
Maximum Junction-to-Lead <sup>C</sup>	$R_{\theta JL}$	12	16	$^\circ\text{C/W}$

Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±12V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	0.8	1	1.5	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =5V	60			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =12A T <sub>J</sub> =125°C		11.5	14	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A		13.5	16.5	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =8A		19.5	26	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =10A	25	38		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =10A, V <sub>GS</sub> =0V		0.83	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				4.5	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		1630	2300	pF
C <sub>oss</sub>	Output Capacitance			201		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			142	200	pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	0.4	0.8	1.8	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =15V, I <sub>D</sub> =11.5A	13.5	18	24	nC
Q <sub>gs</sub>	Gate Source Charge			2.5		nC
Q <sub>gd</sub>	Gate Drain Charge			5.5		nC
t <sub>D(on)</sub>	Turn-On Delay Time	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =1.2Ω, R <sub>GEN</sub> =3Ω		4	6	ns
t <sub>r</sub>	Turn-On Rise Time			5	7.5	ns
t <sub>D(off)</sub>	Turn-Off Delay Time			32	50	ns
t <sub>f</sub>	Turn-Off Fall Time			5	10	ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =10A, dI/dt=100A/μs		18.7	24	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =10A, dI/dt=100A/μs		12.5	15	nC

A: The value of R<sub>θJA</sub> is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R<sub>θJA</sub> is the sum of the thermal impedance from junction to lead R<sub>θJL</sub> and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The SOA curve provides a single pulse rating.

F: The current rating is based on the ≤ 10s junction to ambient thermal resistance rating.

Rev8: July 2008

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

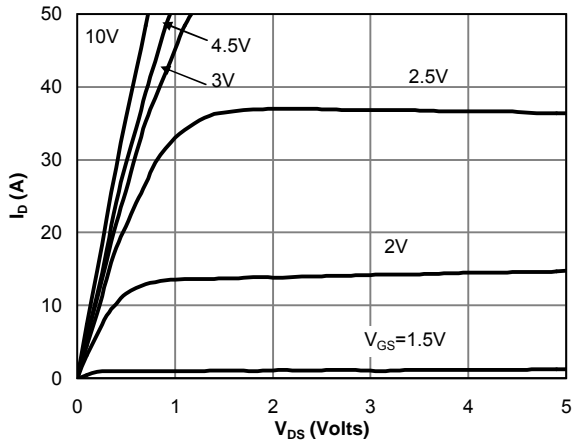


Fig 1: On-Region Characteristics

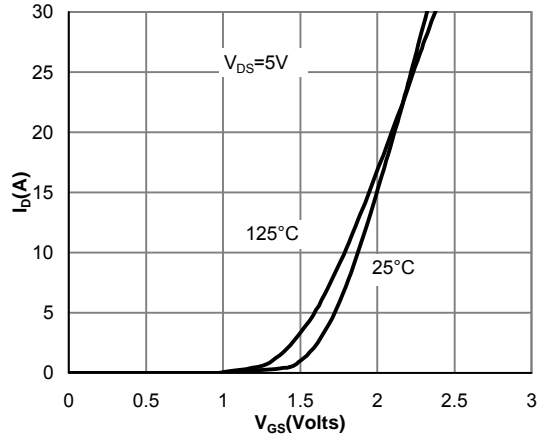


Figure 2: Transfer Characteristics

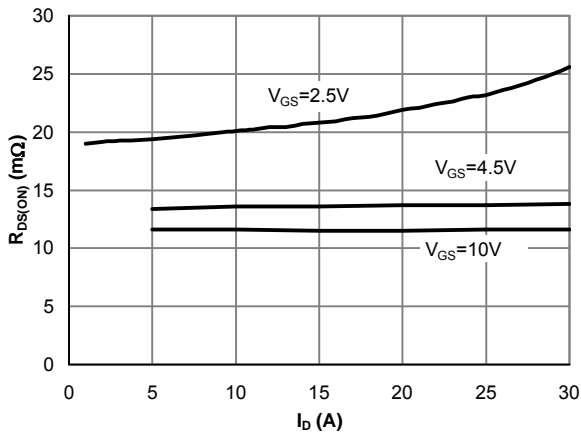


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

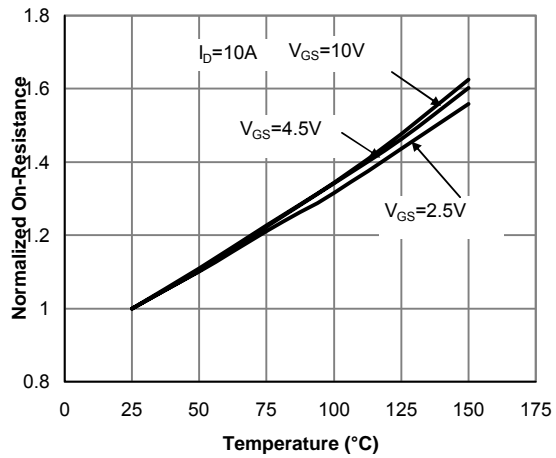


Figure 4: On-Resistance vs. Junction Temperature

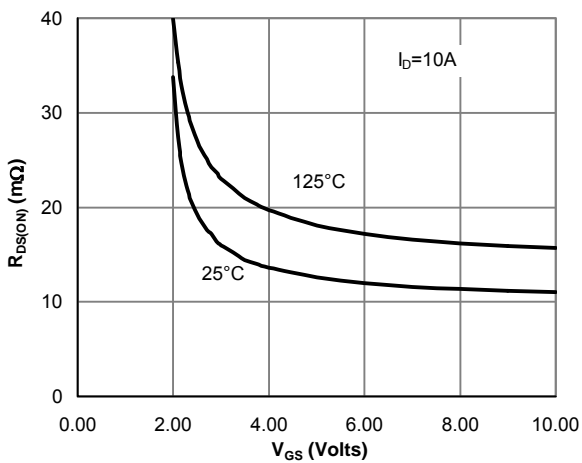


Figure 5: On-Resistance vs. Gate-Source Voltage

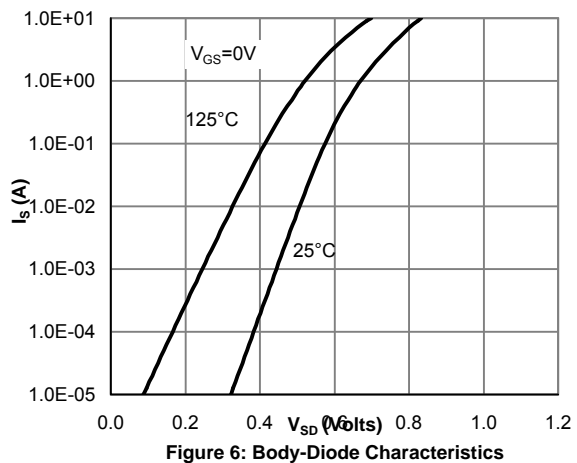


Figure 6: Body-Diode Characteristics

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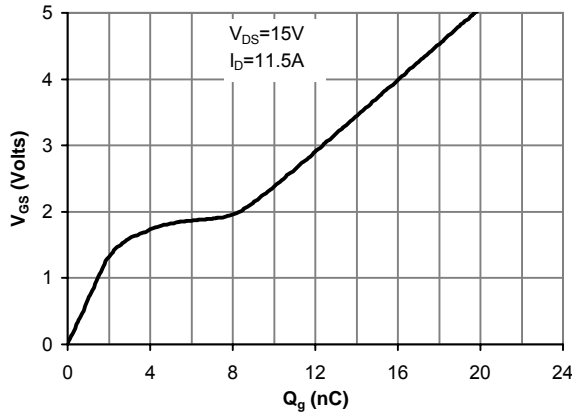


Figure 7: Gate-Charge Characteristics

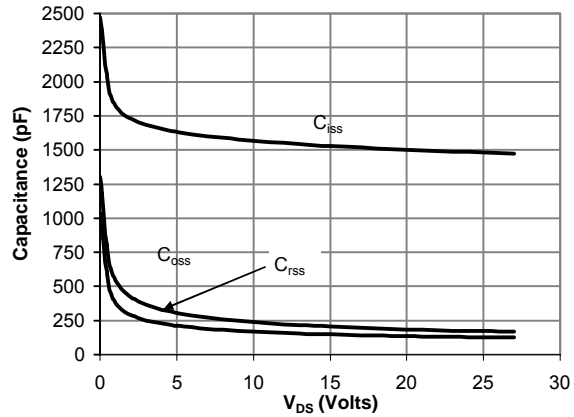


Figure 8: Capacitance Characteristics

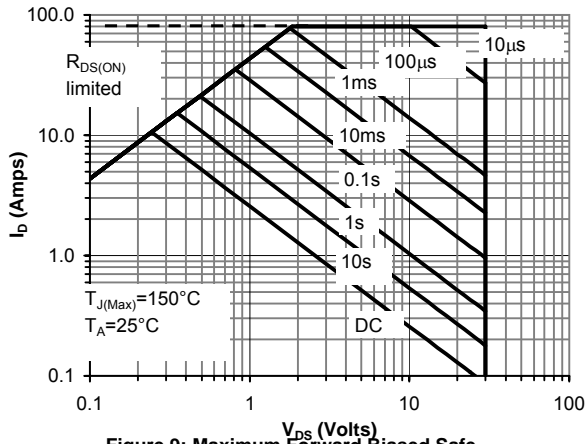


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

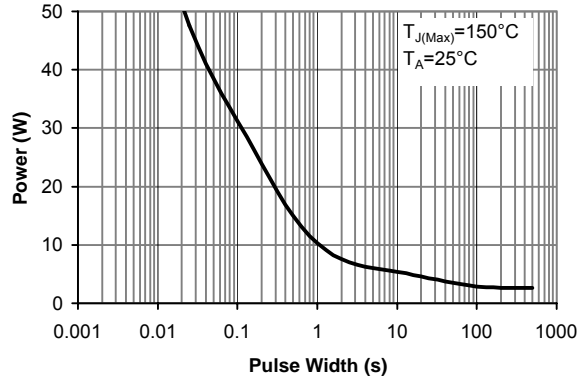


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

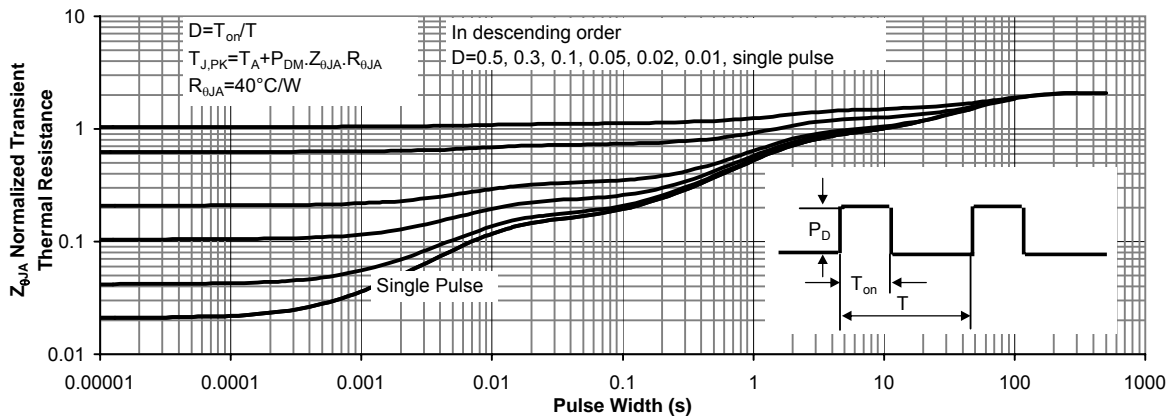
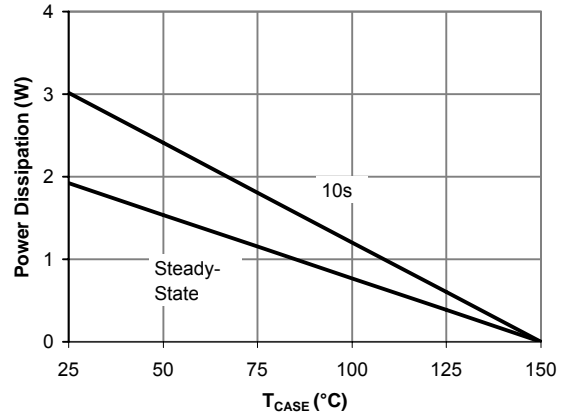
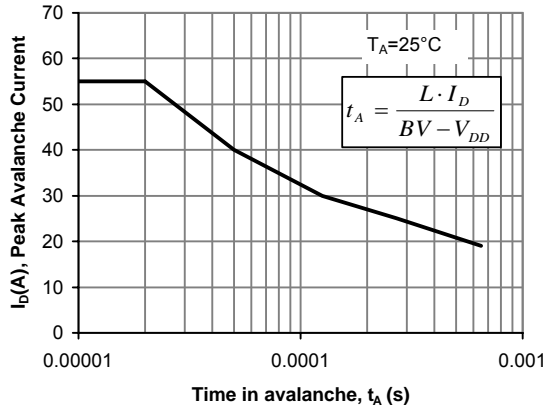
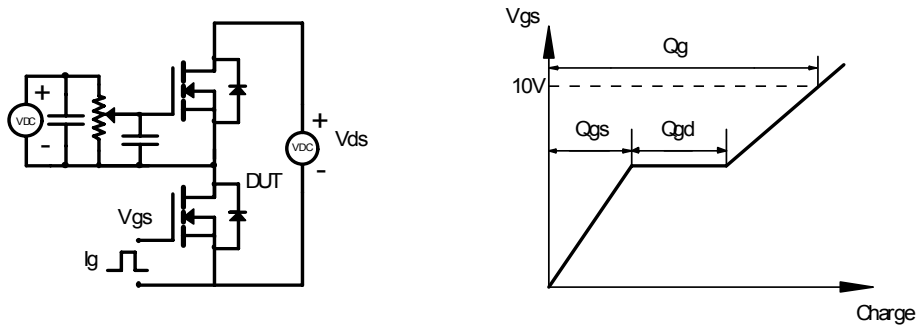


Figure 11: Normalized Maximum Transient Thermal Impedance

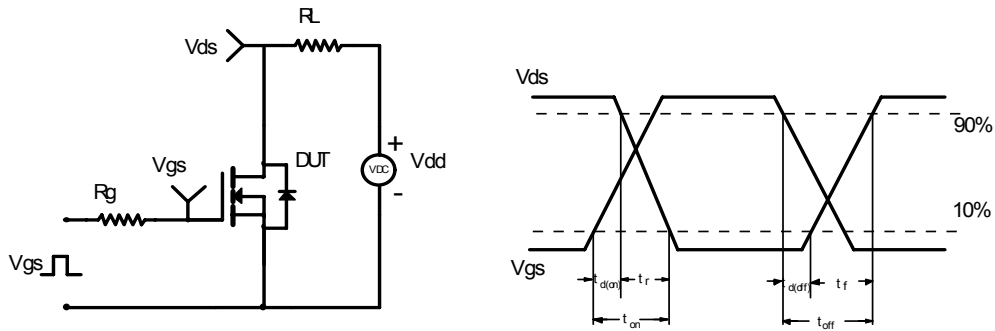
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



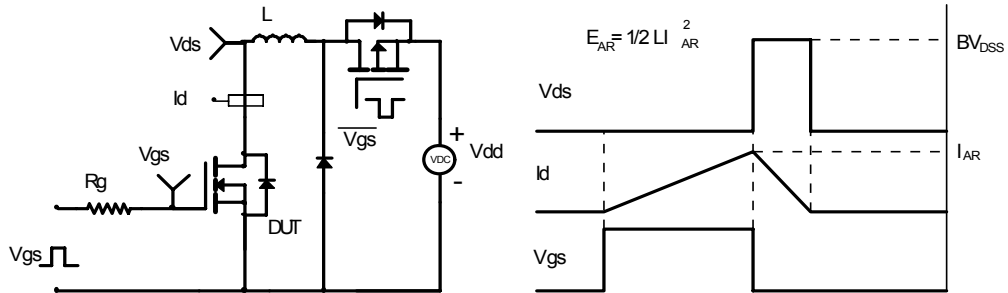
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

