NTLJS1102P

Power MOSFET

−8 V, −8.1 A, μCOOL™ Single P−Channel, 2x2 mm, WDFN package

Features

- WDFN Package with Exposed Drain Pad for Excellent Thermal Conduction
- Lowest $R_{DS(on)}$ in 2 x 2 mm Package
- 1.2 V $R_{DS(on)}$ Rating for Operation at Low Voltage Logic Level Gate Drive
- 2 x 2 mm Footprint Same as SC−88 Package
- Low Profile (<0.8 mm) for Easy Fit in Thin Environments
- This is a Halide−Free Device
- This is a Pb−Free Device

Applications

- High Side Load Switch
- Li Ion Battery Linear Mode Charging
- Optimized for Battery and Load Management Applications in Portable Equipment

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	−8	V
Gate−to−Source Voltage			V_{GS}	± 6	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	−6.2	A
		T_A = 85°C		−4.5	
	t ≤ 5 s	T_A = 25°C		−8.1	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	1.9	W
	t ≤ 5 s			3.3	
Continuous Drain Current (Note 2)	Steady State	T_A = 25°C	I_D	−3.7	A
		T_A = 85°C		−2.7	
Power Dissipation (Note 2)		T_A = 25°C	P_D	0.7	W
Pulsed Drain Current		t_p = 10 μs	I_{DM}	−30	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Source Current (Body Diode) (Note 2)			I_S	−5.5	A
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

1. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface−mounted on FR4 board using the minimum recommended pad size (Cu area = 30 mm² [2 oz] including traces).

ON Semiconductor®

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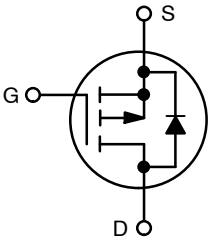
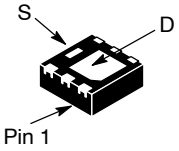
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
−8.0 V	36 mΩ @ −4.5 V	−6.2 A
	45 mΩ @ −2.5 V	−5.5 A
	68 mΩ @ −1.8 V	−3.0 A
	90 mΩ @ −1.5 V	−1.0 A
	300 mΩ @ −1.2 V	−0.2 A



P−CHANNEL MOSFET

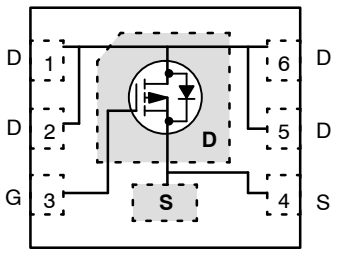


WDFN6
CASE 506AP

MARKING DIAGRAM

J6 = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Ambient − Steady State (Note 3)	$R_{\theta JA}$	65	°C/W
Junction−to−Ambient − t ≤ 5 s (Note 3)	$R_{\theta JA}$	38	
Junction−to−Ambient − Steady State min Pad (Note 4)	$R_{\theta JA}$	180	

3. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
4. Surface−mounted on FR4 board using the minimum recommended pad size (Cu area = 30 mm^2 [2 oz] including traces).

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA		−8.0			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = −250 μA, Ref to 25°C			−7.2		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −8V	T_J = 25°C			−1.0	μA
			T_J = 85°C			−10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±6V				±0.1	μA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −250 μA		−0.29		−0.72	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				2.7		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = −4.5 V, I_D = −6.2 A			25	36	mΩ
		V_{GS} = −4.5 V, I_D = −3.0 A			25	36	
		V_{GS} = −2.5 V, I_D = −5.5 A			34	45	
		V_{GS} = −2.5 V, I_D = −3.0 A			34	45	
		V_{GS} = −1.8 V, I_D = −3.0 A			45	68	
		V_{GS} = −1.5 V, I_D = −1.0 A			55	90	
		V_{GS} = −1.2 V, I_D = −0.2 A			80	300	
Forward Transconductance	g_{FS}	V_{DS} = −4 V, I_D = −6.2 A			14.3		S
CHARGES, CAPACITANCES AND GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = −4 V			1585		pF
Output Capacitance	C_{OSS}				350		
Reverse Transfer Capacitance	C_{RSS}				185		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −4.5 V, V_{DS} = − 4 V; I_D = −6.2 A			15.7	25	nC
Threshold Gate Charge	$Q_{G(TH)}$				0.8		
Gate−to−Source Charge	Q_{GS}				1.9		
Gate−to−Drain Charge	Q_{GD}				3.3		
SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 6)							
Turn−On Delay Time	$t_{D(ON)}$	V_{GS} = −4.5 V, V_{DS} = −4 V, I_D = −6.2 A, R_G = 1 Ω			8.0		ns
Rise Time	t_r				41		
Turn−Off Delay Time	$t_{d(OFF)}$				80		
Fall Time	t_f				70		

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
6. Switching characteristics are independent of operating junction temperatures

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 6)							
Turn−On Delay Time	$t_{D(ON)}$	V_{GS} = −4.5 V, V_{DS} = −4 V, I_D = −8.1 A, R_G = 1 Ω			8.0		ns
Rise Time	t_r				19		
Turn−Off Delay Time	$t_{d(OFF)}$				78		
Fall Time	t_f				50		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −1.0 A	T_J = 25°C		−0.6	−1.0	V
			T_J = 85°C		−0.58		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, d_{ISD}/d_t = 100 A/μs, I_S = −1.0 A			55	85	ns
Charge Time	t_a				18		
Discharge Time	t_b				37		
Reverse Recovery Charge	Q_{RR}				39		nC

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
6. Switching characteristics are independent of operating junction temperatures

ORDERING INFORMATION

Device	Package	Shipping†
NTLJS1102PTBG	WDFN6 (Pb−Free)	3000 / Tape & Reel
NTLJS1102PTAG	WDFN6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

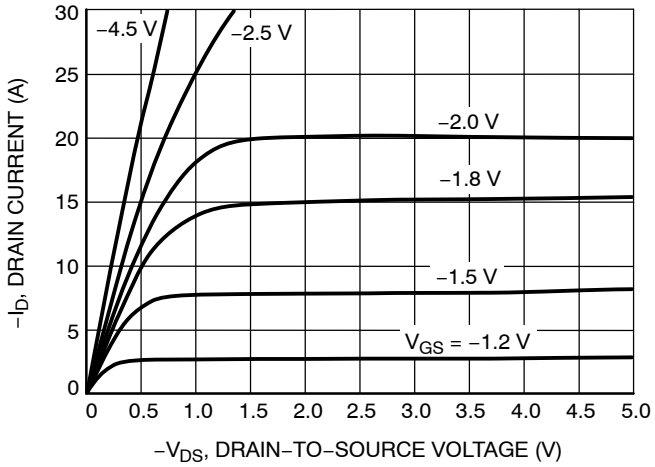


Figure 1. On−Region Characteristics

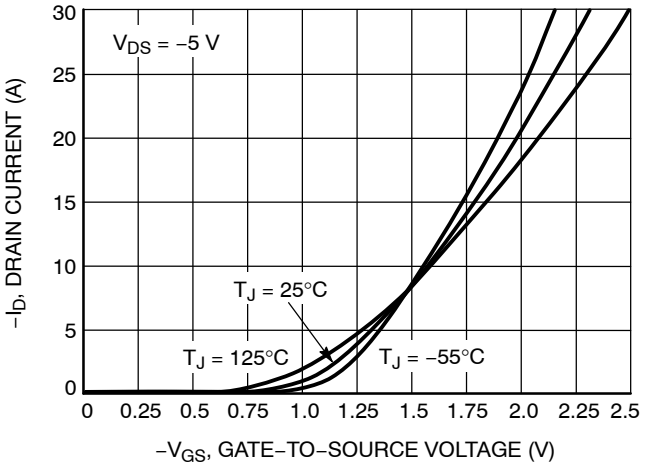


Figure 2. Transfer Characteristics

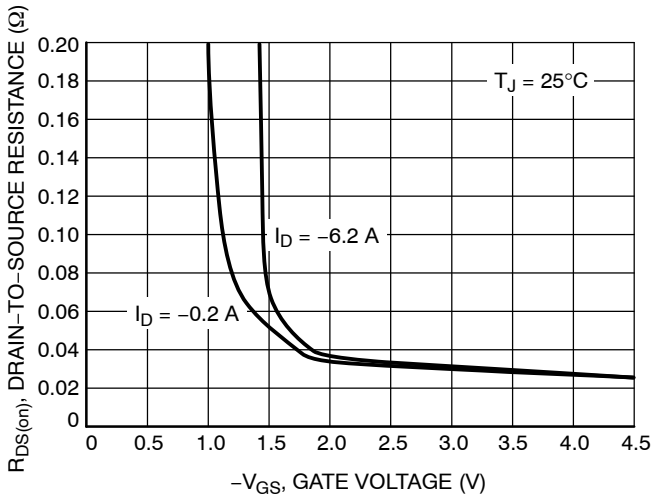


Figure 3. On−Resistance vs. Gate−to−Source Voltage

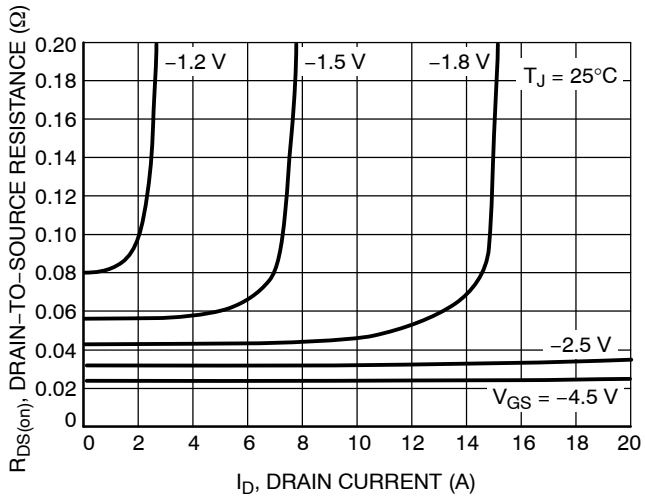


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

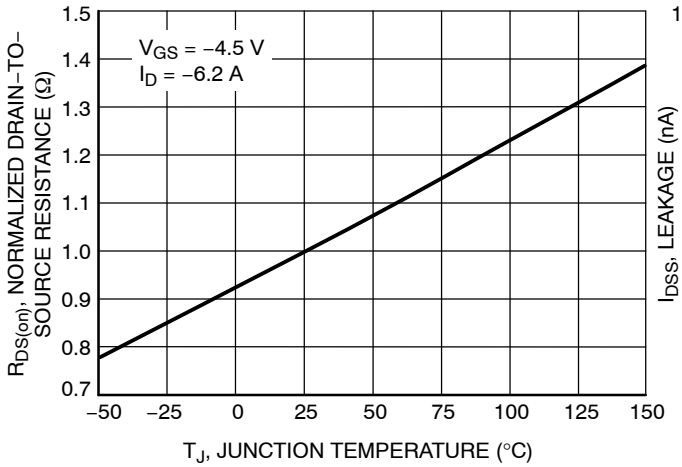


Figure 5. On−Resistance Variation with Temperature

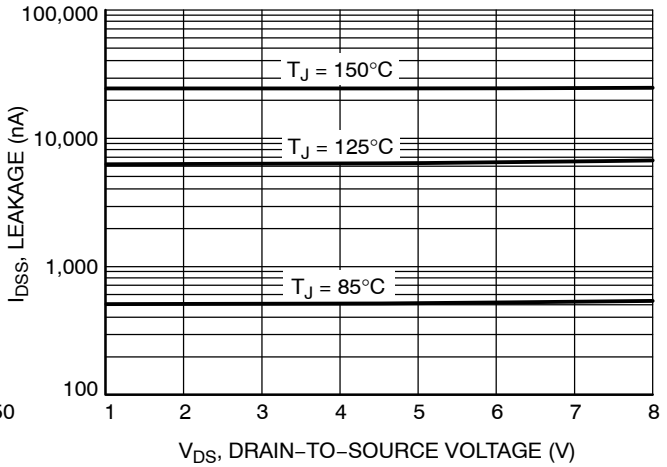


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

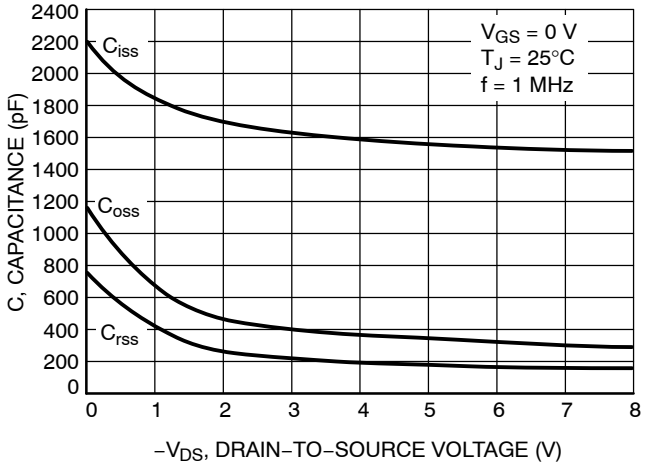


Figure 7. Capacitance Variation

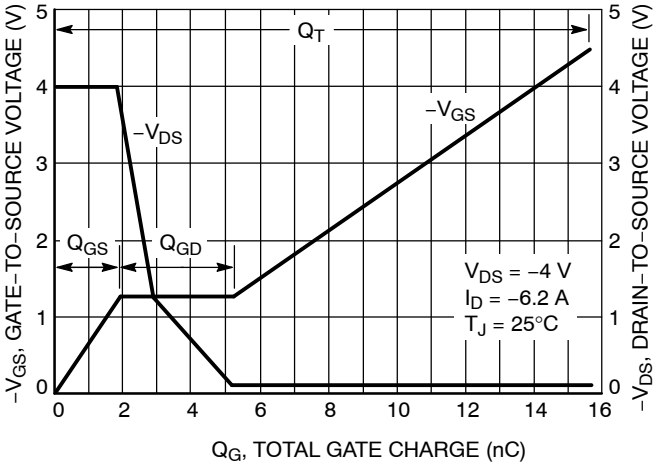


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

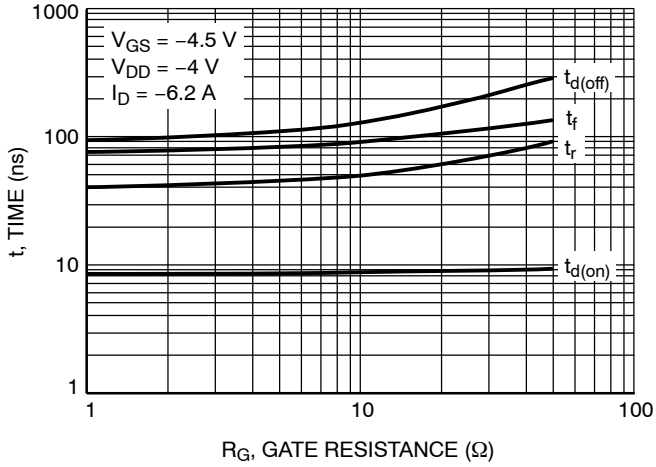


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

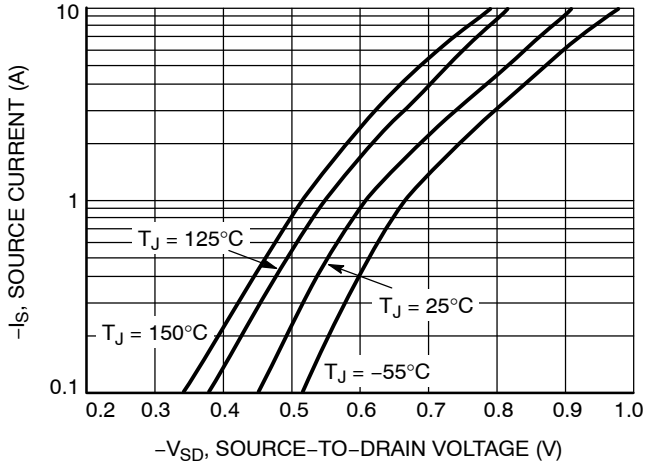


Figure 10. Diode Forward Voltage vs. Current

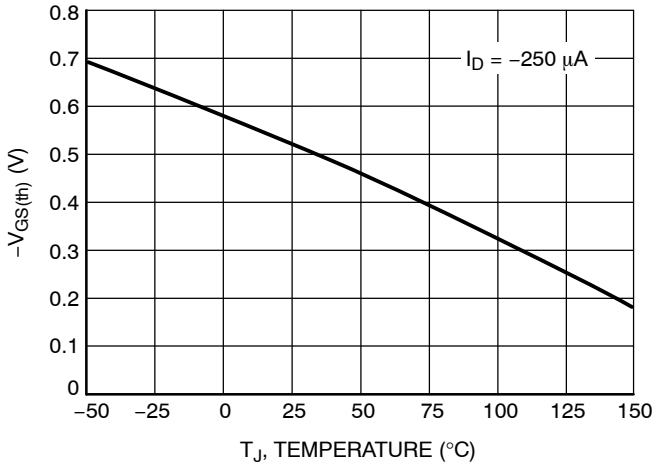


Figure 11. Threshold Voltage

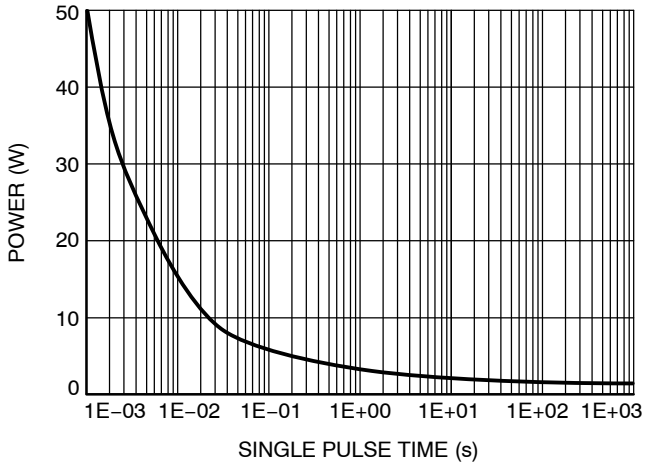


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

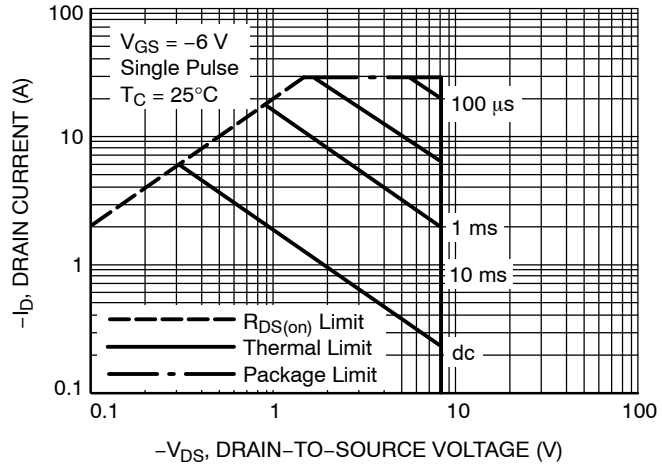


Figure 13. Maximum Rated Forward Biased Safe Operating Area

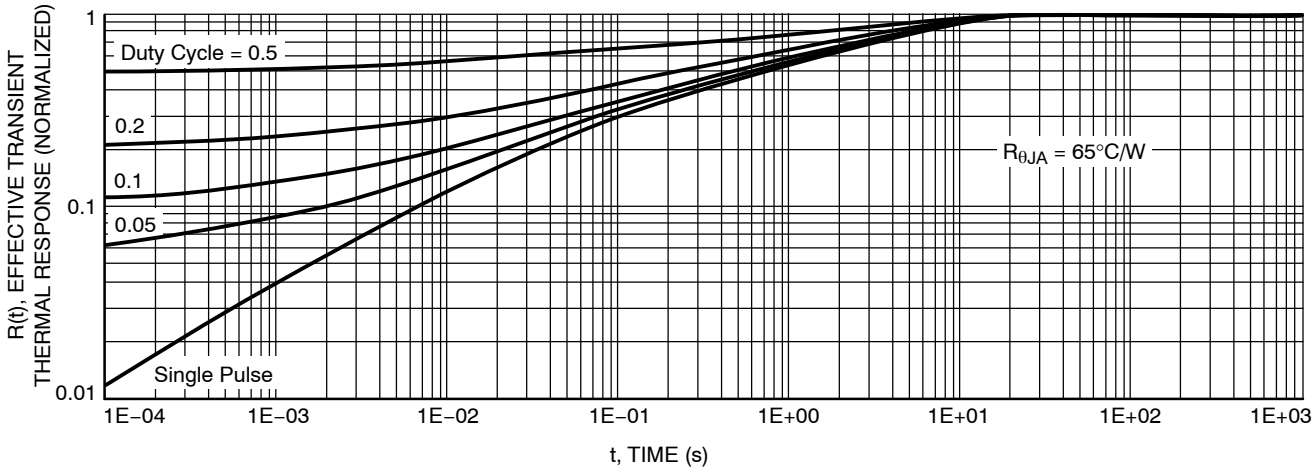
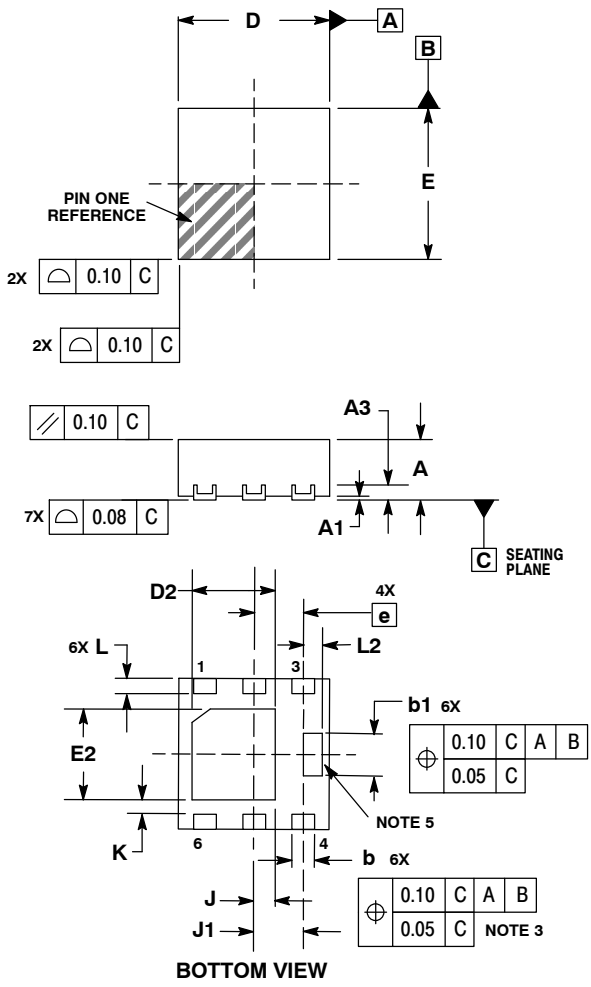


Figure 14. FET Thermal Response

PACKAGE DIMENSIONS

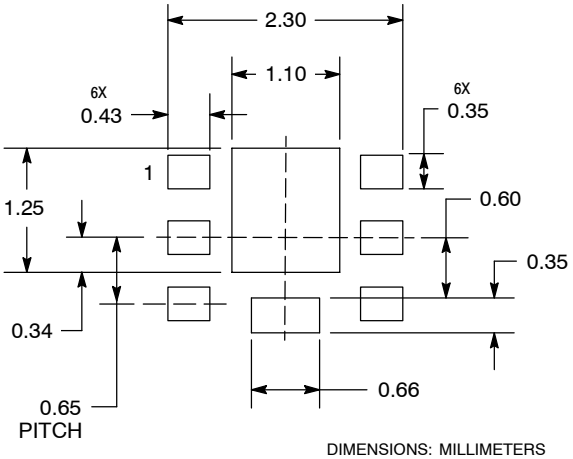
WDFN6 2x2
CASE 506AP−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. CENTER TERMINAL LEAD IS OPTIONAL. TERMINAL LEAD IS CONNECTED TO TERMINAL LEAD # 4.
6. PINS 1, 2, 5 AND 6 ARE TIED TO THE FLAG.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
b1	0.51	0.61
D	2.00 BSC	
D2	1.00	1.20
E	2.00 BSC	
E2	1.10	1.30
e	0.65 BSC	
K	0.15 REF	
L	0.20	0.30
L2	0.20	0.30
J	0.27 REF	
J1	0.65 REF	

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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For additional information, please contact your local Sales Representative

NTLJS1102P/D