



AO3401A

P-Channel Enhancement Mode Field Effect Transistor

General Description

The AO3401A/L uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation gate voltages as low as 2.5V. This device is suitable for use as a load switch or other general applications. AO3401A and AO3401AL are electrically identical.
-RoHS Compliant
-AO3401AL is Halogen Free

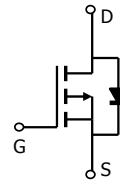
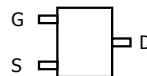
Features

V_{DS} (V) = -30V
 I_D = -4.3A (V_{GS} = -10V)
 $R_{DS(ON)}$ < 46m Ω (V_{GS} = -10V)
 $R_{DS(ON)}$ < 55m Ω (V_{GS} = -4.5V)
 $R_{DS(ON)}$ < 80m Ω (V_{GS} = -2.5V)

Rg, Ciss, Coss, Crss Tested



Top View



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current ^{A,F}	I_D	$T_A=25^\circ\text{C}$	A
		$T_A=70^\circ\text{C}$	
Pulsed Drain Current ^B	I_{DM}	-25	
Power Dissipation ^A	P_D	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^{AF}	$R_{\theta JA}$	$t \leq 10\text{s}$	65	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		Steady-State	85	$^\circ\text{C/W}$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	43	80	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±12V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =-250μA	-0.6	-1	-1.3	V
I _{D(ON)}	On state drain current	V _{GS} =-4.5V, V _{DS} =-5V	-25			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-4.3A T _J =125°C		36 52	44 63	mΩ
		V _{GS} =-4.5V, I _D =-3.5A		44	55	mΩ
		V _{GS} =-2.5V, I _D =-2.5A		62	80	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-4.3A		13		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.75	-1	V
I _S	Maximum Body-Diode Continuous Current				-2	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1MHz		933	1200	pF
C _{oss}	Output Capacitance			108		pF
C _{rss}	Reverse Transfer Capacitance			81		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		6	9	Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =-4.5V, V _{DS} =-15V, I _D =-4.3A		9.3	12.2	nC
Q _{gs}	Gate Source Charge			1.5		nC
Q _{gd}	Gate Drain Charge			3.7		nC
t _{D(on)}	Turn-On Delay Time	V _{GS} =-10V, V _{DS} =-15V, R _L =3.5Ω, R _{GEN} =6Ω		5.2		ns
t _r	Turn-On Rise Time			6.8		ns
t _{D(off)}	Turn-Off Delay Time			42		ns
t _f	Turn-Off Fall Time			15		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-4.3A, dI/dt=100A/μs		21	28	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-4.3A, dI/dt=100A/μs		14.3		nC

A: The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

F: The current rating is based on the t ≤ 10s thermal resistance rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

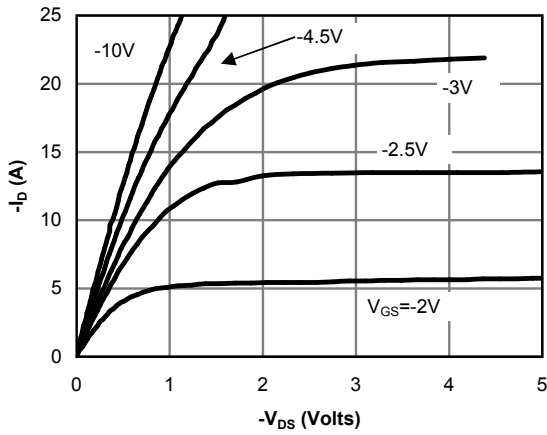


Figure 1: On-Region Characteristics

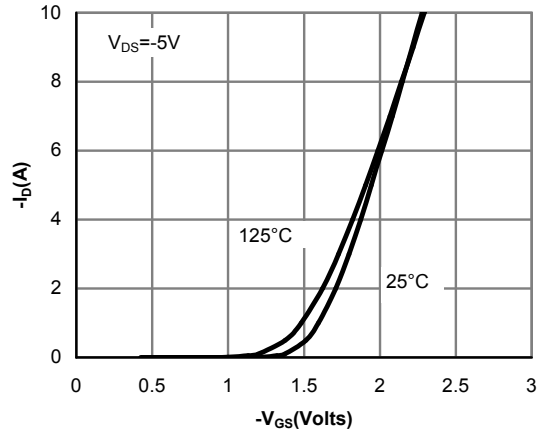


Figure 2: Transfer Characteristics

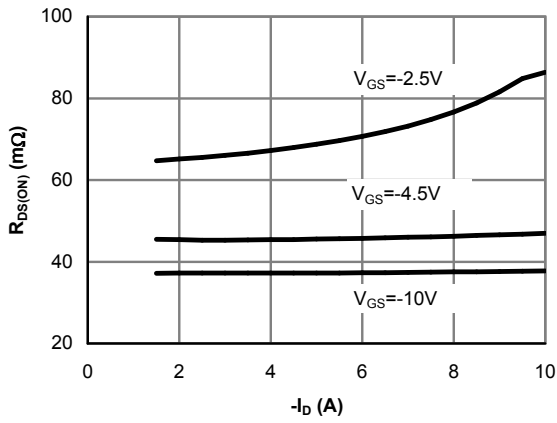


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

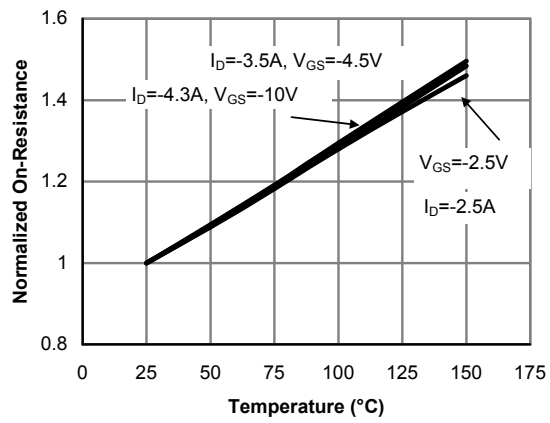


Figure 4: On-Resistance vs. Junction Temperature

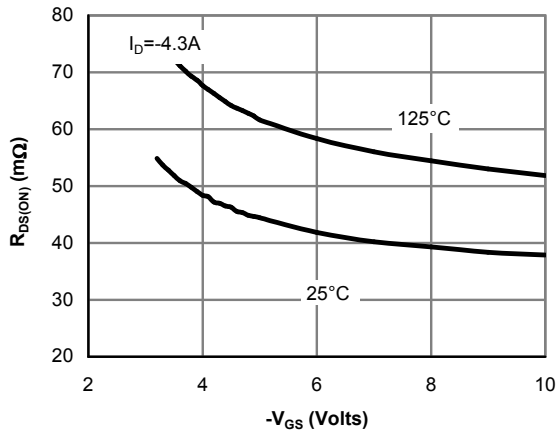


Figure 5: On-Resistance vs. Gate-Source Voltage

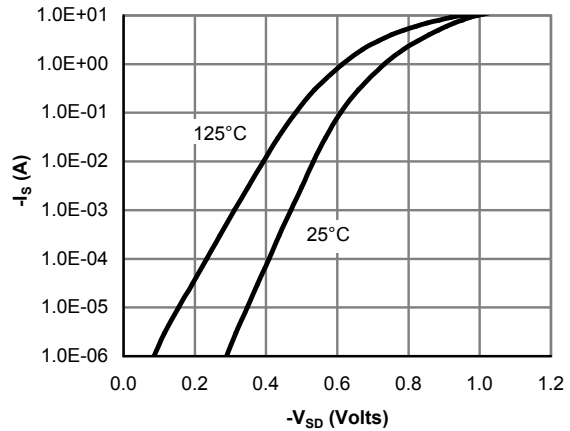


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

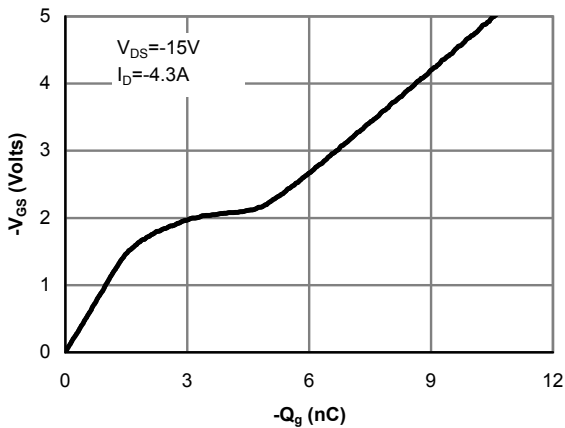


Figure 7: Gate-Charge Characteristics

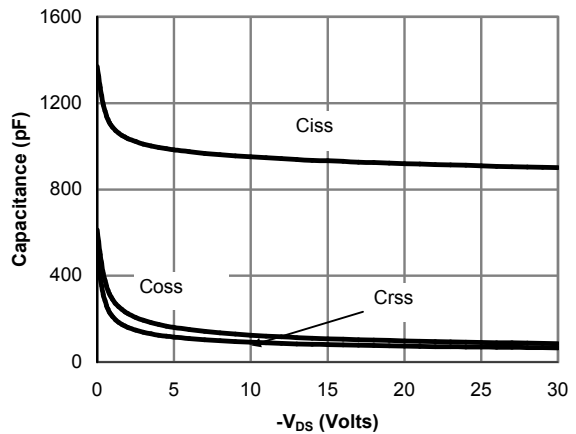


Figure 8: Capacitance Characteristics

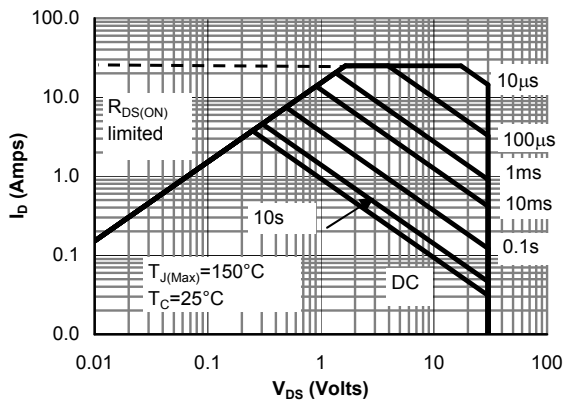


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

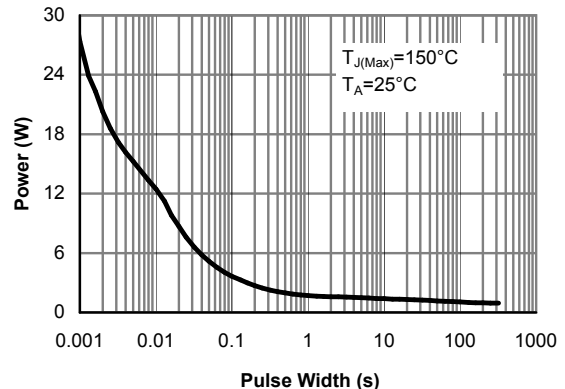


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

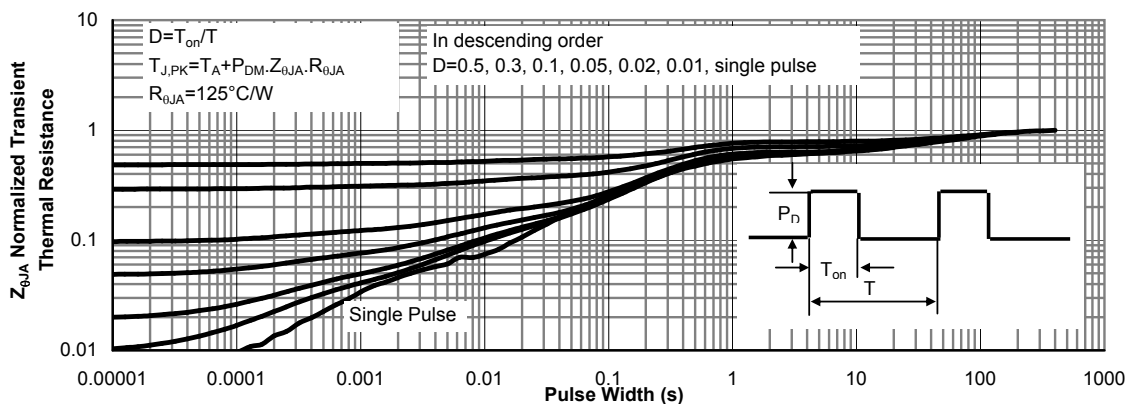
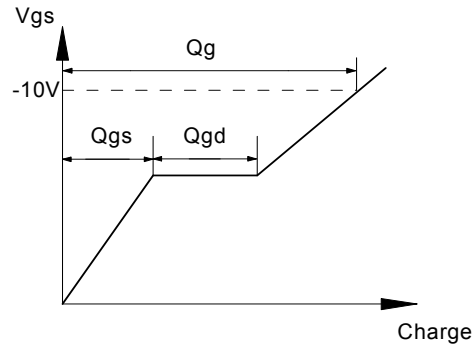
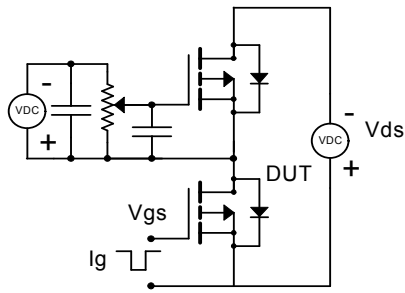
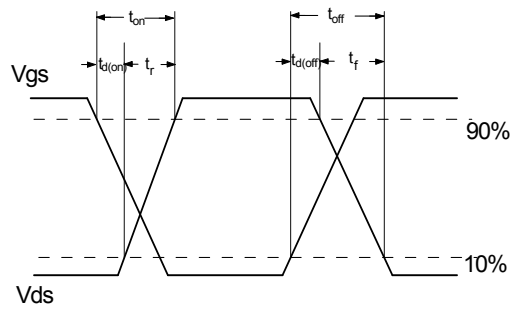
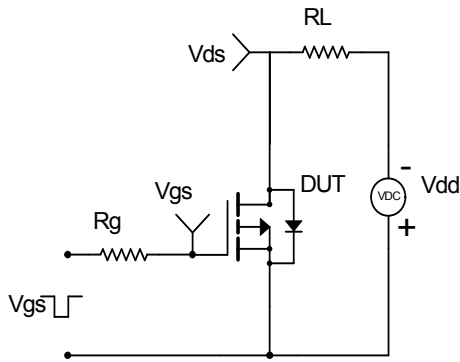


Figure 11: Normalized Maximum Transient Thermal Impedance

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

