# **Power MOSFET**

# 30 V, 3.2 A, Single N-Channel, SOT-23

### **Features**

- Low R<sub>DS(on)</sub>
- Low Gate Charge
- Low Threshold Voltage
- Halide Free
- This is a Pb-Free Device

## **Applications**

- Power Converters for Portables
- Battery Management
- Load/Power Switch

## MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit	
Drain-to-Source Voltage			V <sub>DSS</sub>	30	V	
Gate-to-Source Voltage			V <sub>GS</sub>	±12	V	
Continuous Drain	t ≤ 30 s	T <sub>A</sub> = 25°C		3.2		
Current (Note 1)	1 ≤ 30 S	T <sub>A</sub> = 85°C	I <sub>D</sub>	2.3	Α	
	t ≤ 10 s	T <sub>A</sub> = 25°C		4.0		
Power Dissipation (Note 1)	Steady State	T <sub>A</sub> = 25°C	P <sub>D</sub>	0.78	W	
	t ≤ 10 s			1.25		
Pulsed Drain Current	Ised Drain Current $t_p = 10 \mu s$			8.0	Α	
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>stg</sub>	–55 to 150	°C	
Source Current (Body Diode)			I <sub>S</sub>	0.78	Α	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	260	°C/W
Junction-to-Ambient - t ≤ 30 s	$R_{\theta JA}$	153	
Junction-to-Ambient - t < 10 s (Note 1)	$R_{\theta JA}$	100	

Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).

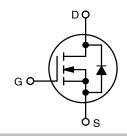


## ON Semiconductor®

## http://onsemi.com

V <sub>(BR)DSS</sub>	V <sub>(BR)DSS</sub> R <sub>DS(on)</sub> MAX	
30 V	55 mΩ @ 10 V	3.2 A
	70 mΩ @ 4.5 V	2.8 A
	110 mΩ @ 2.5 V	2.0 A

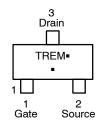
## SIMPLIFIED SCHEMATIC - N-CHANNEL



## MARKING DIAGRAM/ PIN ASSIGNMENT



SOT-23 CASE 318 STYLE 21



TRE = Specific Device Code

M = Date Code ■ = Pb-Free Package

(Note: Microdot may be in either location)

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NTR4170NT1G	SOT-23 (Pb-Free)	3000/Tape & Reel
NTR4170NT3G	SOT-23 (Pb-Free)	10000/Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

## **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise noted)

Parameter	Parameter Symbol Test Conditions Min		Min	Тур	Max	Units
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA 30				V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub>	I <sub>D</sub> = 250 μA, Reference to 25°C		26.4		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 24 V, T <sub>J</sub> = 25°C V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 24 V, T <sub>J</sub> = 125°C			1.0 5.0	μΑ
Gate-to-Source Leakage Current	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_D = 250 \mu A$	0.6	1.0	1.4	٧
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			3.3		mV/°C
Drain-to-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.2 A		45	55	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 2.8 A		50	70	
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 2.0 A		64	110	
Forward Transconductance	9FS	V <sub>DS</sub> = 5.0 V, I <sub>D</sub> = 3.2 A		8.0		S
CHARGES, CAPACITANCES AND GA	TE RESISTA	NCE			•	
Input Capacitance	C <sub>iss</sub>			432		pF
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 \text{ V, f} = 1.0 \text{ MHz,}$ $V_{DS} = 15 \text{ V}$		53.6		
Reverse Transfer Capacitance	C <sub>rss</sub>	VDS = 10 V		37.1		
Total Gate Charge	Q <sub>G(TOT)</sub>			4.76		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 15 V,		0.3		
Gate-to-Source Charge	$Q_{GS}$	I <sub>D</sub> = 3.2 A		1.0		
Gate-to-Drain Charge	$Q_{GD}$			1.4		1
Gate Resistance	$R_{G}$					Ω
SWITCHING CHARACTERISTICS, VG	is = <b>4.5 V</b> (No	te 4)		•	•	•
Turn-On Delay Time	t <sub>d(on)</sub>			6.4		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DD</sub> = 15 V,		9.9		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D = 3.2 \text{ A}, R_G = 6.2 \Omega$		15.1		1
Fall Time	t <sub>f</sub>			3.5		1
DRAIN-SOURCE DIODE CHARACTE	RISTICS			•	•	
Forward Diode Voltage	$V_{SD}$	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.0 A, T <sub>J</sub> = 25°C		0.75	1.0	٧
Reverse Recovery Time	t <sub>RR</sub>			8.0		ns
Charge Time	ta	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.0 A,		5.1		1
Discharge Time	t <sub>b</sub>	$dI_{SD}/d_t = 100 \text{ A/}\mu\text{s}$		2.9		1
Reverse Recovery Charge	Q <sub>RR</sub>			2.9		nC

- Surface–mounted on FR4 board using 1 in sq pad size (CU area = 1.127 in sq [2 oz] including traces).
   Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
   Switching characteristics are independent of operating junction temperatures.

## **TYPICAL CHARACTERISTICS**

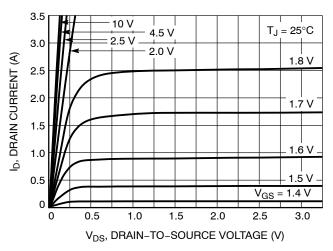


Figure 1. On-Region Characteristics

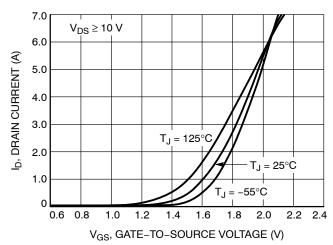


Figure 2. Transfer Characteristics

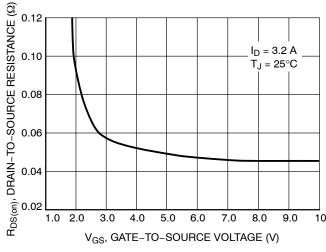


Figure 3. On-Resistance vs. Gate Voltage

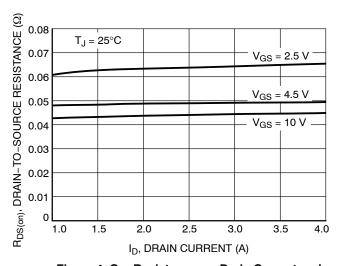


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

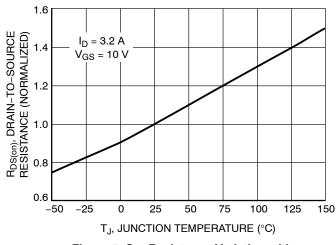


Figure 5. On–Resistance Variation with Temperature

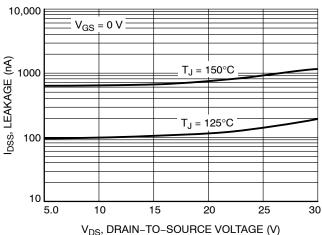


Figure 6. Drain-to-Source Leakage Current vs. Voltage

## **TYPICAL CHARACTERISTICS**

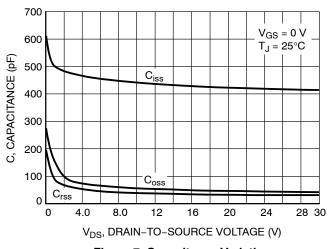


Figure 7. Capacitance Variation

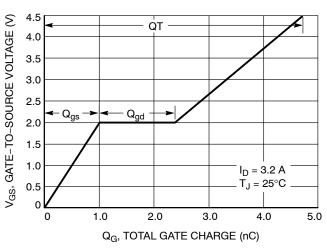


Figure 8. Gate-to-Source Voltage vs. Total Charge

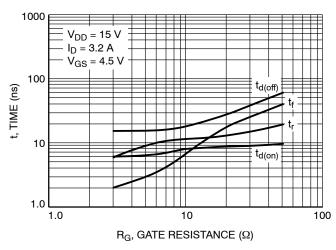


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

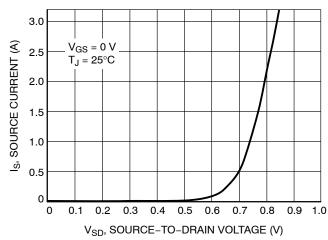
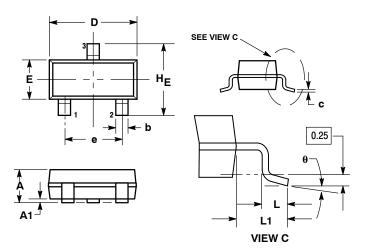


Figure 10. Diode Forward Voltage vs. Current

### PACKAGE DIMENSIONS

## SOT-23 (TO-236) CASE 318-08 ISSUE AN



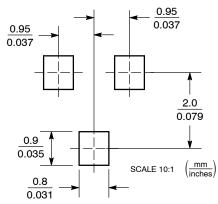
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- THASIN, 1962.
  CONTROLLING DIMENSION: INCH.
  MAXIMUM LEAD THICKNESS INCLUDES LEAD
  FINISH THICKNESS. MINIMUM LEAD
  THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
- 318-01 THRU -07 AND -09 OBSOLETE, NEW STANDARD 318-08.

	MILLIMETERS			INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
Α	0.89	1.00	1.11	0.035	0.040	0.044	
A1	0.01	0.06	0.10	0.001	0.002	0.004	
b	0.37	0.44	0.50	0.015	0.018	0.020	
С	0.09	0.13	0.18	0.003	0.005	0.007	
D	2.80	2.90	3.04	0.110	0.114	0.120	
E	1.20	1.30	1.40	0.047	0.051	0.055	
е	1.78	1.90	2.04	0.070	0.075	0.081	
L	0.10	0.20	0.30	0.004	0.008	0.012	
L1	0.35	0.54	0.69	0.014	0.021	0.029	
HE	2.10	2.40	2.64	0.083	0.094	0.104	

STYLE 21:

- PIN 1. GATE
  - SOURCE
  - DRAIN

## **SOLDERING FOOTPRINT**



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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