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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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HAT2198R

Silicon N Channel Power MOS FET Power Switching

REJ03G0062-0200

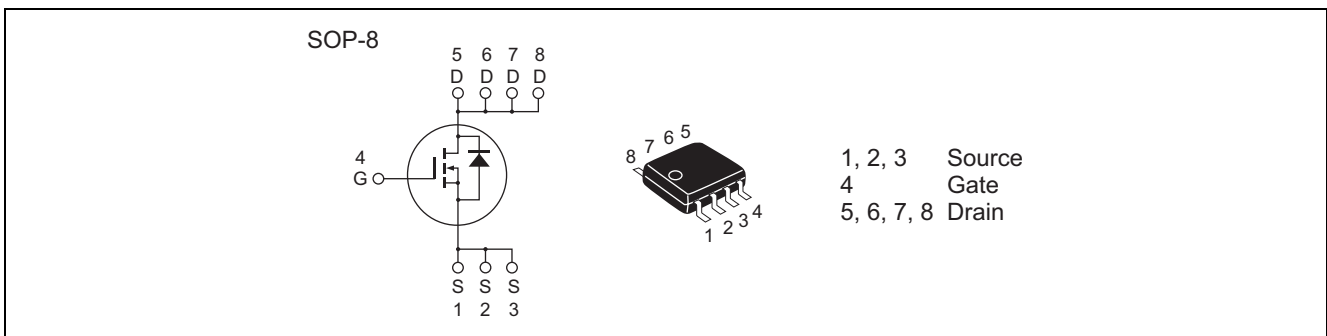
Rev.2.00

Oct.18.2004

Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 7.2 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)

Outline



Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	14	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	112	A
Body-drain diode reverse drain current	I_{DR}	14	A
Avalanche current	I_{AP} ^{Note 2}	14	A
Avalanche energy	E_{AR} ^{Note 2}	19.6	mJ
Channel dissipation	P_{ch} ^{Note3}	2.5	W
Channel to ambient thermal impedance	θ_{ch-a} ^{Note3}	50	$^\circ\text{C}/\text{W}$
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$

2. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$

3. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10\text{s}$

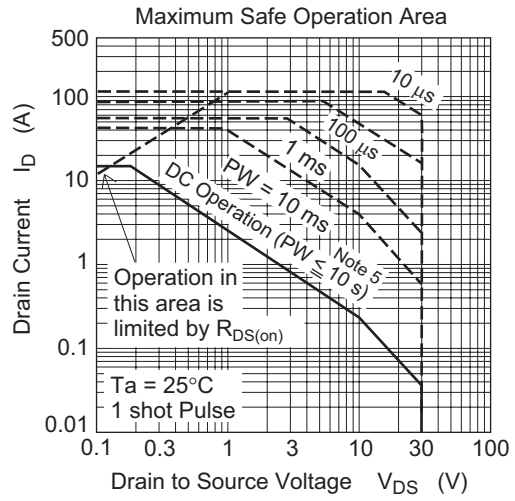
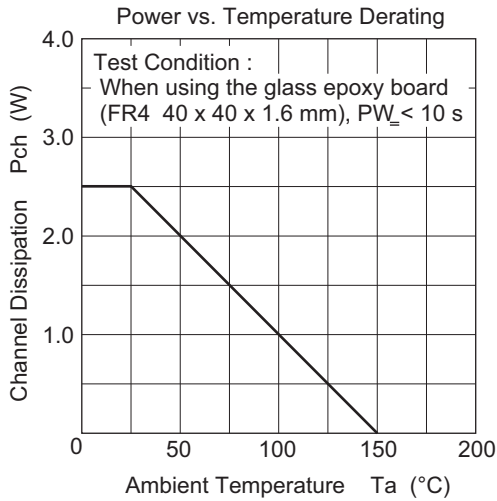
Electrical Characteristics

(Ta = 25°C)

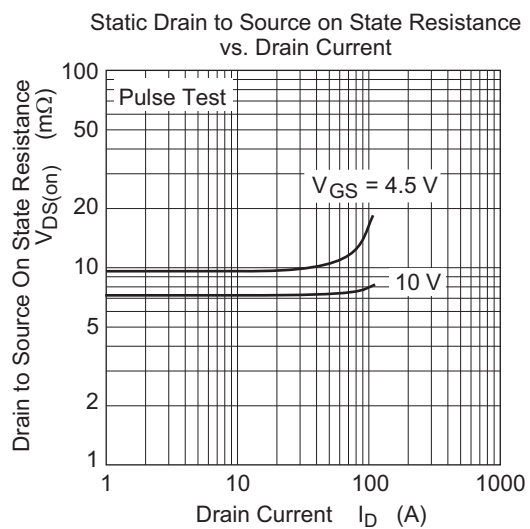
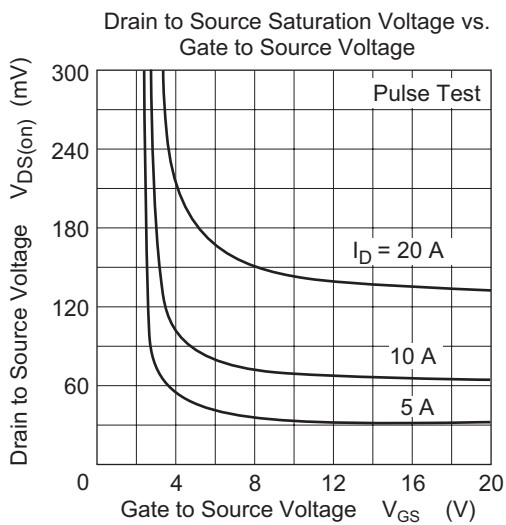
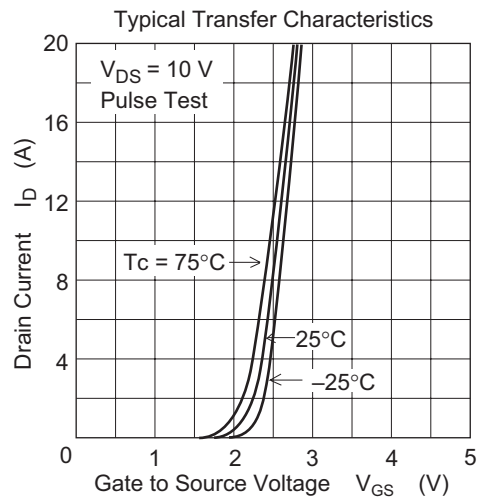
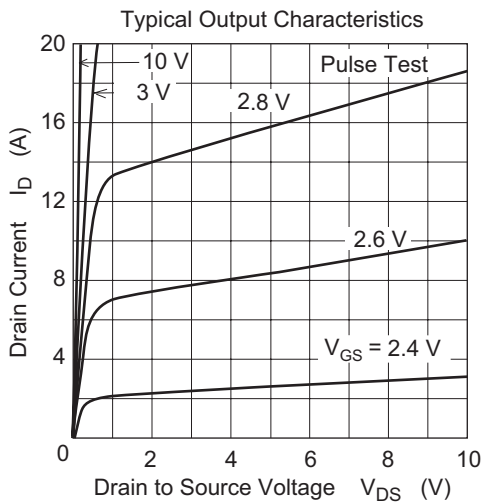
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	7.2	9.0	$\text{m}\Omega$	$I_D = 7 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	9.6	14.0	$\text{m}\Omega$	$I_D = 7 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	18	30	—	S	$I_D = 7 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	1650	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	390	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	135	—	pF	$f = 1 \text{ MHz}$
Gate Resistance	R_g	—	0.55	—	Ω	
Total gate charge	Q_g	—	11	—	nC	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	4.7	—	nC	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	Q_{gd}	—	2.5	—	nC	$I_D = 14 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	8.5	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 7 \text{ A}$
Rise time	t_r	—	5	—	ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	38	—	ns	$R_L = 1.42 \Omega$
Fall time	t_f	—	3.8	—	ns	$R_g = 4.7 \Omega$
Body-drain diode forward voltage	V_{DF}	—	0.80	1.04	V	$I_F = 14 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	28	—	ns	$I_F = 14 \text{ A}$, $V_{GS} = 0$ $diF/dt = 100 \text{ A}/\mu\text{s}$

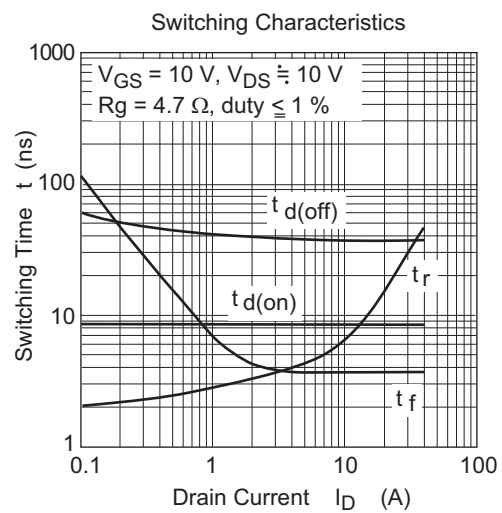
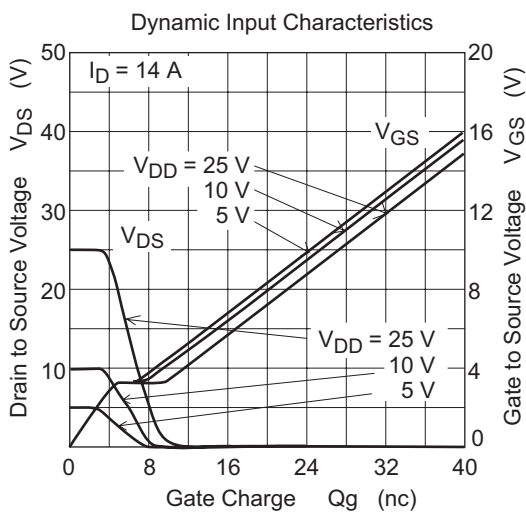
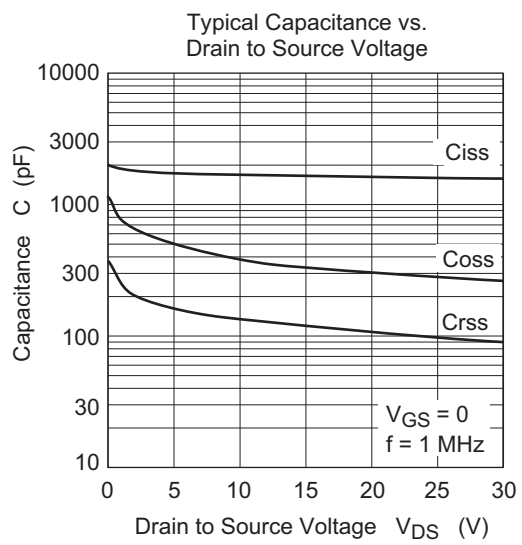
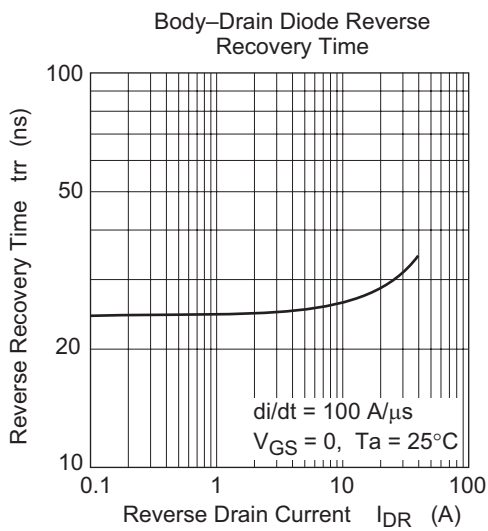
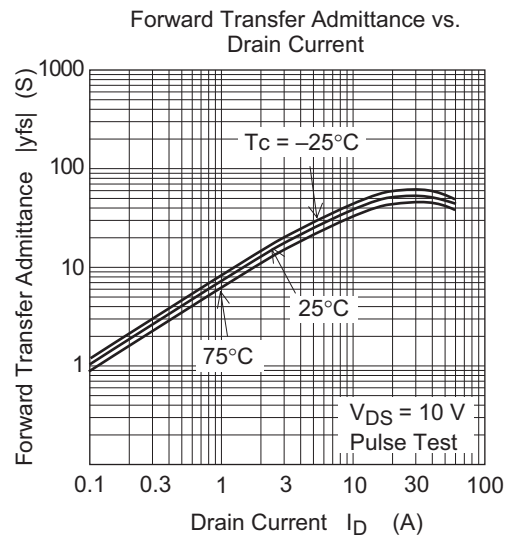
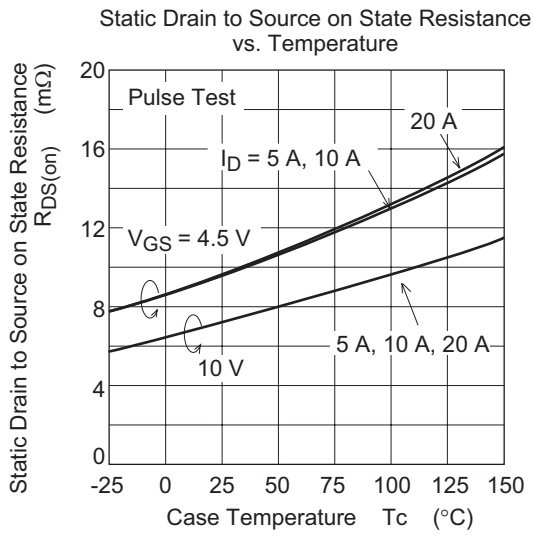
Notes: 4. Pulse test

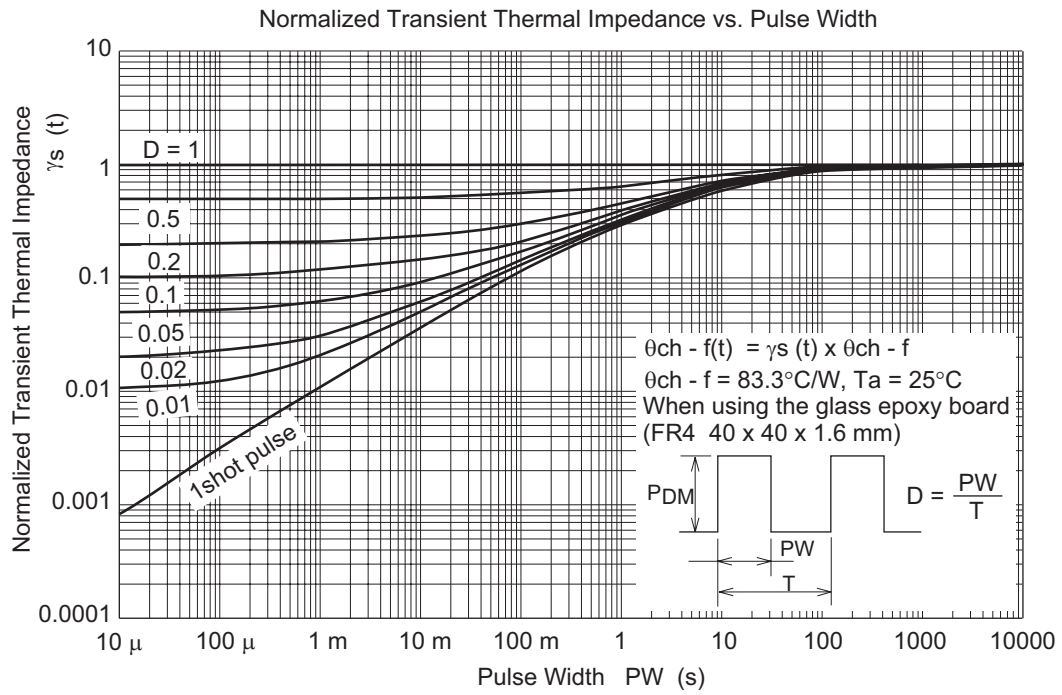
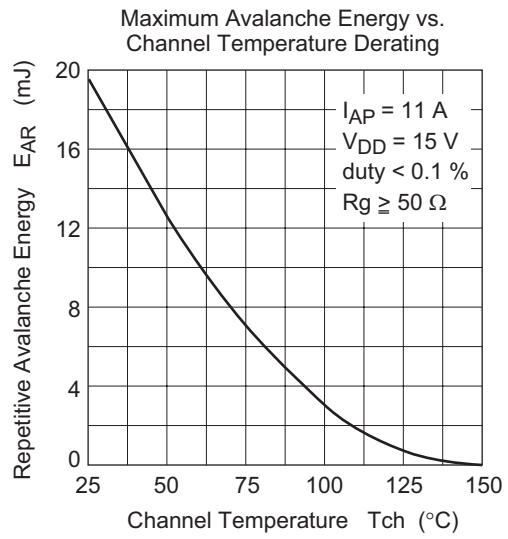
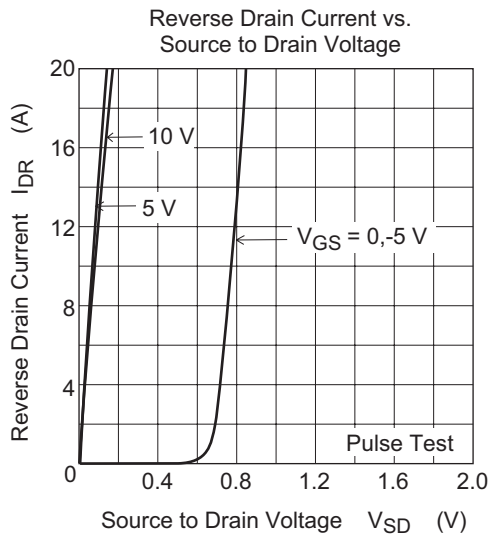
Main Characteristics



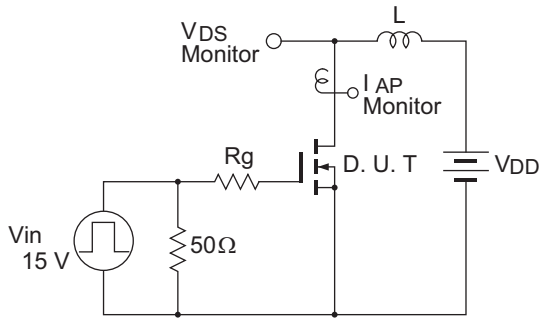
Note 5 :
When using the glass epoxy board (FR4 40x40x1.6 mm)





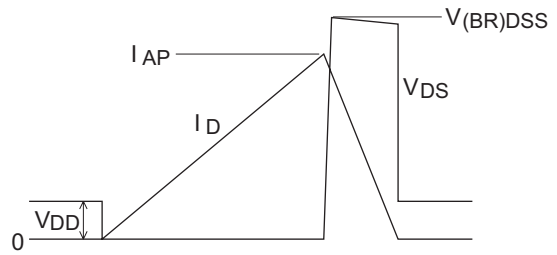


Avalanche Test Circuit

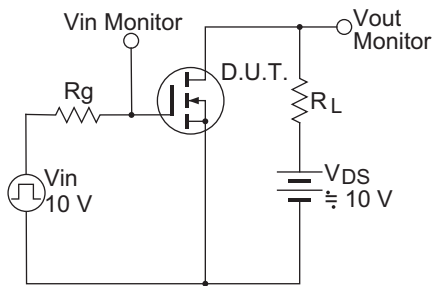


Avalanche Waveform

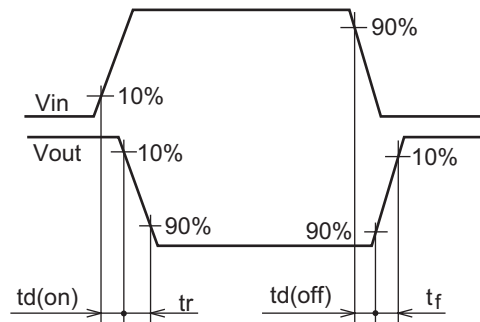
$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit

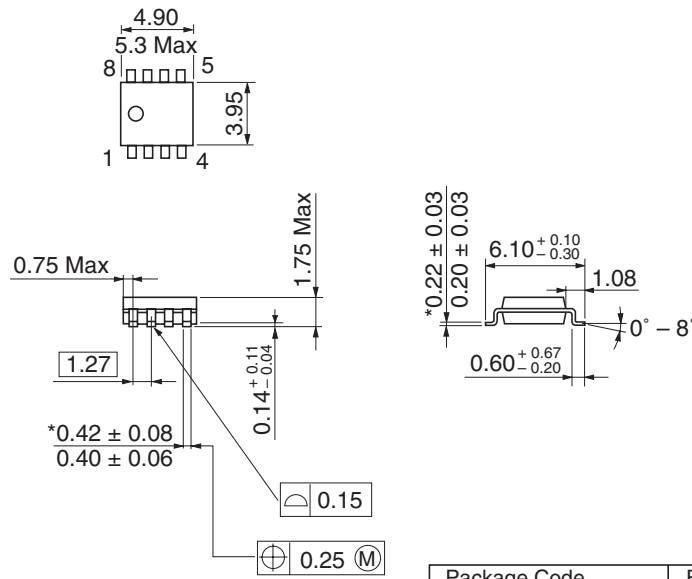


Switching Time Waveform



Package Dimensions

As of January, 2003
Unit: mm



*Dimension including the plating thickness
Base material dimension

Package Code	FP-8DA
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.085 g

Ordering Information

Part Name	Quantity	Shipping Container
HAT2198R-EL-E	2500 pcs	Taping

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