



# P-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A)			
- 60	$0.0145 \text{ at V}_{GS} = -10 \text{ V}$	- 14.4			
	0.019 at V <sub>GS</sub> = - 4.5 V	- 12.6			

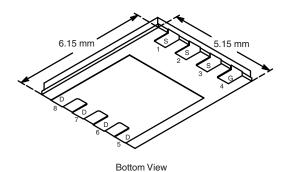
### **FEATURES**

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFETs
- Low Thermal Resistance PowerPAK<sup>®</sup> Package with Low 1.07 mm Profile
- · Compliant to RoHS Directive 2002/95/EC



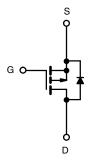


#### PowerPAK SO-8



Ordering Information: Si7461DP-T1-E3 (Lead (Pb)-free)

Si7461DP-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b>	$G(T_A = 25  ^{\circ}C, \text{ unlet})$	ess otherwise	noted)		
Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V <sub>DS</sub>	- 60		V
Gate-Source Voltage		V <sub>GS</sub>	± 20		
Continuous Dusin Comment /T 450 °C)	T <sub>A</sub> = 25 °C	I_	- 14.4	- 8.6	
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 70 °C	- I <sub>D</sub>	- 11.5	- 6.9	
Pulsed Drain Current		I <sub>DM</sub>	- 60		Α
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	- 4.5	- 1.6	
Avalanche Current	L = 1.0 mH	I <sub>AS</sub>	50 125		
Single Pulse Avalanche Energy	L = 1.0 IIII1	E <sub>AS</sub>			
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 25 °C	- P <sub>D</sub>	5.4	1.9	W
	T <sub>A</sub> = 70 °C		3.4	1.2	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) <sup>b, c</sup>				260	C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum lunction to Ambienta	t ≤ 10 s	R <sub>thJA</sub>	18	23	°C/W
Maximum Junction-to-Ambient <sup>a</sup>	Steady State		52	65	
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	1.0	1.3	

#### Notes:

- a. Surface mounted on 1" x 1" FR4 board.
- b. See solder profile (<a href="www.vishay.com/ppg?73257">www.vishay.com/ppg?73257</a>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

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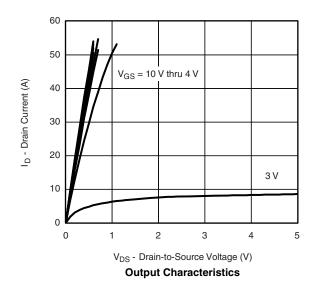
<b>SPECIFICATIONS</b> (T <sub>J</sub> = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 1		- 3	V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 60 V, V <sub>GS</sub> = 0 V			- 1	μА	
		V <sub>DS</sub> = - 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C			- 10		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \le -5 \text{ V}, V_{GS} = -10 \text{ V}$	- 40			Α	
Drain-Source On-State Resistance <sup>a</sup>	D	V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 14.4 A		0.0115	0.0145	Ω	
	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 12.6 A		0.015	0.019		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = - 15 V, I <sub>D</sub> = - 14.4 A		31		S	
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	I <sub>S</sub> = - 4.5 A, V <sub>GS</sub> = 0 V		- 0.8	- 1.2	V	
Dynamic <sup>b</sup>							
Total Gate Charge	$Q_g$			121	190		
Gate-Source Charge	$Q_{gs}$	$V_{DS} = -30 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -14.4 \text{ A}$		20		nC	
Gate-Drain Charge	$Q_{gd}$			32			
Gate Resistance	$R_g$			3		Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			20	30		
Rise Time	t <sub>r</sub>	$V_{DD}$ = - 30 V, $R_L$ = 30 $\Omega$		20	30		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong -1 \text{ A}, V_{GEN} = -10 \text{ V}, R_g = 6 \Omega$		205	310	ns	
Fall Time	t <sub>f</sub>			90	135		
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 4.5 A, dl/dt = 100 A/μs		45	70		

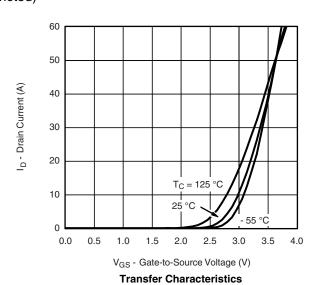
#### Notes:

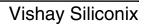
- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

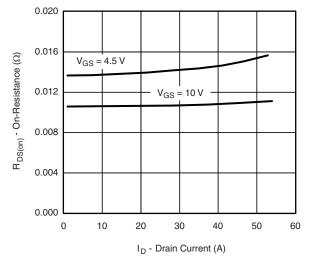




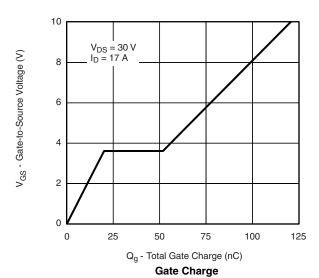


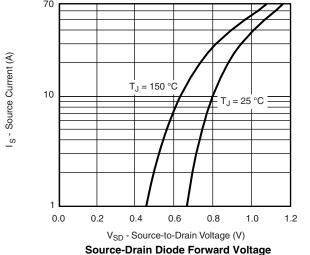


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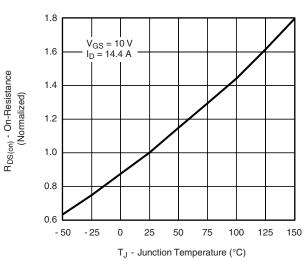
#### On-Resistance vs. Drain Current



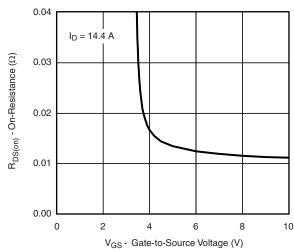


8000 7000  $C_{iss}$ 6000 C - Capacitance (pF) 5000 4000 3000 2000 1000 0 0 10 20 30 40 50 60  $V_{DS}$  - Drain-to-Source Voltage (V)

Capacitance



On-Resistance vs. Junction Temperature

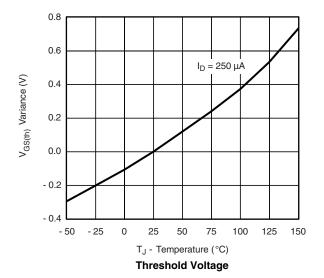


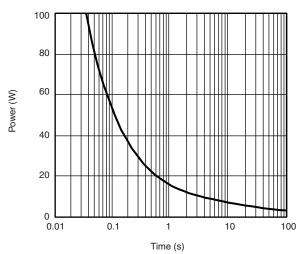
On-Resistance vs. Gate-to-Source Voltage

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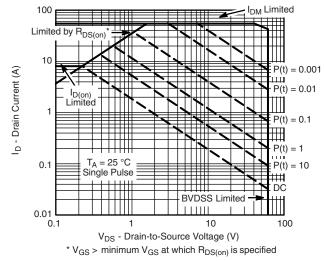
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## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

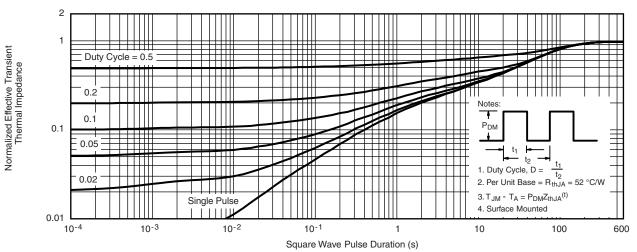




Single Pulse Power, Junction-to-Ambient



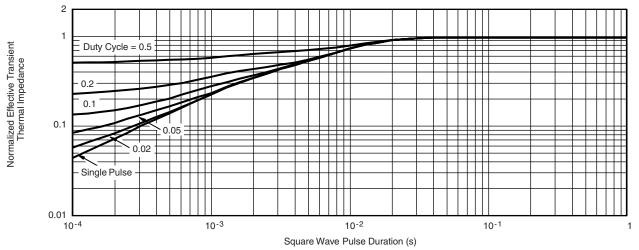
#### **Safe Operating Area**



Normalized Thermal Transient Impedance, Junction-to-Ambient



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppq?72567">www.vishay.com/ppq?72567</a>.

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