IXYS

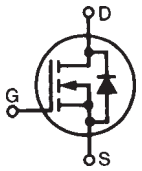
Advance Technical Information

High Current MegaMOS™FET

IXTK 160N20

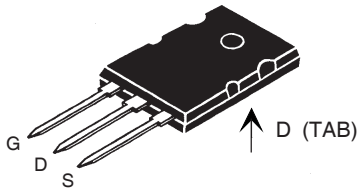
V_{DSS} = 200 V
I_{D25} = 160 A
$R_{DS(on)}$ = 13 mΩ

N-Channel Enhancement Mode



Symbol	Test conditions	Maximum ratings	
V_{DSS}	T_J = 25°C to 150°C	200	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1.0 MΩ	200	V
V_{GS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C MOSFET chip capability	160	A
$I_{D(RMS)}$	External lead current limit	75	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	640	A
I_{AR}	T_C = 25°C	90	A
E_{AR}	T_C = 25°C	80	mJ
E_{AS}	T_C = 25°C	4.0	J
dv/dt	$I_S \le I_{DM}$, di/dt ≤ 100 A/µs, $V_{DD} \le V_{DSS}$ $T_J \le$ 150°C, R_G = 2 Ω	5	V/ns
P_D	T_C = 25°C	730	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6 mm (0.063 in.) from case for 10 s	300	°C
M_d	Mounting torque	0.7/6	Nm/lb.in.
Weight	TO-264	10	g

TO-264 AA (IXTK)



G = Gate D = Drain
S = Source Tab = Drain

Symbol	Test Conditions (T_J = 25°C unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
V_{DSS}	V_{GS} = 0 V, I_D = 1 mA	200			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	2.0		4.0	V
I_{GSS}	V_{GS} = ±20 V DC, V_{DS} = 0			±200	nA
I_{DSS}	$V_{DS} = V_{DSS}$ V_{GS} = 0 V; T_J = 25°C			50	µA
	T_J = 125°C			3	mA
$R_{DS(on)}$	V_{GS} = 10 V, $I_D = 0.5\ I_{D25}$ Pulse test, t ≤ 300 ms, duty cycle d ≤ 2%			13	mΩ

Features

- Low $R_{DS\ (on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- International standard package
- Fast switching times

Applications

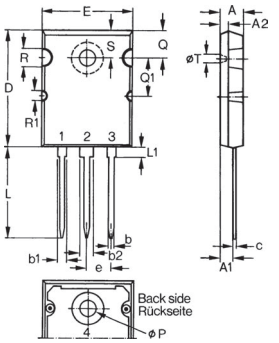
- Motor controls
- DC choppers
- Switched-mode power supplies

Advantages

- Easy to mount with one screw (isolated mounting screw hole)
- Space savings
- High power density

Symbol	Test Conditions (T_J = 25°C unless otherwise specified)	Characteristic values Min.	Typ.	Max.	
g_{fs}	V_{DS} = 10 V; I_D = 0.5 I_{D25}, pulse test	75	95		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		12900		pF
C_{oss}			2220		pF
C_{rss}			730		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, I_D = 0.5 I_{D25} R_G = 1.0 Ω (External)		30		ns
t_r			38		ns
$t_{d(off)}$			150		ns
t_f			30		ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, I_D = 0.5 I_{D25}		415		nC
Q_{gs}			63		nC
Q_{gd}			200		nC
R_{thJC}				0.17	K/W
R_{thCK}			0.15		K/W

TO-264 AA Outline



Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.82	5.13	.190	.202
A1	2.54	2.89	.100	.114
A2	2.00	2.10	.079	.083
b	1.12	1.42	.044	.056
b1	2.39	2.69	.094	.106
b2	2.90	3.09	.114	.122
c	0.53	0.83	.021	.033
D	25.91	26.16	1.020	1.030
E	19.81	19.96	.780	.786
e	5.46 BSC		.215 BSC	
J	0.00	0.25	.000	.010
K	0.00	0.25	.000	.010
L	20.32	20.83	.800	.820
L1	2.29	2.59	.090	.102
P	3.17	3.66	.125	.144
Q	6.07	6.27	.239	.247
Q1	8.38	8.69	.330	.342
R	3.81	4.32	.150	.170
R1	1.78	2.29	.070	.090
S	6.04	6.30	.238	.248
T	1.57	1.83	.062	.072

Source-Drain Diode **Ratings and Characteristics** (T_J = 25°C unless otherwise specified)

Symbol	Test Conditions	Min.	Typ.	Max.	
I_S	V_{GS} = 0V			160	A
I_{SM}	Repetitive; pulse width limited by T_{JM}			640	A
V_{SD}	I_F = I_S, V_{GS} = 0 V, Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %			1.5	V
t_{rr}	I_F = 25A, -di/dt = 100 A/µs, V_R = 100V		250		ns
Q_{rr}			3		µC

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,881,106 5,017,508 5,049,961 5,187,117 5,486,715 6,306,728B1 6,259,123B1 6,306,728B1 4,850,072 4,931,844 5,034,796 5,063,307 5,237,481 5,381,025 6,404,065B1 6,162,665 6,534,343

Fig. 1. Output Characteristics @ 25ºC

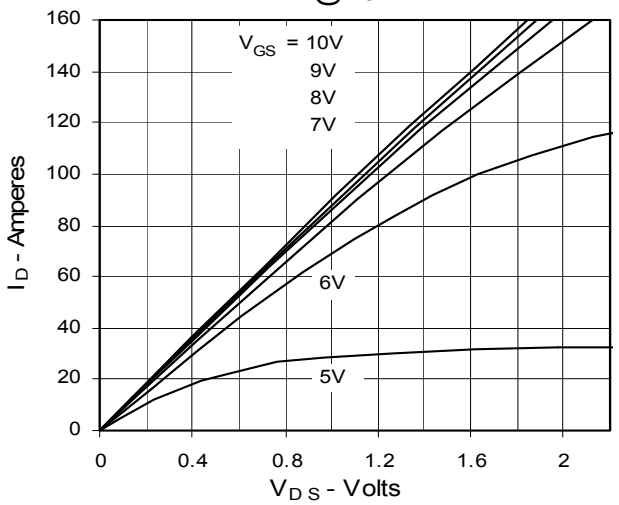


Fig. 2. Extended Output Characteristics @ 25ºC

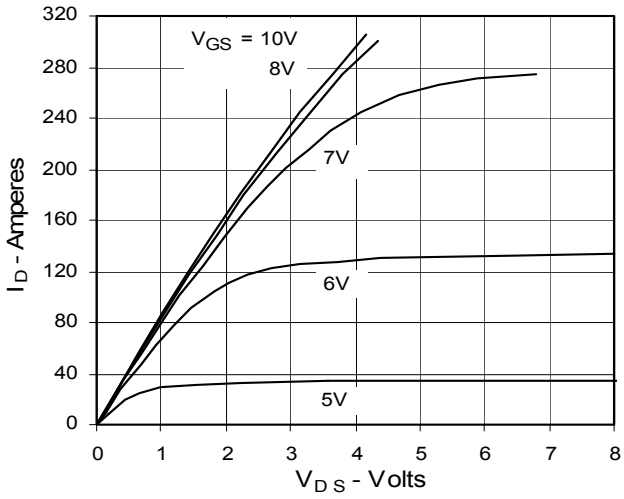


Fig. 3. Output Characteristics @ 125ºC

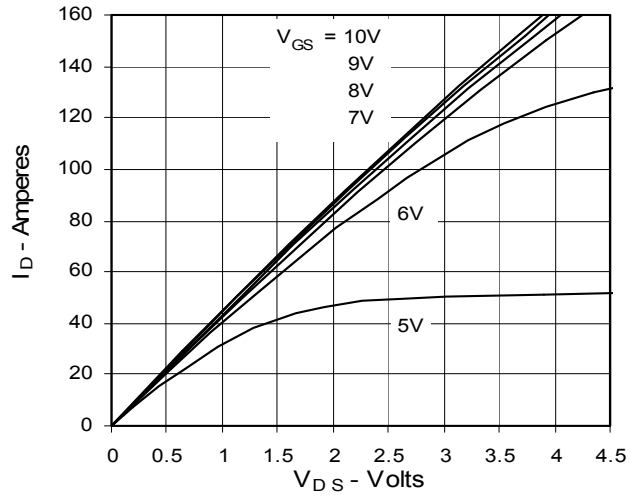


Fig. 4. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. Junction Temperature

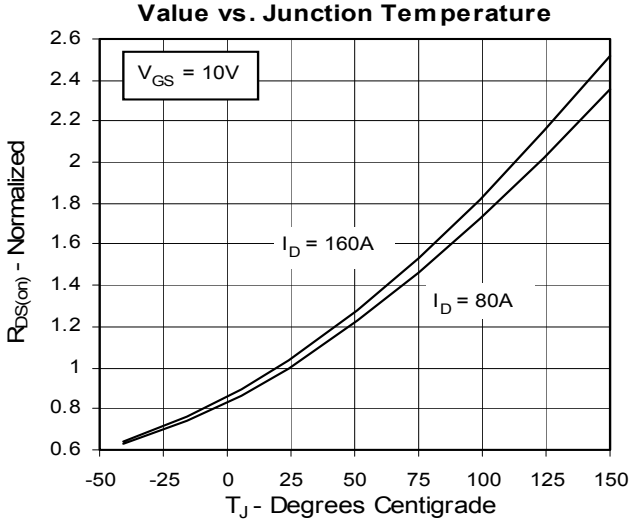


Fig. 5. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. I_D

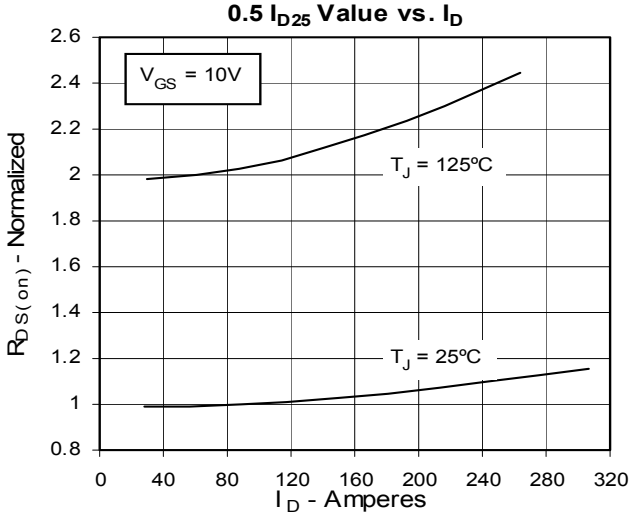


Fig. 6. Drain Current vs. Case Temperature

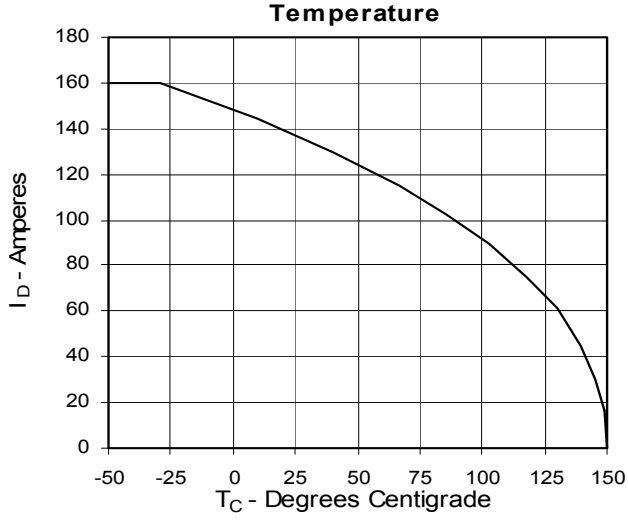


Fig. 7. Input Admittance

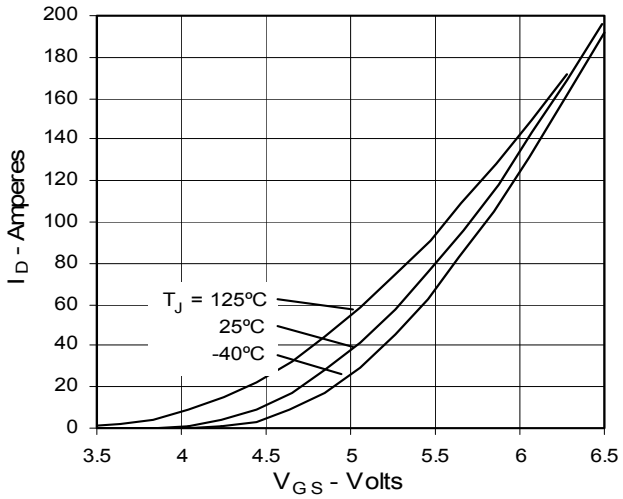


Fig. 8. Transconductance

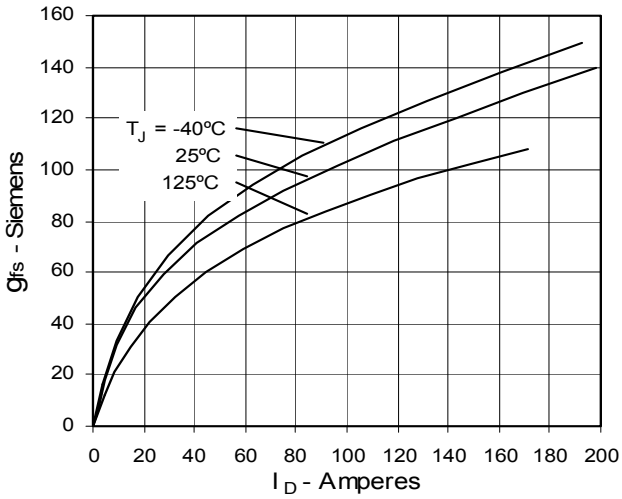


Fig. 9. Source Current vs. Source-To-Drain Voltage

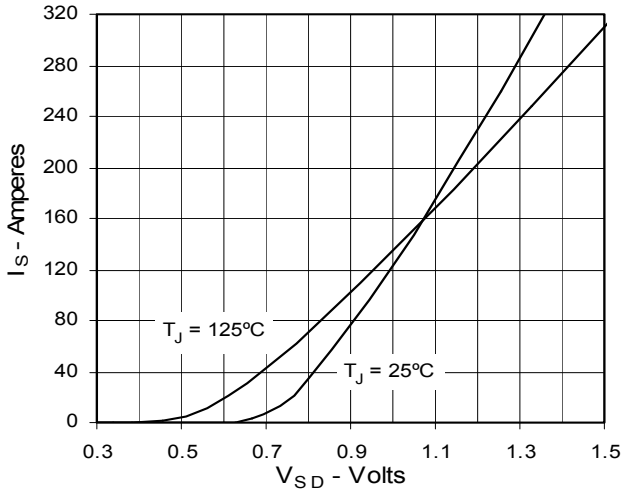


Fig. 10. Gate Charge

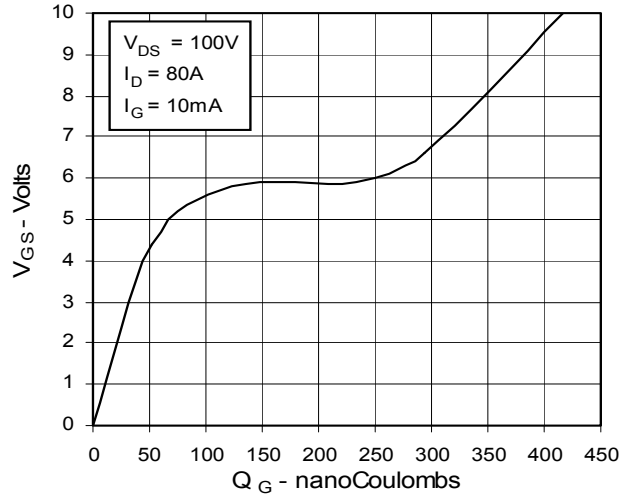


Fig. 11. Capacitance

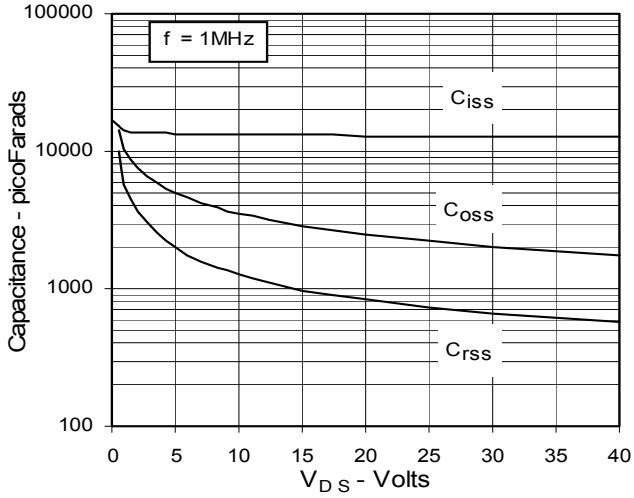


Fig. 12. Forward-Bias Safe Operating Area

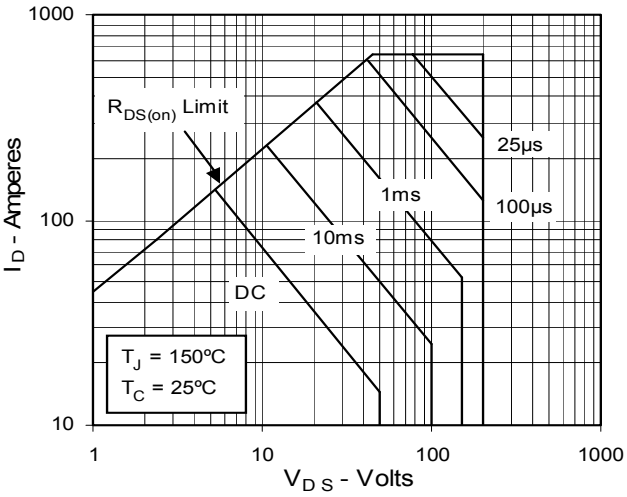


Fig. 13. Maximum Transient Thermal Resistance