IXYS

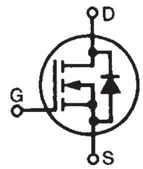
PolarHV™ HiPerFET Power MOSFET ISOPLUS264™

IXFL 100N50P

(Electrically Isolated Back Surface)

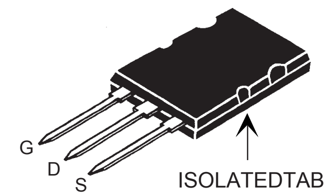
N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Diode

V_{DSS}	=	500	V
I_{D25}	=	70	A
$R_{DS(on)}$	≤	52	mΩ
t_{rr}	≤	200	ns



Symbol	Test Conditions		Maximum Ratings	
V_{DSS}	T_J = 25° C to 150° C		500	V
V_{DGR}	T_J = 25° C to 150° C; R_{GS} = 1 MΩ		500	V
V_{GSS}	Continuous		±30	V
V_{GSM}	Transient		±40	V
I_{D25}	T_C = 25° C		70	A
I_{DM}	T_C = 25° C, pulse width limited by T_{JM}		250	A
I_{AR}	T_C = 25° C		100	A
E_{AR}	T_C = 25° C		100	mJ
E_{AS}	T_C = 25° C		5	J
dv/dt	I_S ≤ I_{DM}, di/dt ≤ 100 A/µs, V_{DD} ≤ V_{DSS}, T_J ≤ 150° C, R_G = 2 Ω		20	V/ns
P_D	T_C = 25° C		625	W
T_J			-55 ... +150	°C
T_{JM}			150	°C
T_{stg}			-55 ... +150	°C
T_L	1.6 mm (0.062 in.) from case for 10 s		300	°C
V_{ISOL}	50/60 Hz, RMS	t = 1 min	2500	V~
	I_{ISOL} ≤ 1 mA	t = 1 s	3000	V~
F_C	Mounting force		28..150 / 6.4..30	N/lb
Weight			5	g

ISOPLUS264



G = Gate D = Drain
S = Source

Features

- International standard isolated package
- UL recognized package
- Silicon chip on Direct-Copper-Bond substrate
  - High power dissipation
  - Isolated mounting surface
  - 2500V electrical isolation
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
  - easy to drive and to protect
- Fast intrinsic diode

Advantages

- Easy to mount
- Space savings
- High power density

Symbol	Test Conditions (T_J = 25° C, unless otherwise specified)		Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0 V, I_D = 3 mA		500			V
$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 8 mA		3.0		5.0	V
I_{GSS}	V_{GS} = ±30 V_{DC}, V_{DS} = 0				±200	nA
I_{DSS}	V_{DS} = V_{DSS}				25	µA
	V_{GS} = 0 V	T_J = 125° C			2000	µA
$R_{DS(on)}$	V_{GS} = 10 V, I_D = I_T, Note 1				52	mΩ

Symbol	Test Conditions	Min.	Typ.	Max.	
	Characteristic Values (T_J = 25° C, unless otherwise specified)				
g_{fs}	V_{DS} = 20 V; I_D = I_T, Note 1	50	80		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		20		nF
C_{oss}			1700		pF
C_{rss}			140		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, I_D = I_T		36		ns
t_r	R_G = 1 Ω (External)		29		ns
$t_{d(off)}$			110		ns
t_f			26		ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, I_D = I_T		240		nC
Q_{gs}			96		nC
Q_{gd}			78		nC
R_{thJC}				0.20	°C/W
R_{thCS}			0.13		°C/W

Source-Drain Diode

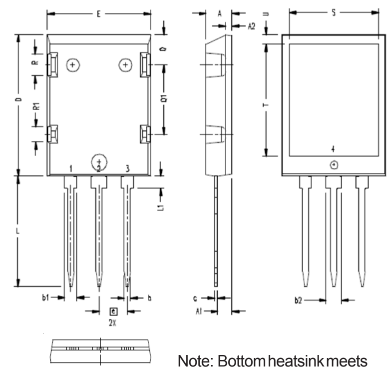
Symbol	Test Conditions	Min.	Typ.	Max.	
	Characteristic Values (T_J = 25° C, unless otherwise specified)				
I_S	V_{GS} = 0 V			100	A
I_{SM}	Repetitive			250	A
V_{SD}	I_F = I_S, V_{GS} = 0 V, Note 1			1.5	V
t_{rr}	I_F = 25A, -di/dt = 100 A/μs			200	ns
Q_{RM}	V_R = 100V		0.6		μC
I_{RM}			6.0		A

Notes:

1. Pulse test, t ≤300 μs, duty cycle d≤ 2 %

Test Current I_T = 50 A

ISOPLUS264 (IXFL) Outline



Note: Bottom heatsink meets 2500Vrms Isolation to the other pins.

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	190	205	4.83	5.21
A1	.102	.118	2.59	3.00
A2	.046	.055	1.17	1.40
b	.045	.055	1.14	1.40
b1	.087	.102	2.21	2.59
b2	.111	.126	2.82	3.20
c	.020	.029	0.51	0.74
D	1.020	1.040	25.91	26.42
E	.770	.799	19.56	20.29
e	215 BSC		5.46 BSC	
L	.780	.820	19.81	20.83
L1	.080	.102	2.03	2.59
Q	.210	.235	5.33	5.97
Q1	.490	.513	12.45	13.03
R	150	180	3.81	4.57
R1	.100	.130	2.54	3.30
S	668	690	16 97	17 53
T	.801	.821	20.34	20.85
U	.065	.080	1.65	2.03

Ref: IXYS CO 0128 R0

Fig. 1. Output Characteristics @ 25ºC

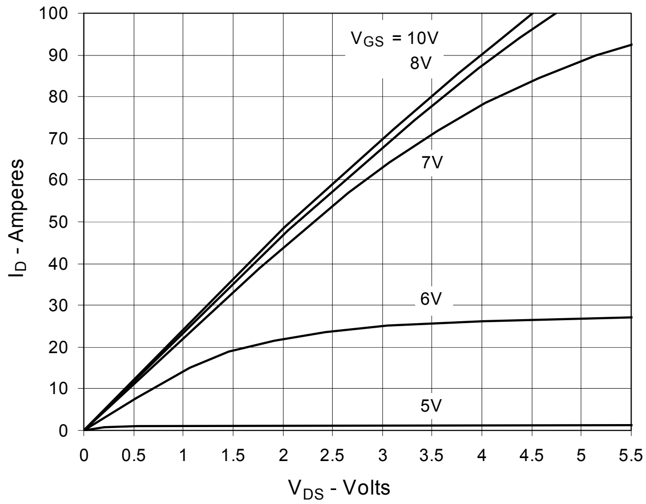


Fig. 2. Extended Output Characteristics @ 25ºC

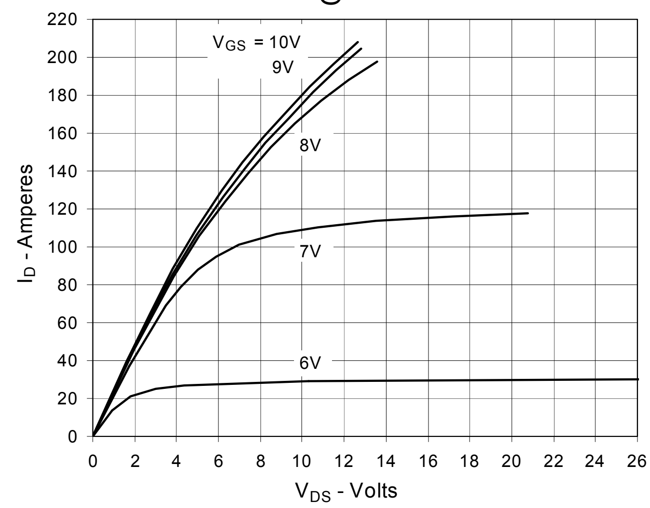


Fig. 3. Output Characteristics @ 125ºC

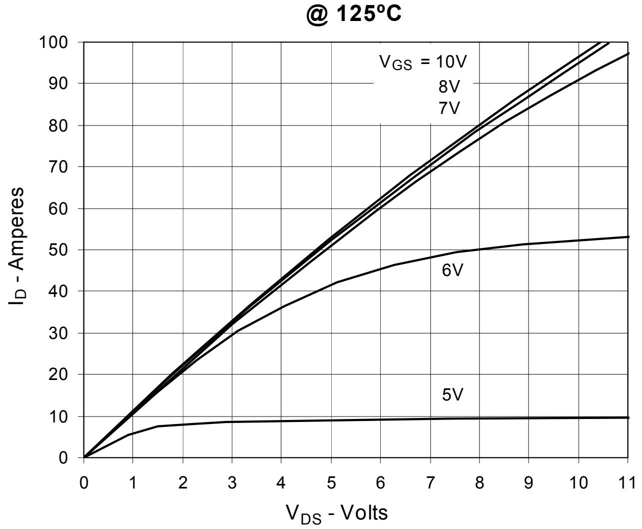


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 50A Value vs. Junction Temperature

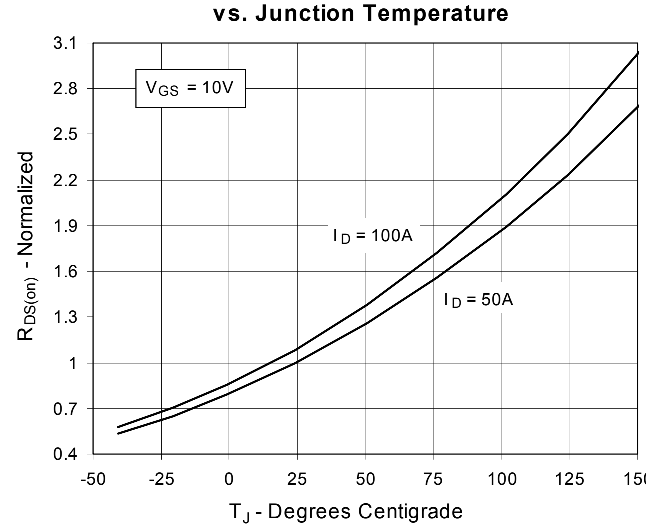


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 50A Value vs. Drain Current

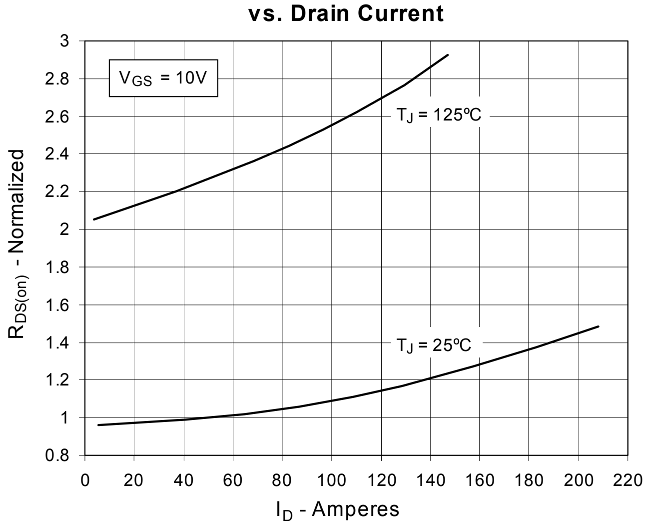


Fig. 6. Maximum Drain Current vs. Case Temperature

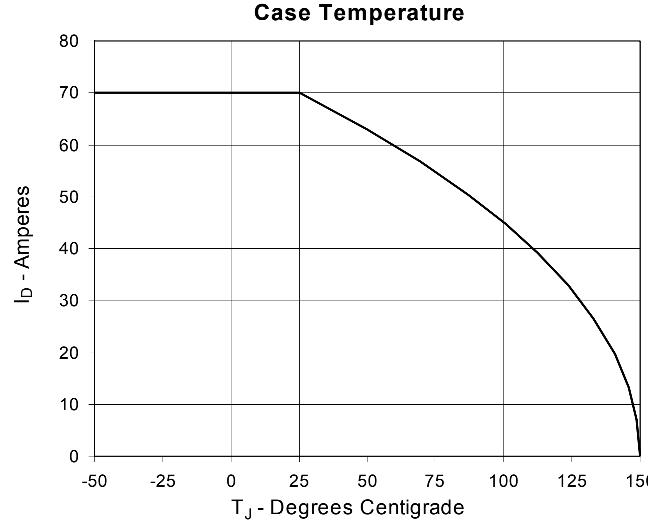


Fig. 7. Input Admittance

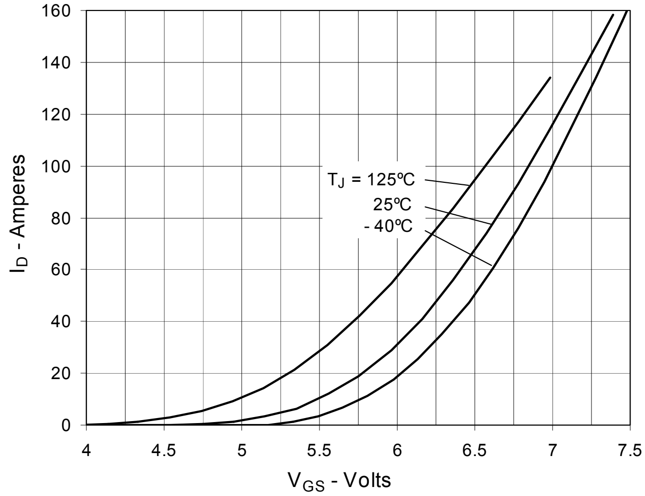


Fig. 8. Transconductance

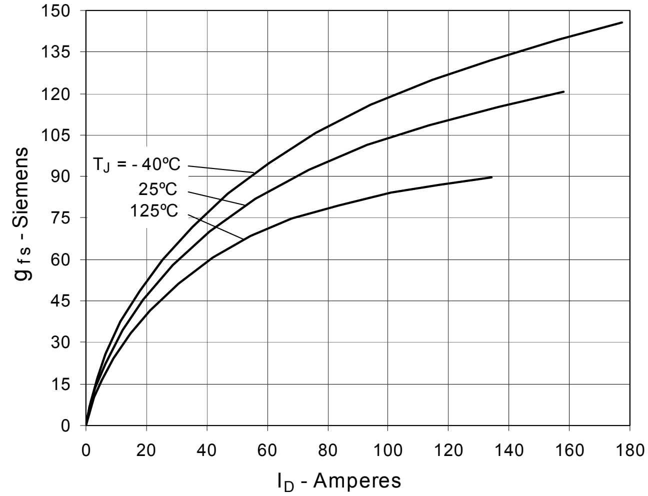


Fig. 9. Forward Voltage Drop of Intrinsic Diode

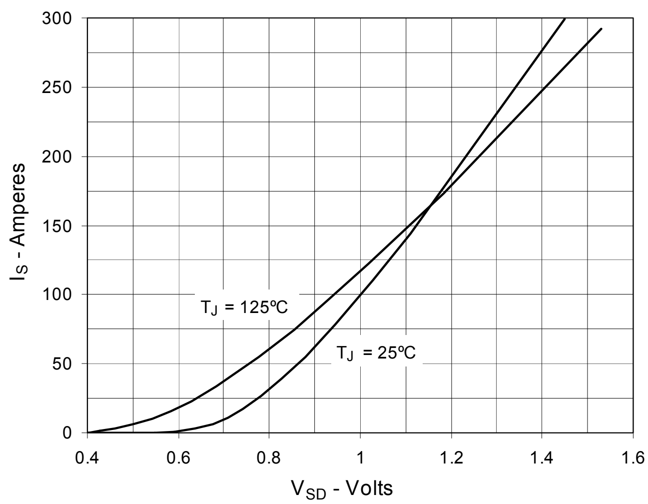


Fig. 10. Gate Charge

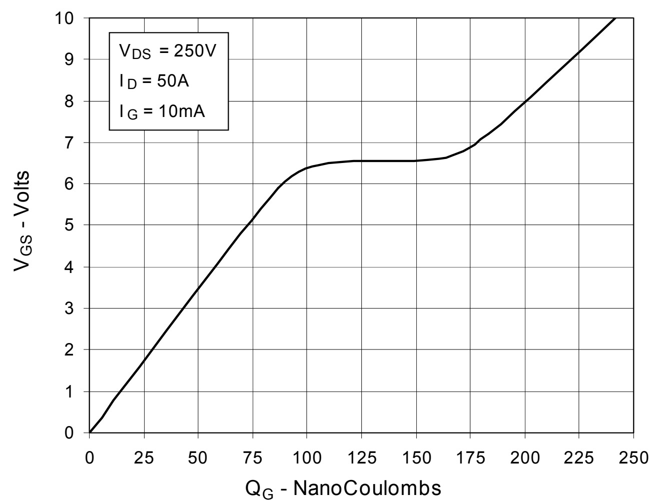


Fig. 11. Capacitance

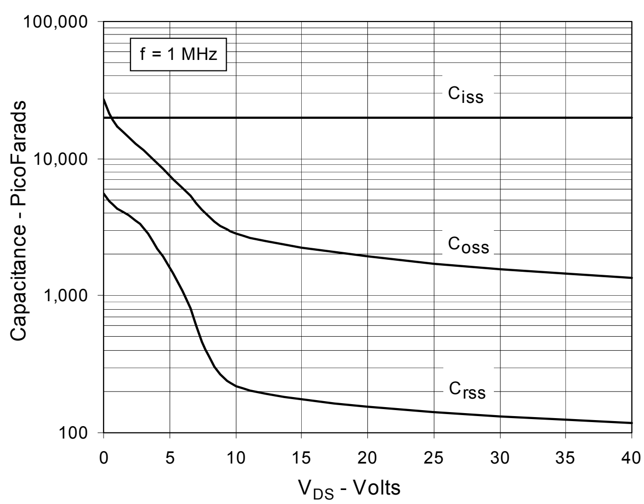
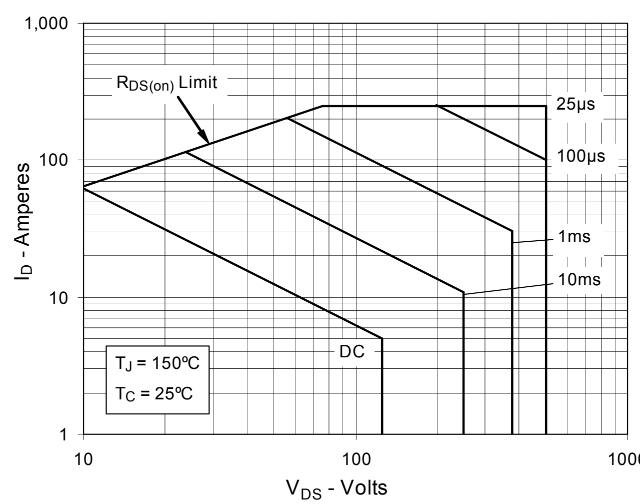


Fig. 12. Forward-Bias Safe Operating Area



IXYS reserves the right to change limits, test conditions, and dimensions.

Fig. 13. Maximum Transient Thermal Resistance