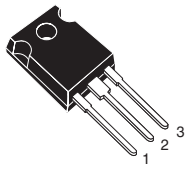
STW9N150

N-channel 1500 V - 1.8 Ω - 8 A - TO-247 very high voltage PowerMESH™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STW9N150	1500 V	< 2.5 Ω	8 A	320 W

- 100% avalanche tested
- Avalanche ruggedness
- Gate charge minimized
- Very low intrinsic capacitances
- High speed switching
- Very low on-resistance



TO-247

Application

- Switching applications

Description

Using the well consolidated high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of Power MOSFETs with outstanding performances. The strengthened layout coupled with the company's proprietary edge termination structure, gives the lowest $R_{DS(on)}$ per area, unrivalled gate charge and switching characteristics.

Figure 1. Internal schematic diagram

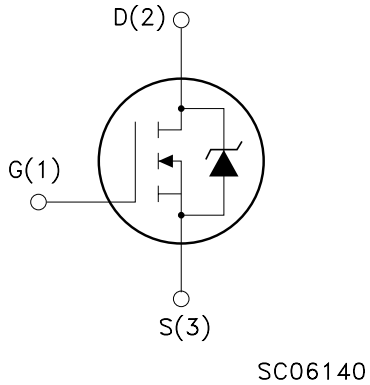


Table 1. Device summary

Order code	Marking	Package	Packaging
STW9N150	9N150	TO-247	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	1500	V
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	8	A
I_D	Drain current (continuous) at T_C = 100 °C	5	A
I_{DM} (1)	Drain current (pulsed)	32	A
P_{TOT}	Total dissipation at T_C = 25 °C	320	W
	Derating factor	2.56	W/°C
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	0.39	°C/W
Rthj-amb	Thermal resistance junction-ambient max	50	°C/W
T_J	Maximum lead temperature for soldering purpose	300	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	8	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	720	mJ

2 Electrical characteristics

(Tcase =25°C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	1500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0) V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C				10 500	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 30 V			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 4 A		1.8	2.5	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D = 4 A		7.5		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		3255 294 22.4		pF pF pF
$C_{oss\ eq.}$	Equivalent Output capacitance	V_{GS} = 0, V_{DS} = 0 to 1200 V		118		pF
R_g	Gate input resistance	f=1MHz Gate DC Bias=0 Test signal level=20 mV open drain		2.4		Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 1200 V, I_D = 8 A, V_{GS} = 10 V *(see Figure 15)*		89.3 15.8 50.4		nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 750 V, I_D = 4 A, R_G = 4.7 Ω, V_{GS} = 10 V *(see Figure 14)*		41 14.7 86 52		ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				8 32	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 8 A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 8 A, di/dt = 100 A/µs V_{DD}= 60 V *(see Figure 16)*		988 9.5 19.3		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 8 A, di/dt = 100 A/µs V_{DD}= 60 V T_J = 150 °C *(see Figure 16)*		884 8.2 18.6		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

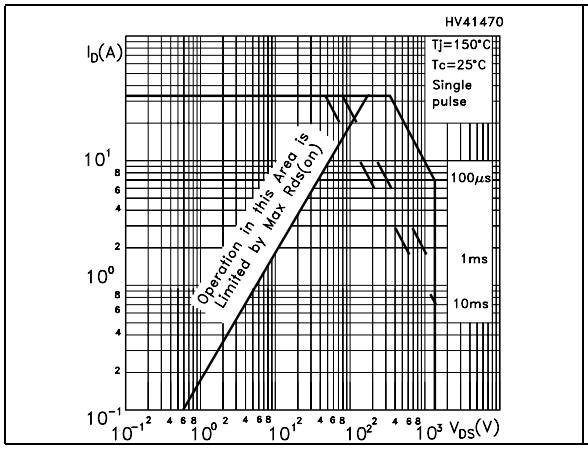


Figure 3. Thermal impedance

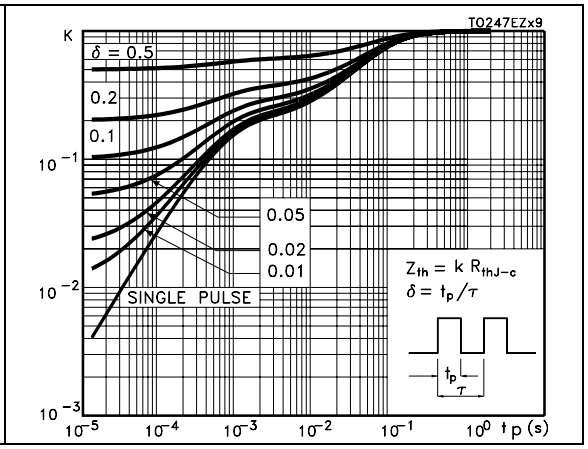


Figure 4. Output characteristics

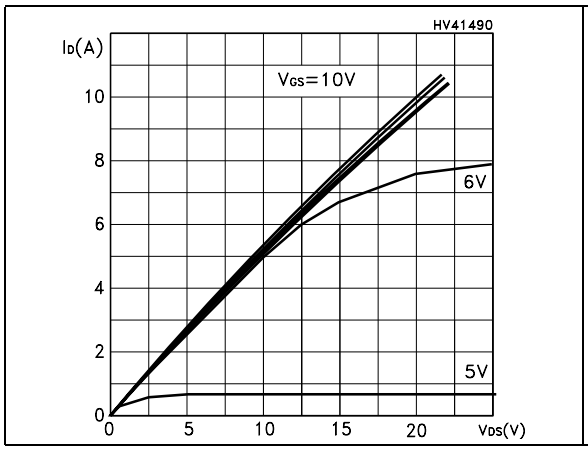


Figure 5. Transfer characteristics

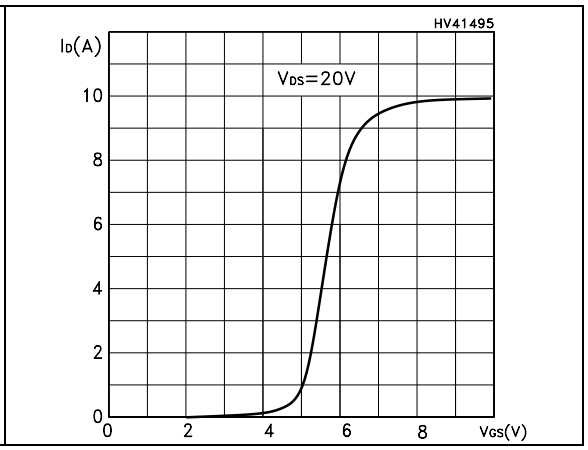


Figure 6. Normalized BV_{DSS} vs temperature

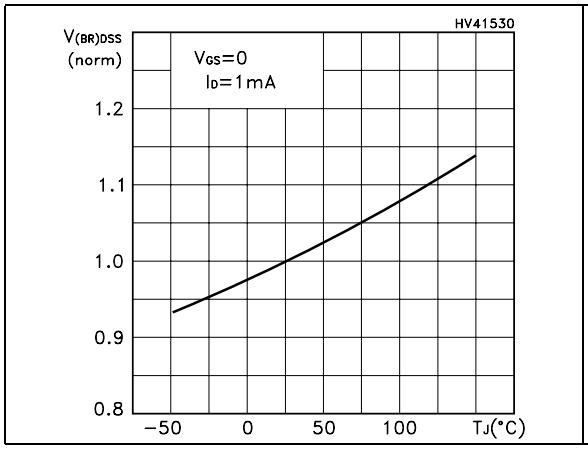


Figure 7. Static drain-source on resistance

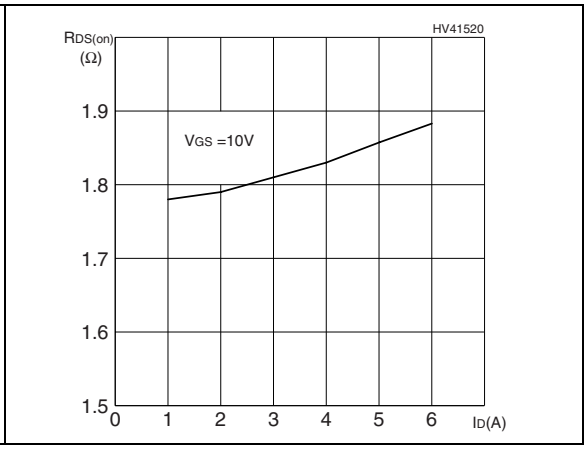


Figure 8. Gate charge vs gate-source voltage

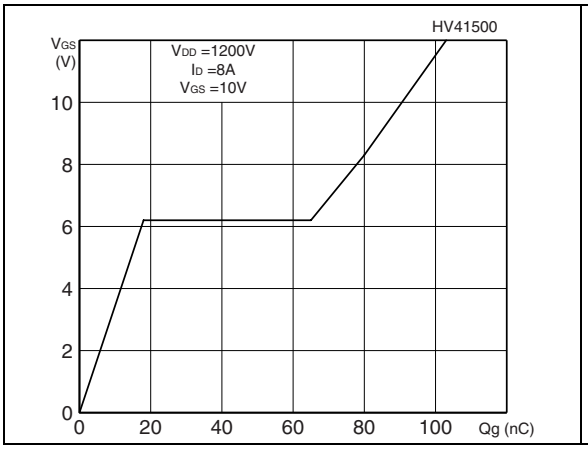


Figure 9. Capacitance variations

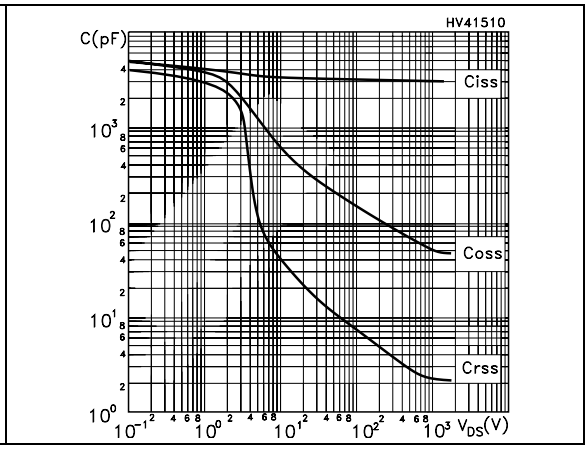


Figure 10. Normalized gate threshold voltage vs temperature

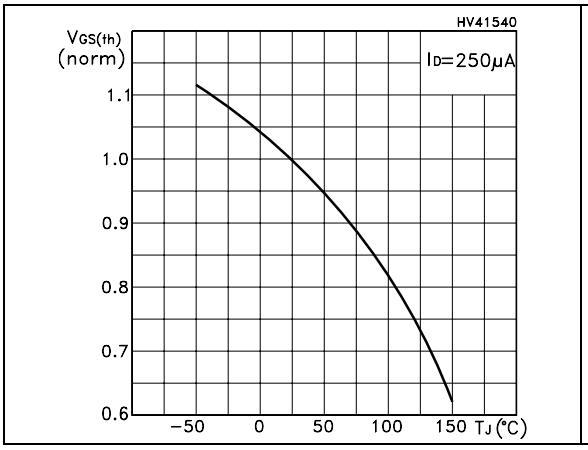


Figure 11. Normalized on resistance vs temperature

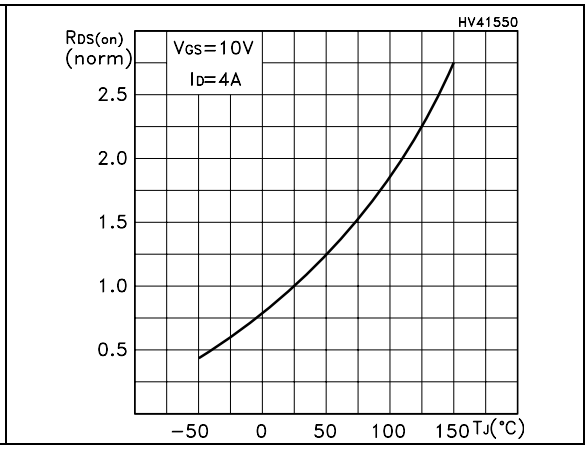


Figure 12. Source-drain diode forward characteristics

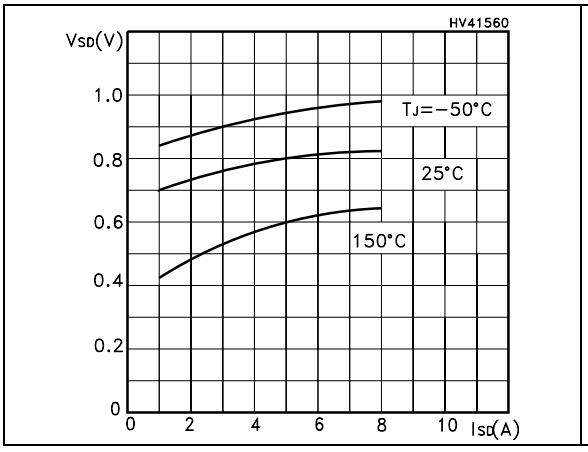
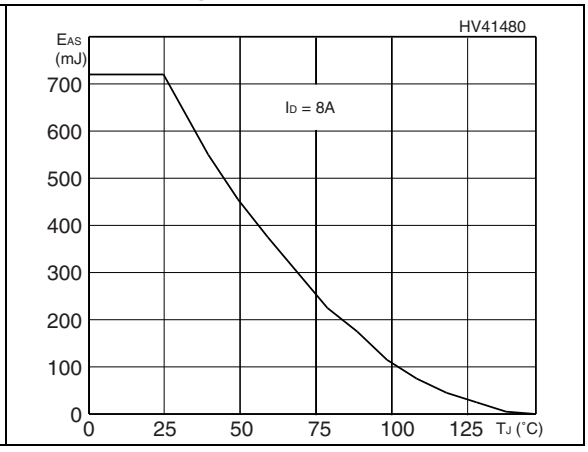


Figure 13. Maximum avalanche energy vs temperature



3 Test circuits

Figure 14. Switching times test circuit for resistive load

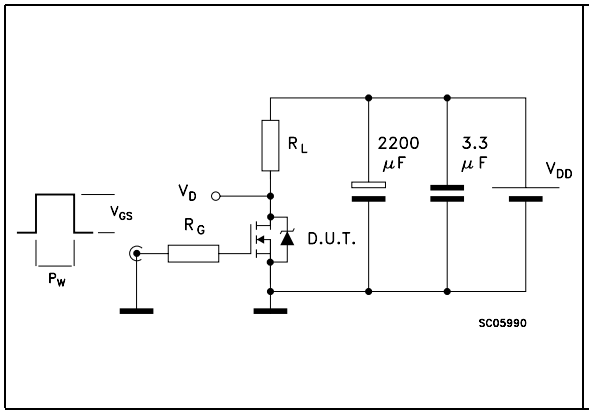


Figure 15. Gate charge test circuit

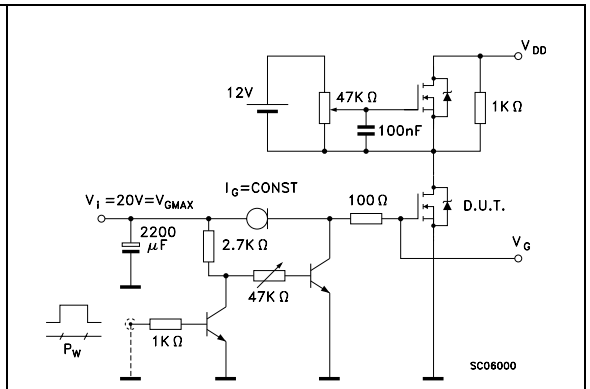


Figure 16. Test circuit for inductive load switching and diode recovery times

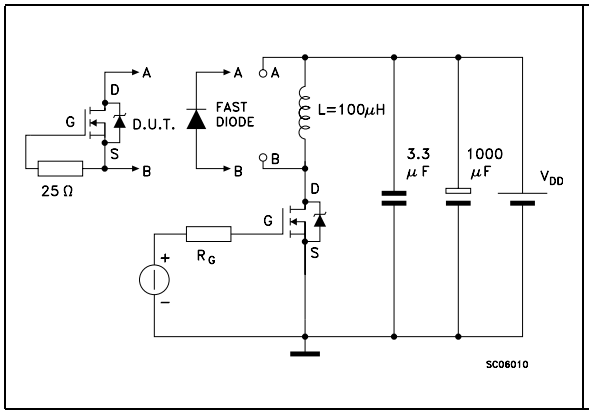


Figure 17. Unclamped Inductive load test circuit

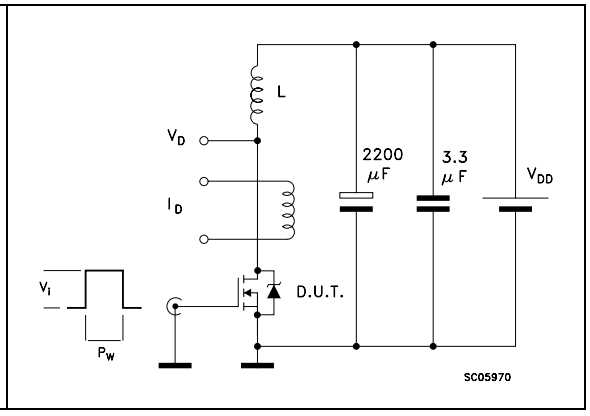


Figure 18. Unclamped inductive waveform

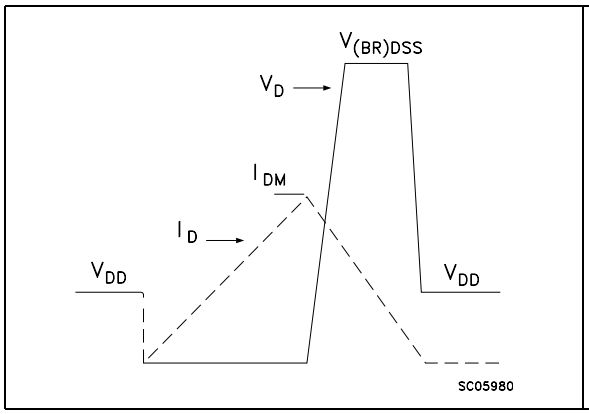
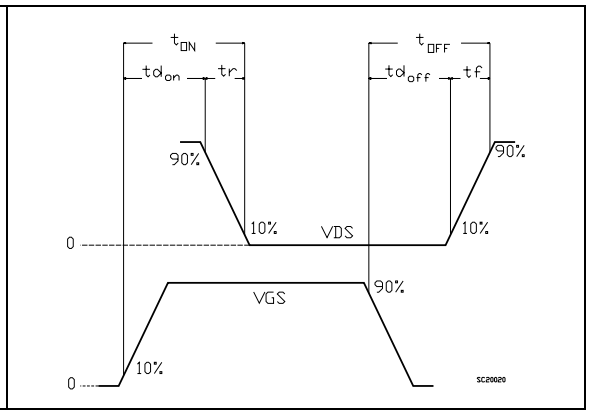


Figure 19. Switching time waveform

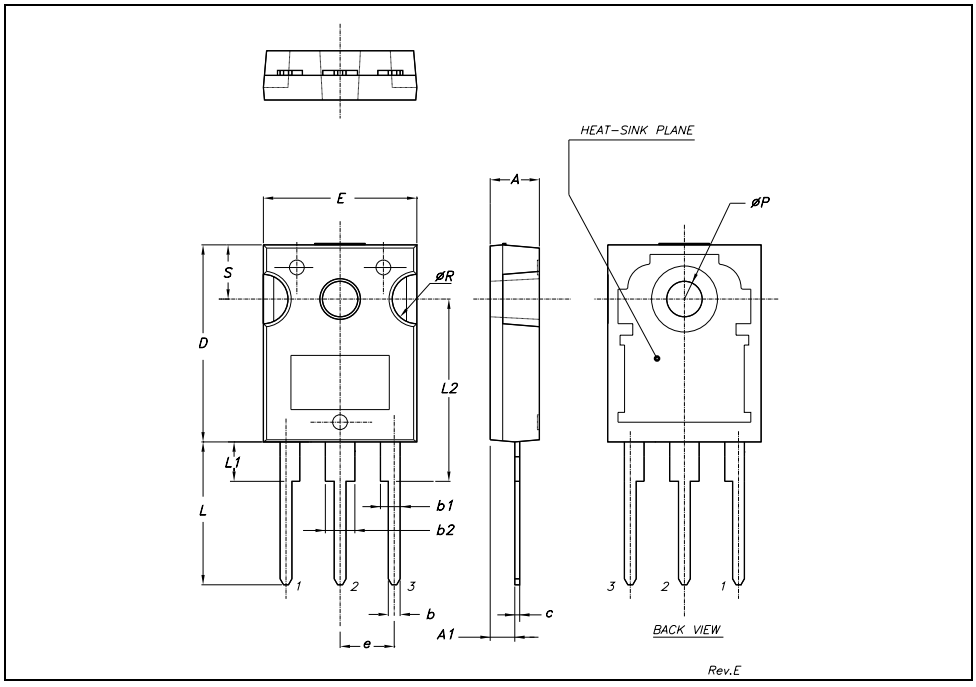


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
24-May-2007	1	First release
04-Jan-2007	2	Document status promoted from preliminary data to datasheet

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