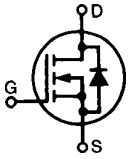
IXYS

HiPerFET™ Power MOSFETs

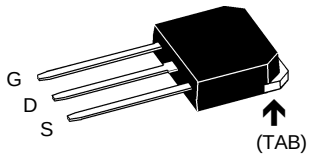
IXFJ 13N50

V_{DSS} = 500 V
$I_{D (cont)}$ = 13 A
$R_{DS(on)}$ = 0.4 Ω
t_{rr} ≤ 250 ns

N-Channel Enhancement Mode
High dv/dt, Low t_{rr}, HDMOS™ Family



Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	500	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ	500	V
V_{GS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C	13	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	52	A
I_{AR}	T_C = 25°C	13	A
E_{AR}	T_C = 25°C	18	mJ
dv/dt	$I_S \le I_{DM}$, di/dt ≤ 100 A/μs, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$, R_G = 2 Ω	5	V/ns
P_D	T_C = 25°C	180	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6 mm (0.062 in.) from case for 10 s	300	°C
Weight		5	g



G = Gate, D = Drain,
S = Source, TAB = Drain

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 250 μA	500			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 2.5 mA	2		4	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0			±100	nA
I_{DSS}	$V_{DS} = 0.8 \cdot V_{DSS}$, V_{GS} = 0 V; T_J = 25°C			200	μA
				1	mA
	T_J = 125°C				
$R_{DS(on)}$	V_{GS} = 10 V, $I_D = 0.5 \cdot I_{D25}$, Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %			0.4	Ω

Features

- Low profile, high power package
- Long creep and strike distances
- Easy up-grade path for TO-220 designs
- Low $R_{DS (on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
  - easy to drive and to protect
- Fast intrinsic Rectifier

Applications

- DC-DC converters
- Synchronous rectification
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- AC motor control
- Temperature and lighting controls
- Low voltage relays

Advantages

- High power, low profile package
- Space savings
- High power density

IXYS reserves the right to change limits, test conditions, and dimensions.

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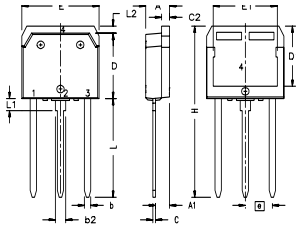
Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
g_{fs}	V_{DS} = 10 V; I_D = 0.5 I_{D25}, pulse test	7.5	9.0		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		2800		pF
C_{oss}			300		pF
C_{rss}			70		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}, R_G = 4.7 Ω (External)		18	30	ns
t_r			27	40	ns
$t_{d(off)}$			76	100	ns
t_f			32	60	ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		110	120	nC
Q_{gs}			15	25	nC
Q_{gd}			40	50	nC
R_{thJC}				0.7	K/W
R_{thCK}			0.25		K/W

Source-Drain Diode

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
I_S	V_{GS} = 0 V				13	A
I_{SM}	Repetitive; pulse width limited by T_{JM}				52	A
V_{SD}	I_F = I_S, V_{GS} = 0 V, Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %				1.5	V
t_{rr}	I_F = I_S, -di/dt = 100 A/µs, V_R = 100 V	T_J = 25°C			250	ns
		T_J = 125°C			350	ns
Q_{RM}		T_J = 25°C		0.6		µC
		T_J = 125°C		1.25		µC
I_{RM}		T_J = 25°C		9		A
		T_J = 125°C		15		A

TO-268 Outline



All metal area are solder plated
1 - gate
2 - drain (collector)
3 - source (emitter)
4 - drain (collector)

Dim.	Inches Min	Inches Max	Millimeters Min	Millimeters Max
A	.193	.201	4.90	5.10
A1	.106	.114	2.70	2.90
b	.045	.057	1.15	1.45
b2	.075	.083	1.90	2.10
C	.016	.026	.040	.065
C2	.057	.063	1.45	1.60
D	.543	.551	13.80	14.00
D1	.488	.500	12.40	12.70
E	.624	.632	15.85	16.05
E1	.524	.535	13.30	13.60
e	.215 BSC		5.45 BSC	
H	1.365	1.395	34.67	35.43
L	.780	.800	19.81	20.32
L1	.079	.091	2.00	2.30
L2	.039	.045	1.00	1.15

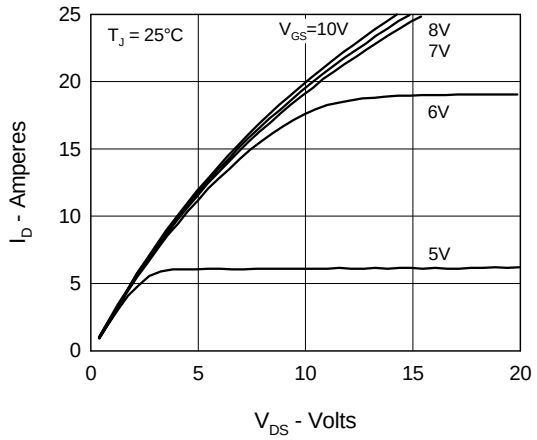


Figure 1. Output Characteristics at 25°C

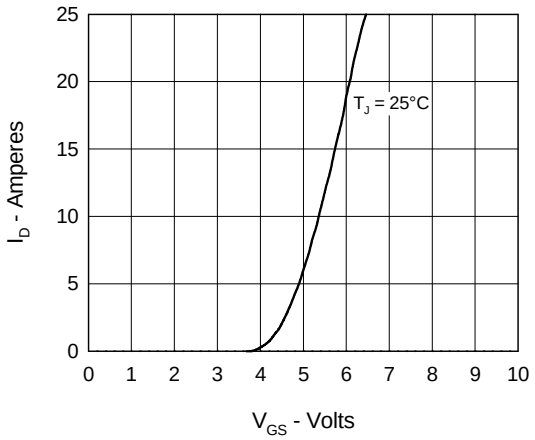


Figure 2. Output Characteristics at 125°C

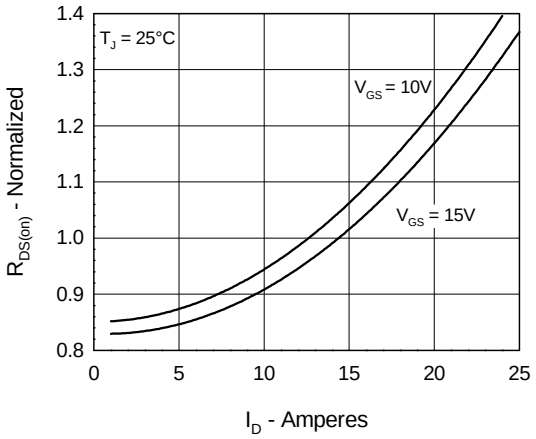


Figure 3. $R_{DS(on)}$ normalized to 0.5 I_{D25} value

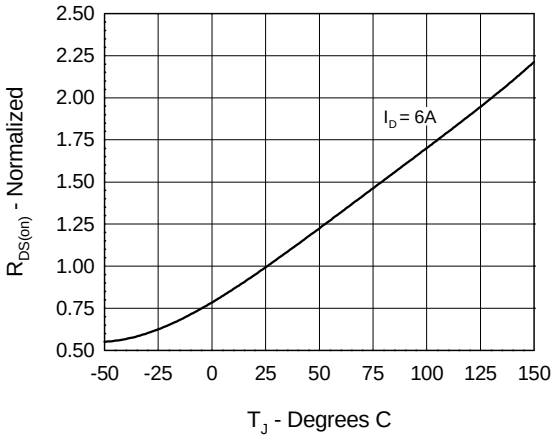


Figure 4. $R_{DS(on)}$ normalized to 0.5 I_{D25} value

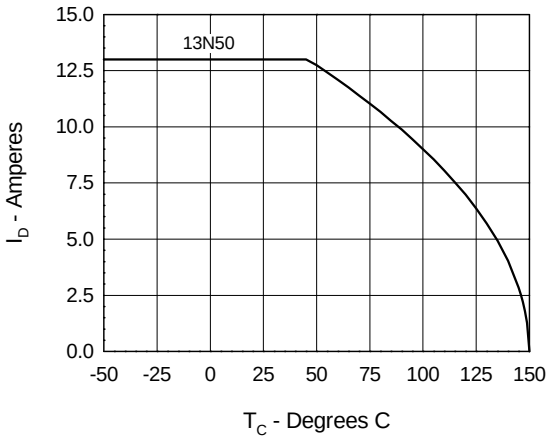


Figure 5. Drain Current vs. Case Temperature

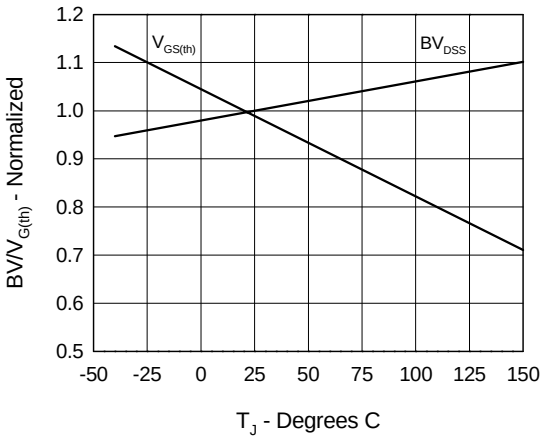


Figure 6. Admittance Curves

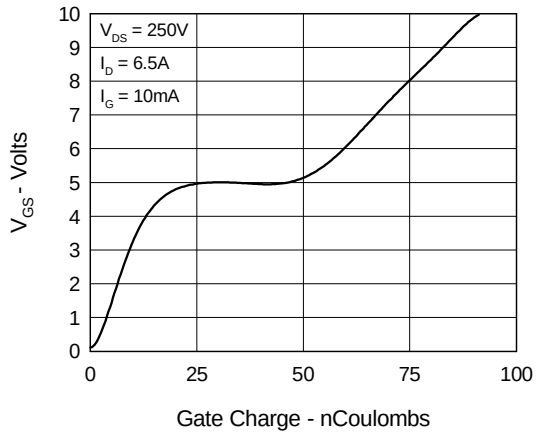


Figure 7. Gate Charge

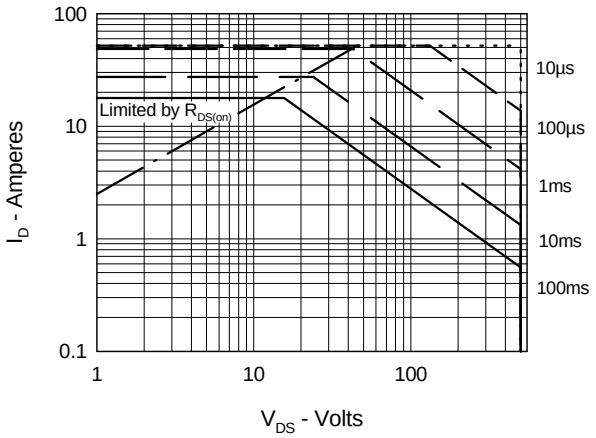


Figure 8. Capacitance Curves

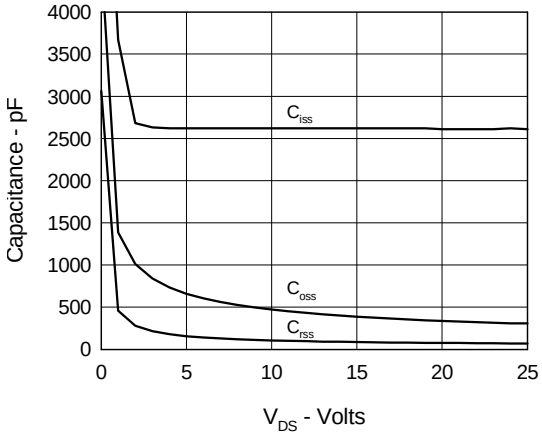


Figure 9. Source Current vs. Source to Drain Voltage

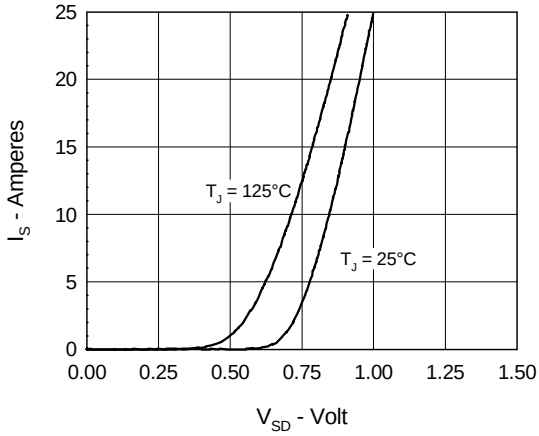


Figure10. Forward Bias Safe Operating Area

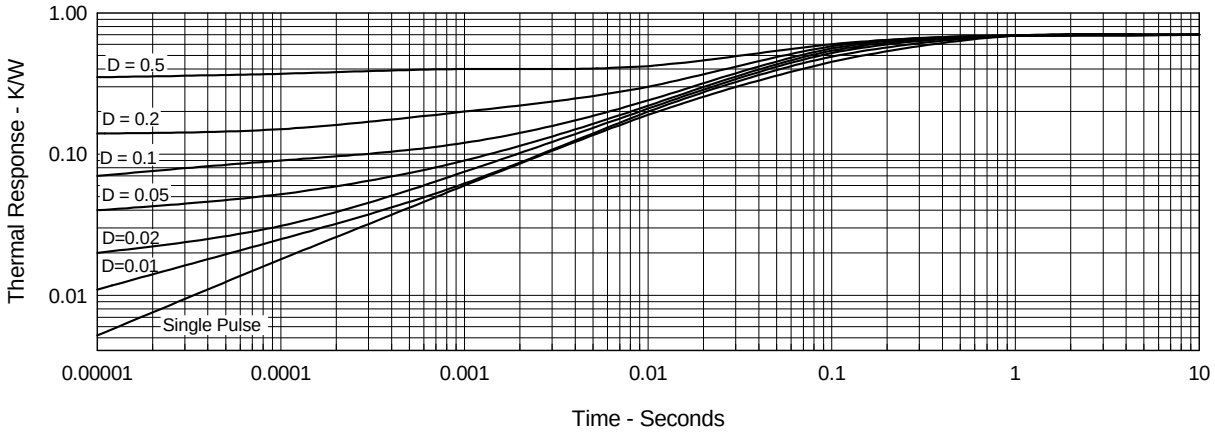


Figure 11. Transient Thermal Resistance