International **IƏR** Rectifier
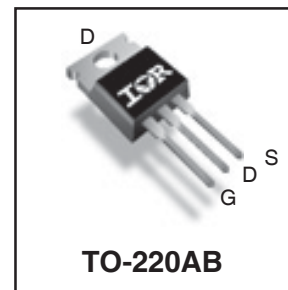
IRFB3006PbF

HEXFET® Power MOSFET

Applications
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free

V_{DSS}	60V
$R_{DS(on)}$ typ.	2.1mΩ
max.	2.5mΩ
I_D (Silicon Limited)	270A ①
I_D (Package Limited)	195A

TO-220AB

G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	270①	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	190 ①	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Wire Bond Limited)	195	
I_{DM}	Pulsed Drain Current ②	1080	
P_D @T_C = 25°C	Maximum Power Dissipation	375	W
	Linear Derating Factor	2.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ④	10	V/ns
T_J	Operating Junction and	-55 to + 175	
T_{STG}	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Avalanche Characteristics

E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ③	320	mJ
I_{AR}	Avalanche Current ②	See Fig. 14, 15, 22a, 22b,	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{θJC}$	Junction-to-Case ⑨	——	0.4	
$R_{θCS}$	Case-to-Sink, Flat Greased Surface	0.50	——	°C/W
$R_{θJA}$	Junction-to-Ambient ⑧⑨	——	62	

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10/6/08

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Static @ $T_J = 25°C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	——	——	V	$V_{GS} = 0V$, $I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.07	——	V/°C	Reference to 25°C, $I_D = 5mA$②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	2.1	2.5	mΩ	$V_{GS} = 10V$, $I_D = 170A$ ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	μA	$V_{DS} = 60V$, $V_{GS} = 0V$
		——	——	250		$V_{DS} = 60V$, $V_{GS} = 0V$, $T_J = 125°C$
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	——	——	-100		$V_{GS} = -20V$
R_G	Internal Gate Resistance	——	2.0	——	Ω	

Dynamic @ $T_J = 25°C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	280	——	——	S	$V_{DS} = 25V$, $I_D = 170A$
Q_g	Total Gate Charge	——	200	300	nC	$I_D = 170A$
Q_{gs}	Gate-to-Source Charge	——	37	——		$V_{DS} = 30V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	60			$V_{GS} = 10V$ ⑤
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	——	140	——		$I_D = 170A$, $V_{DS} = 0V$, $V_{GS} = 10V$
$t_{d(on)}$	Turn-On Delay Time	——	16	——	ns	$V_{DD} = 39V$
t_r	Rise Time	——	182	——		$I_D = 170A$
$t_{d(off)}$	Turn-Off Delay Time	——	118	——		$R_G = 2.7\Omega$
t_f	Fall Time	——	189	——		$V_{GS} = 10V$ ⑤
C_{iss}	Input Capacitance	——	8970	——	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	——	1020	——		$V_{DS} = 50V$
C_{rss}	Reverse Transfer Capacitance	——	534	——		$ƒ = 1.0$ MHz, See Fig. 5
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	——	1480	——		$V_{GS} = 0V$, $V_{DS} = 0V$ to 48V ⑦, See Fig. 11
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)⑥	——	1920	——		$V_{GS} = 0V$, $V_{DS} = 0V$ to 48V ⑥

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	270①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ②	——	——	1080	A	
V_{SD}	Diode Forward Voltage	——	——	1.3	V	$T_J = 25°C$, $I_S = 170A$, $V_{GS} = 0V$ ⑤
t_{rr}	Reverse Recovery Time	——	44	——	ns	$T_J = 25°C$ $V_R = 51V$,
		——	48	——		$T_J = 125°C$ $I_F = 170A$
Q_{rr}	Reverse Recovery Charge	——	63	——	nC	$T_J = 25°C$ di/dt = 100A/μs ⑤
		——	77	——		$T_J = 125°C$
I_{RRM}	Reverse Recovery Current	——	2.4	——	A	$T_J = 25°C$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by T_{Jmax}, starting $T_J = 25°C$, L = 0.022mH
   $R_G = 25\Omega$, $I_{AS} = 170A$, $V_{GS} = 10V$. Part not recommended for use above this value .

④ $I_{SD} \leq 170A$, di/dt $\leq 1360A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175°C$.

⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.

⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recom mended footprint and soldering techniques refer to application note #AN-994.

⑨ R_θ is measured at T_J approximately 90°C.
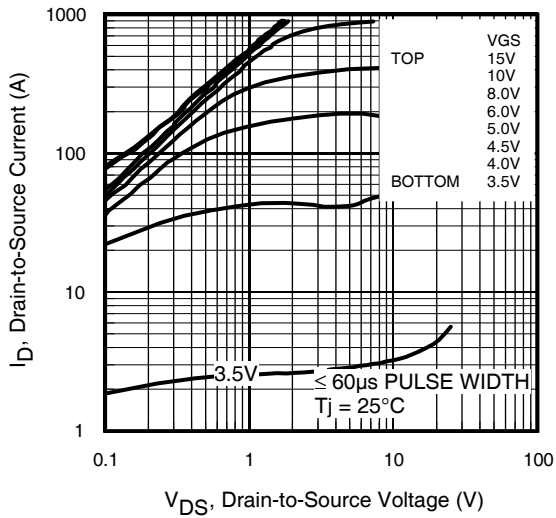
2

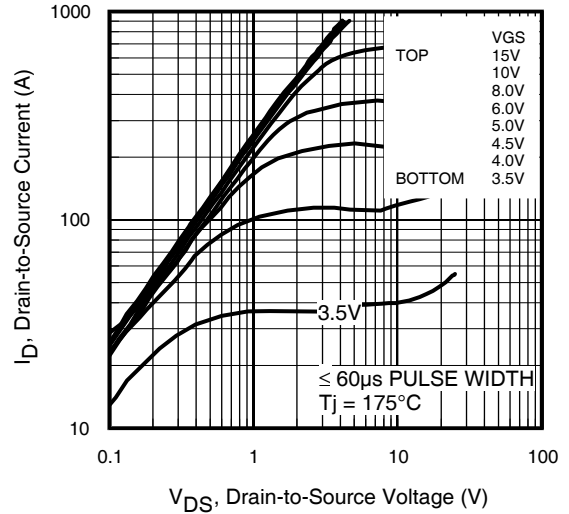**Fig 1.** Typical Output Characteristics

Fig 2. Typical Output Characteristics
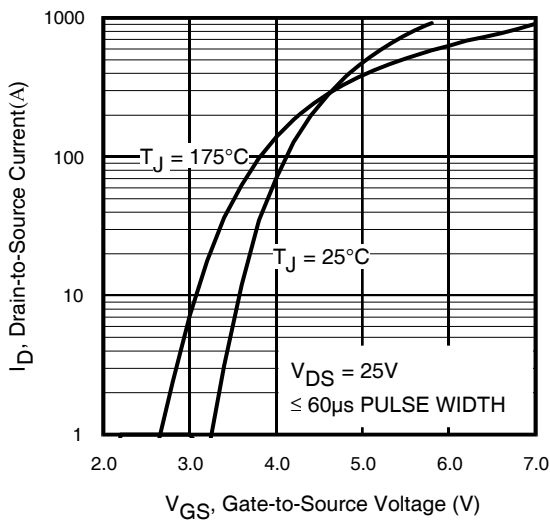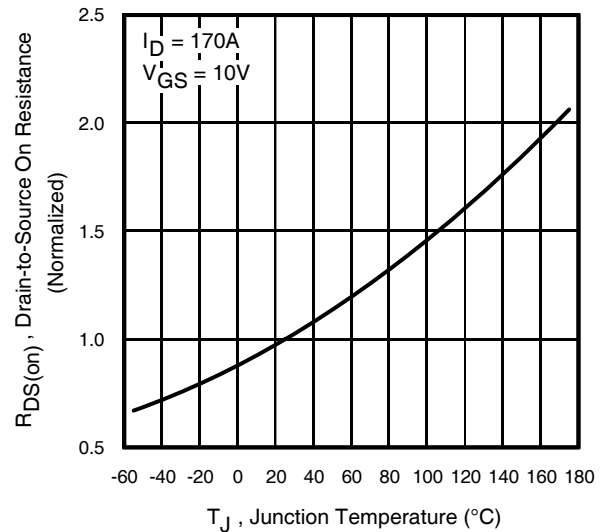
Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

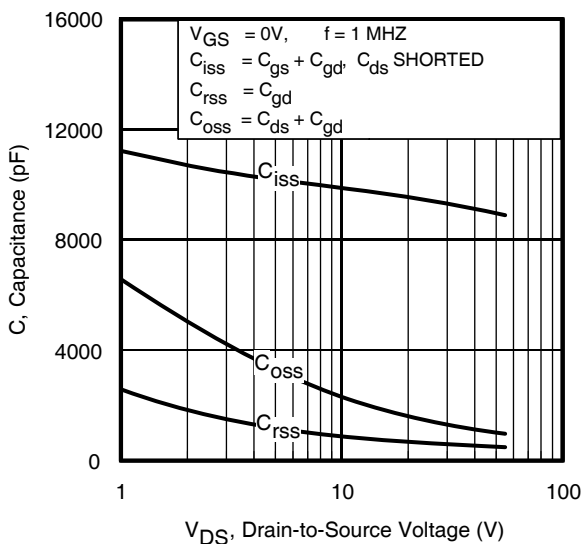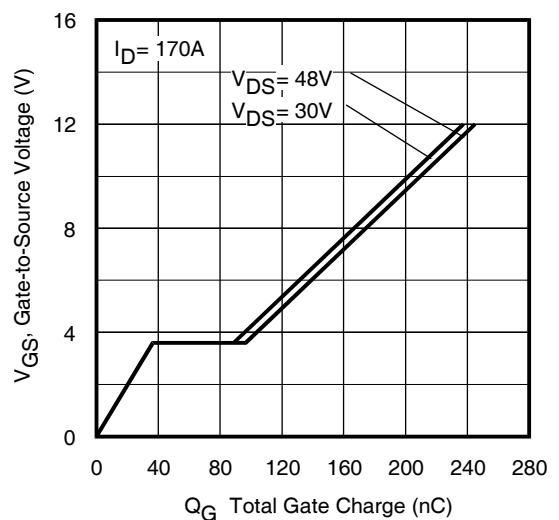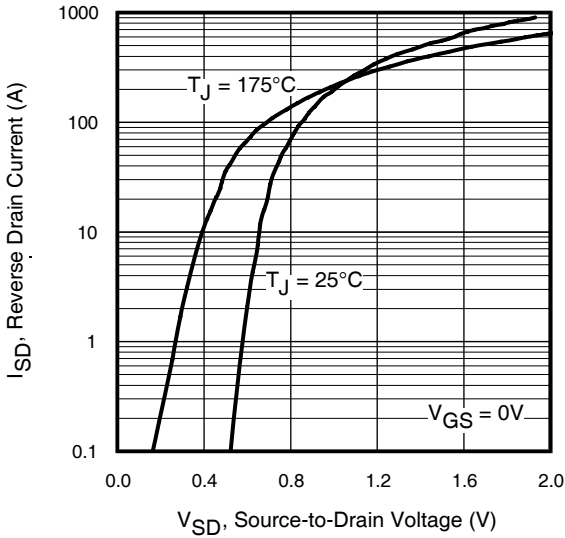**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage
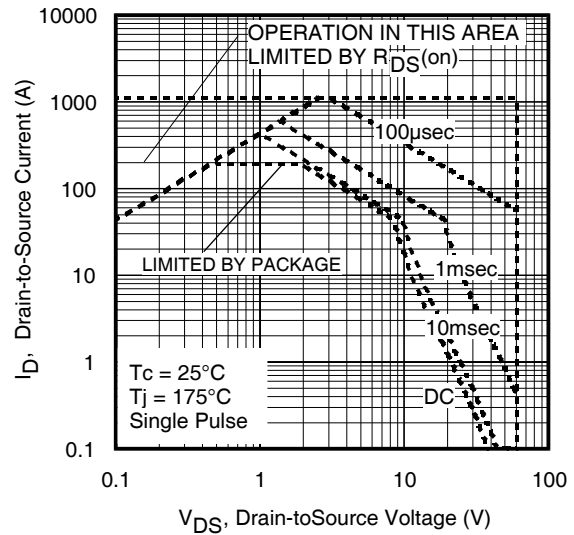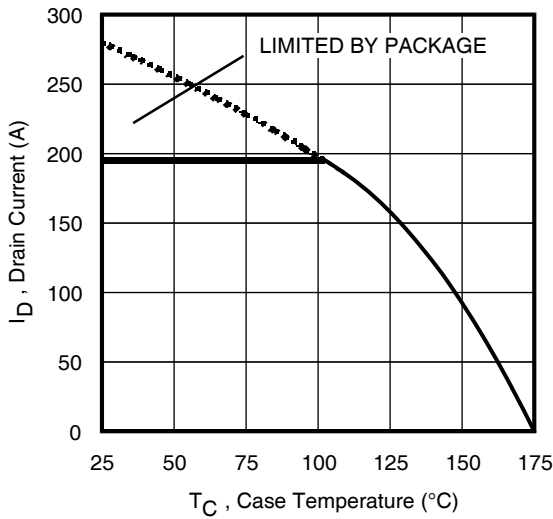
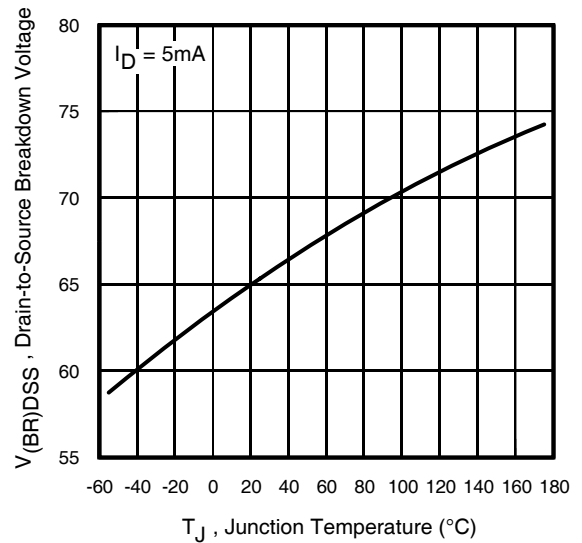**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

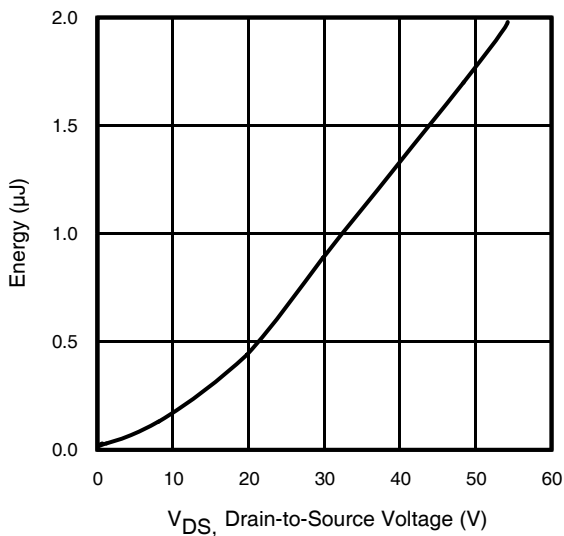**Fig 7.** Typical Source-Drain Diode
Forward Voltage
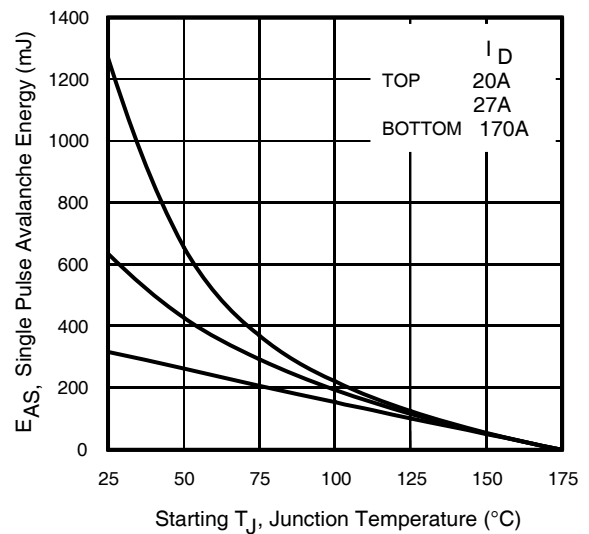
Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs.
Case Temperature

Fig 10. Drain-to-Source Breakdown Voltage

Fig 11. Typical C_{OSS} Stored Energy

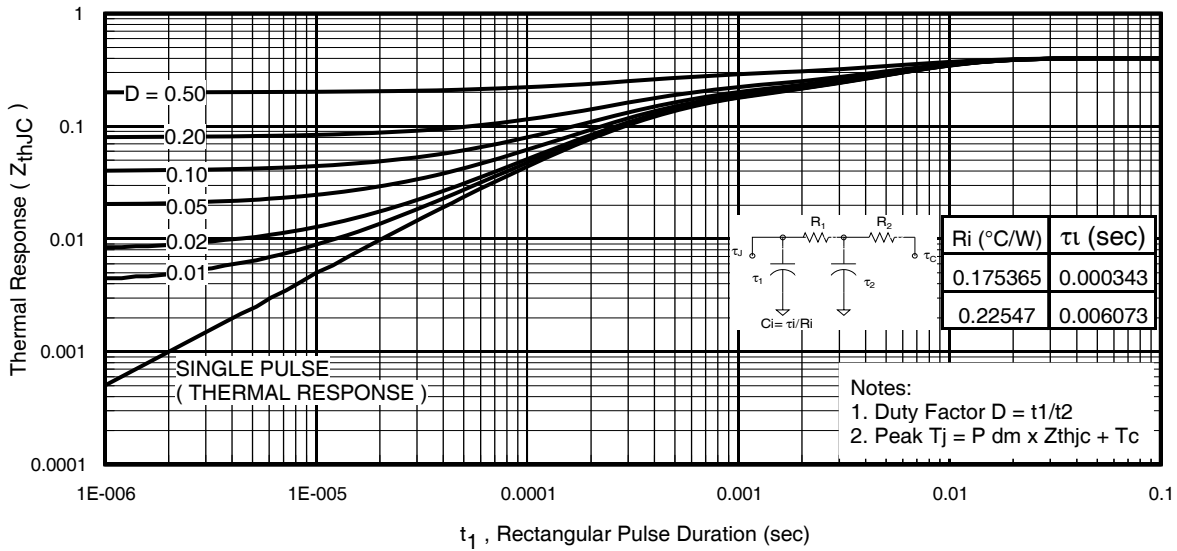**Fig 12.** Maximum Avalanche Energy Vs. DrainCurrent

4

Notes:
1. Duty Factor D = t1/t2
2. Peak Tj = P dm x Zthjc + Tc

Ri (°C/W)	τι (sec)
0.175365	0.000343
0.22547	0.006073

Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

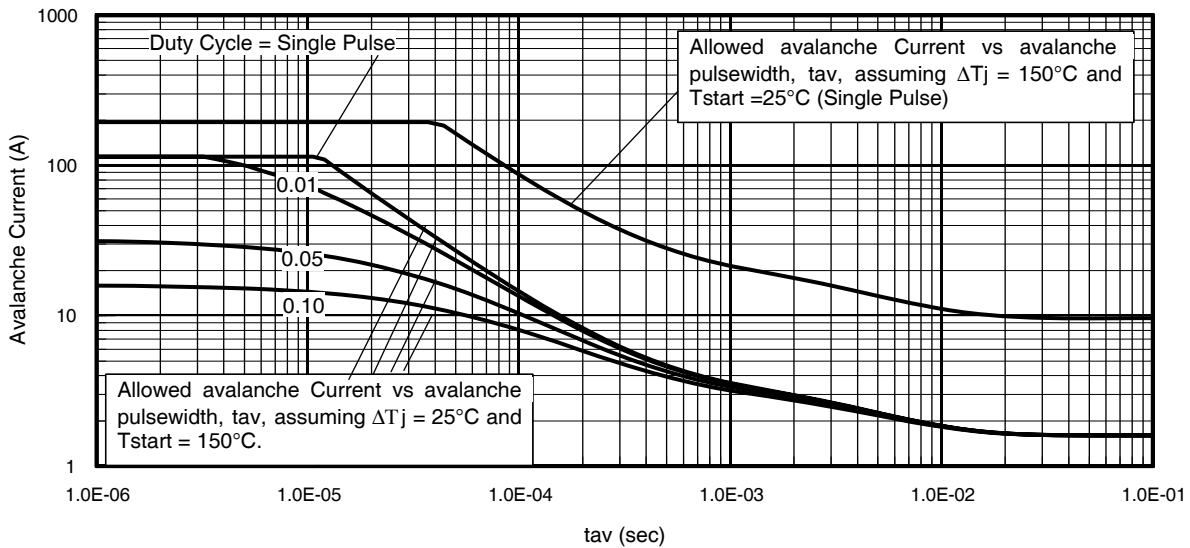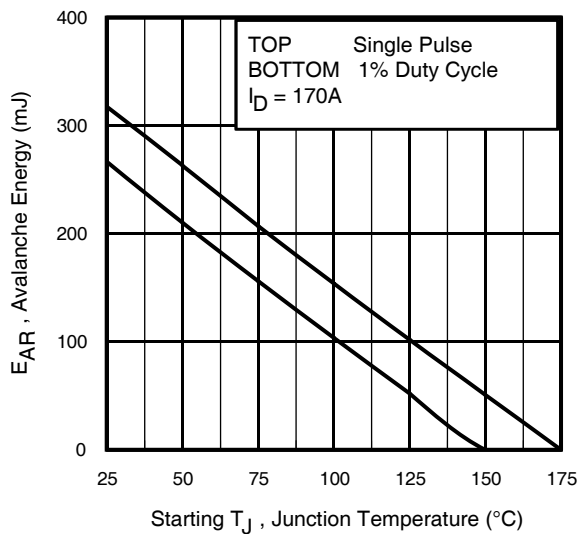**Fig 14.** Typical Avalanche Current vs.Pulsewidth

Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)
1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\ (ave)} = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T/\ Z_{thJC}$$
$$I_{av} = 2\Delta T/\ [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

International
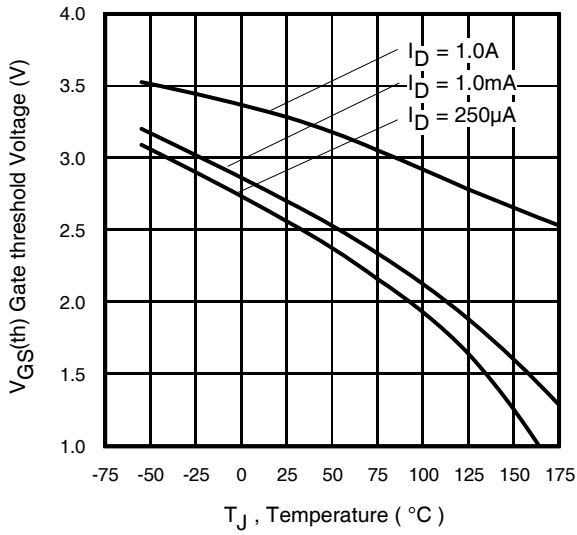**IƏR** Rectifier

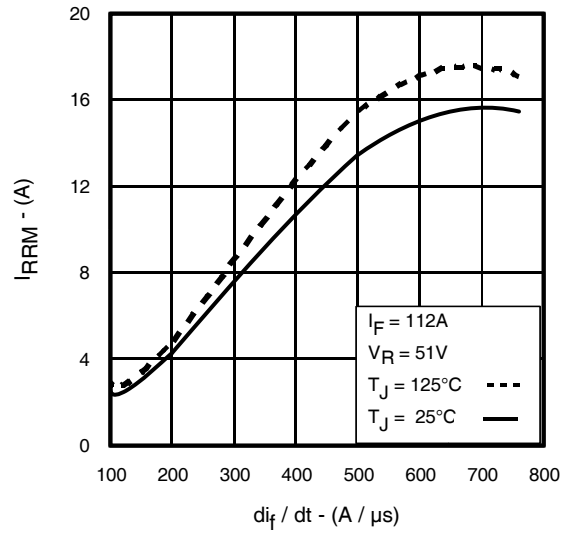**Fig 16.** Threshold Voltage Vs. Temperature

Fig. 17 - Typical Recovery Current vs. di$_f$/dt
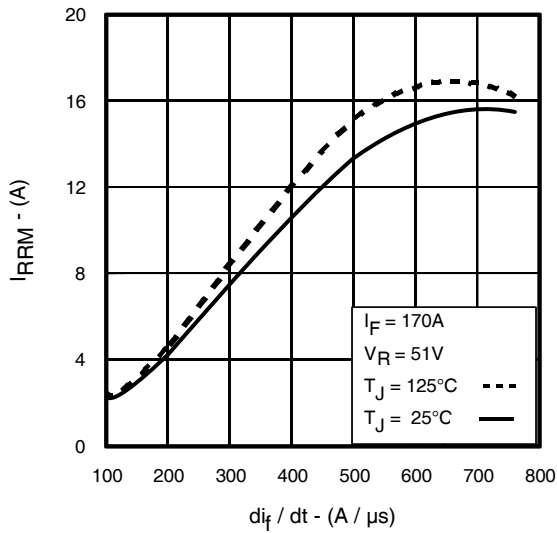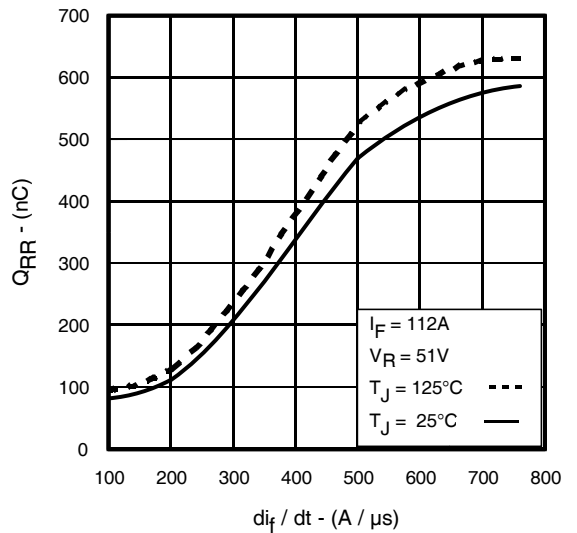

Fig. 18 - Typical Recovery Current vs. di$_f$/dt

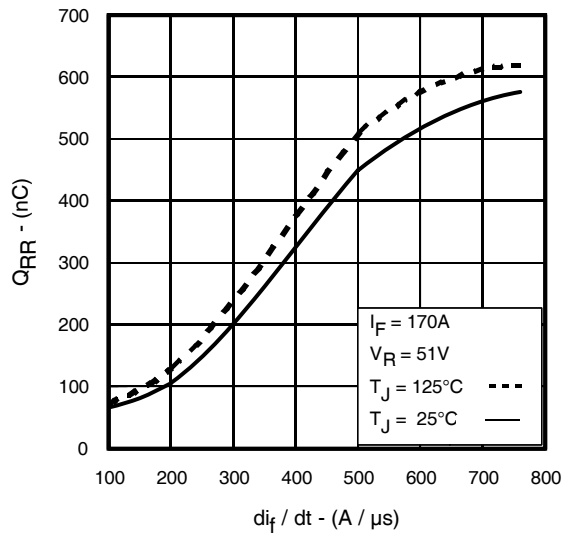**Fig. 19** - Typical Stored Charge vs. di$_f$/dt

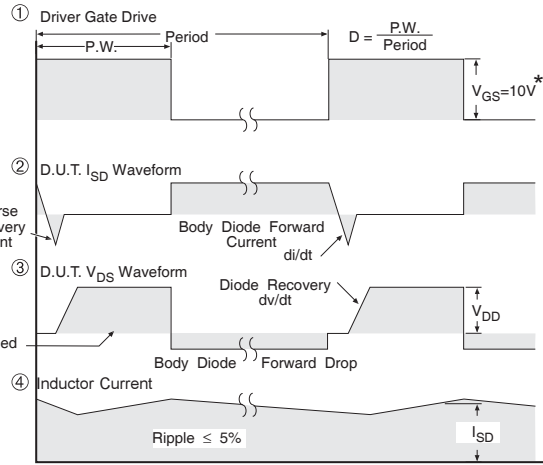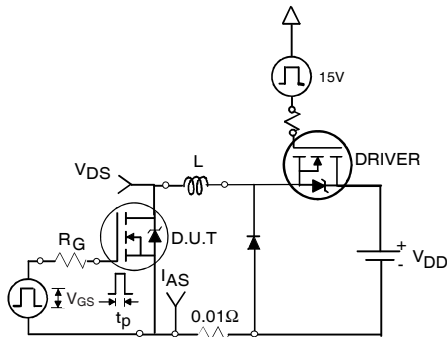**Fig. 20** - Typical Stored Charge vs. di$_f$/dt

Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

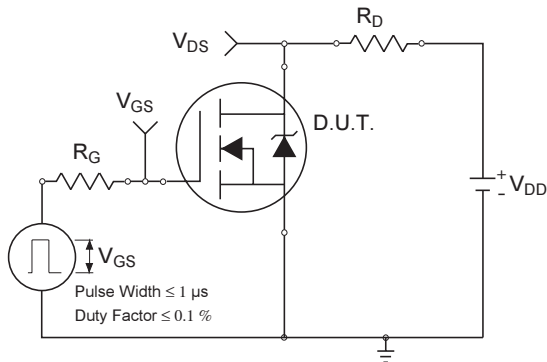**Fig 22a.** Unclamped Inductive Test Circuit

Fig 22b. Unclamped Inductive Waveforms

Fig 23a. Switching Time Test Circuit
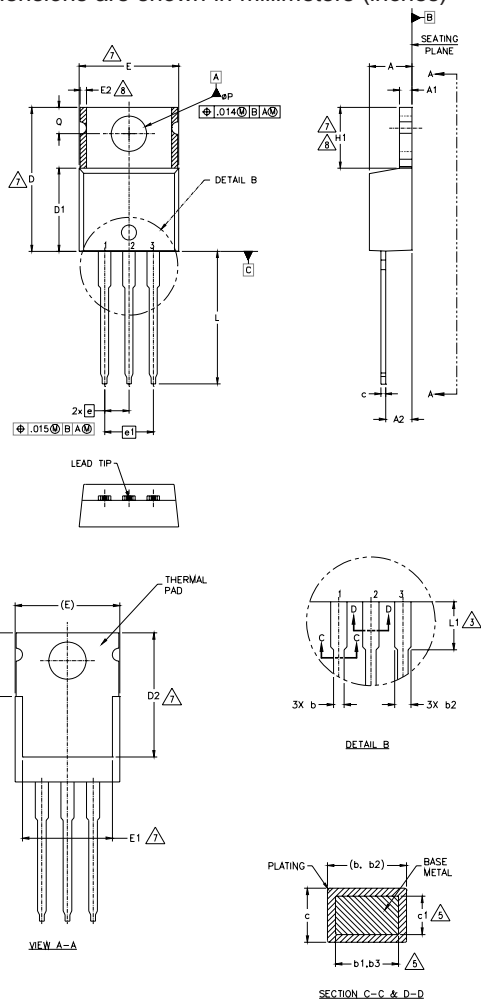

Fig 23b. Switching Time Waveforms

Fig 24a. Gate Charge Test Circuit

Fig 24b. Gate Charge Waveform

International
I⊘R Rectifier

TO-220AB Package Outline
Dimensions are shown in millimeters (inches)

NOTES:
1.– DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M– 1994.
2.– DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3.– LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4.– DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5.– DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
6.– CONTROLLING DIMENSION : INCHES.
7.– THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
8.– DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
9.– OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

| SYMBOL | DIMENSIONS | | | | NOTES |
| | MILLIMETERS | | INCHES | | |
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	–	0.76	–	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS

HEXFET
1.– GATE
2.– DRAIN
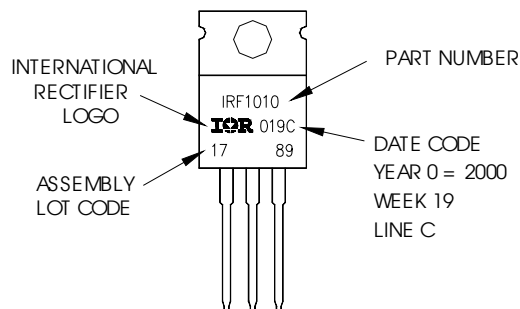3.– SOURCE

IGBTs, CoPACK
1.– GATE
2.– COLLECTOR
3.– EMITTER

DIODES
1.– ANODE
2.– CATHODE
3.– ANODE

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 2000
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

ASSEMBLY LOT CODE

DATE CODE
YEAR 0 = 2000
WEEK 19
LINE C

IRF1010
I⊘R 019C
17   89

TO-220AB packages are not recommended for Surface Mount Application.
Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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